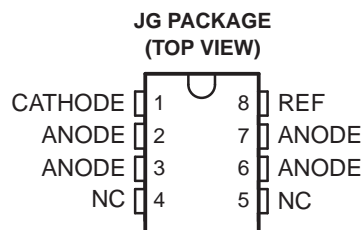


## FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree <sup>(1)</sup>**
- **0.4% Initial Voltage Tolerance**
- **0.2-Ω Typical Output Impedance**
- **Fast Turnon . . . 500 ns**
- **Sink Current Capability . . . 1 mA to 100 mA**
- **Low Reference Current (REF)**
- **Adjustable Output Voltage . . .  $V_{I(\text{ref})}$  to 36 V**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



NC – No internal connection  
ANODE terminals are connected internally.

## DESCRIPTION/ORDERING INFORMATION

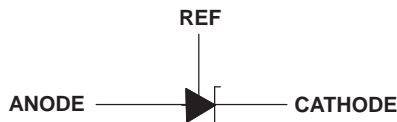
The TL1431 is a precision programmable reference with specified thermal stability over the automotive temperature range. The output voltage can be set to any value between  $V_{I(\text{ref})}$  (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). This device has a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turnon characteristic, making the device an excellent replacement for Zener diodes and other types of references in applications such as onboard regulation, adjustable power supplies, and switching power supplies.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	TL1431QDREP	1431QE
–55°C to 125°C	SOIC – D	Reel of 2500	TL1431MDREP	1431ME

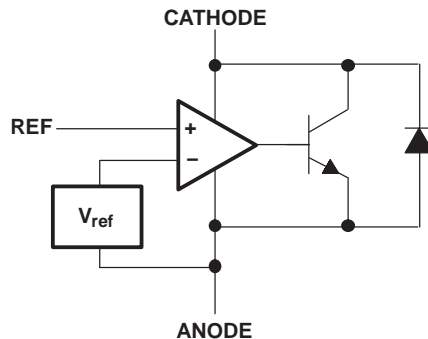
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### SYMBOL

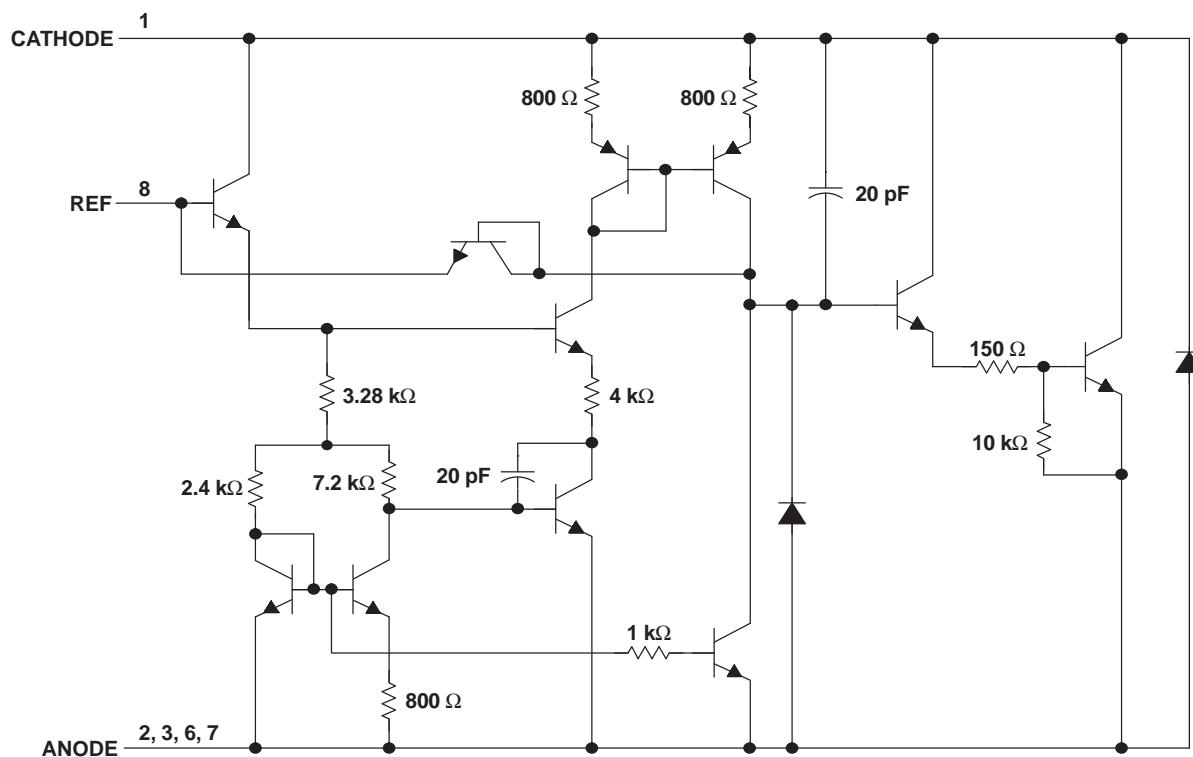


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## FUNCTIONAL BLOCK DIAGRAM



## EQUIVALENT SCHEMATIC<sup>(1)</sup>



(1) All component values are nominal.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{KA}$	Cathode voltage <sup>(2)</sup>		37	V
$I_{KA}$	Continuous cathode current range	–100	150	mA
$I_{I(ref)}$	Reference input current range	–50 $\mu$ A	10 mA	
$\theta_{JA}$ (High)	Package thermal impedance (High K Board) <sup>(3)(4)</sup>		97	°C/W
$\theta_{JA}$ (Low)	Package thermal impedance (Low K Board) <sup>(3)(4)</sup>		165	°C/W
$T_J$	Operating virtual junction temperature <sup>(5)</sup>		150	°C
	Continuous total power dissipation	See Dissipation Rating Table		
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C
$T_{stg}$	Storage temperature range <sup>(5)</sup>	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ANODE, unless otherwise noted.
- (3) Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Long-term high-temperature storage and/or use at the absolute maximum ratings may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

## DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	PACKAGE THERMAL IMPEDANCE	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ ABSOLUTE MAXIMUM POWER RATING	$T_A = 85^\circ\text{C}$ ABSOLUTE MAXIMUM POWER RATING	$T_A = 125^\circ\text{C}$ ABSOLUTE MAXIMUM POWER RATING
D	1102 mW	97°C/W (High K Board)	10 mW/°C	824 mW	670 mW	257 mW
		165°C/W (Low K Board)	6 mW/°C	484 mW	393 mW	151 mW

## Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{KA}$	Cathode voltage	$V_{I(ref)}$	36	V
$I_{KA}$	Cathode current	1	100	mA
$T_A$	Operating free-air temperature	–55	125	°C

## Electrical Characteristics

at specified free-air temperature,  $I_{KA} = 10 \text{ mA}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$ <sup>(1)</sup>	TEST CIRCUIT	MIN	TYP	MAX	UNIT
$V_{I(\text{ref})}$ Reference input voltage	$V_{KA} = V_{I(\text{ref})}$	25°C	Figure 1	2490	2500	2510	mV
		Full range		2470		2530	
$V_{I(\text{dev})}$ Deviation of reference input voltage over full temperature range <sup>(2)</sup>	$V_{KA} = V_{I(\text{ref})}$	Full range	Figure 1	17			mV
$\frac{\Delta V_{I(\text{ref})}}{\Delta V_{KA}}$ Ratio of change in reference input voltage to the change in cathode voltage	$\Delta V_{KA} = 3 \text{ V to } 36 \text{ V}$	Full range	Figure 2	-1.1		-2	mV/V
$I_{I(\text{ref})}$ Reference input current	$R1 = 10 \text{ k}\Omega, R2 = \infty$	25°C	Figure 2	1.5	2.5		$\mu\text{A}$
		Full range			4		
$I_{I(\text{dev})}$ Deviation of reference input current over full temperature range <sup>(2)</sup>	$R1 = 10 \text{ k}\Omega, R2 = \infty$	Full range	Figure 2	0.5			$\mu\text{A}$
$I_{\text{min}}$ Minimum cathode current for regulation	$V_{KA} = V_{I(\text{ref})}$	25°C	Figure 1	0.45	1		mA
$I_{\text{off}}$ Off-state cathode current	$V_{KA} = 36 \text{ V}, V_{I(\text{ref})} = 0$	25°C	Figure 3	0.18	0.5		$\mu\text{A}$
		Full range			2		
$ z_{KA} $ Output impedance <sup>(3)</sup>	$V_{KA} = V_{I(\text{ref})}, f \leq 1 \text{ kHz}, I_{KA} = 1 \text{ mA to } 100 \text{ mA}$	25°C	Figure 1	0.2	0.4		$\Omega$

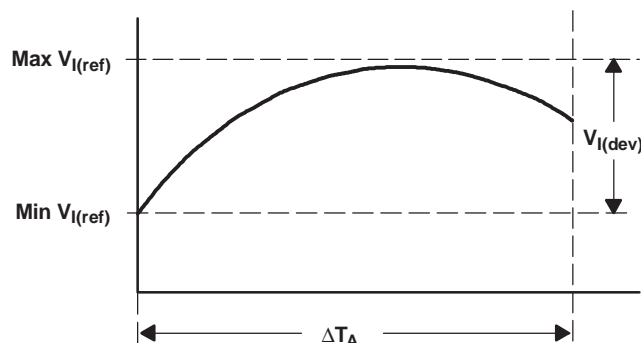
(1) Full range is -40°C to 125°C for Q-suffix devices; -55°C to 125°C for M-suffix devices.

(2) The deviation parameters  $V_{I(\text{dev})}$  and  $I_{I(\text{dev})}$  are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage  $\alpha_{V_{I(\text{ref})}}$  is defined as:

$$\left| \alpha_{V_{I(\text{ref})}} \right| \left( \frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left( \frac{V_{I(\text{dev})}}{V_{I(\text{ref})} \text{ at } 25^\circ\text{C}} \right) \times 10^6}{\Delta T_A}$$

where:

$\Delta T_A$  is the rated operating temperature range of the device.



$\alpha_{V_{I(\text{ref})}}$  is positive or negative, depending on whether minimum  $V_{I(\text{ref})}$  or maximum  $V_{I(\text{ref})}$ , respectively, occurs at the lower temperature.

(3) The output impedance is defined as:  $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$|z'| = \frac{\Delta V}{\Delta I}, \text{ which is approximately equal to } |z_{KA}| = \left( 1 + \frac{R1}{R2} \right).$$

## PARAMETER MEASUREMENT INFORMATION

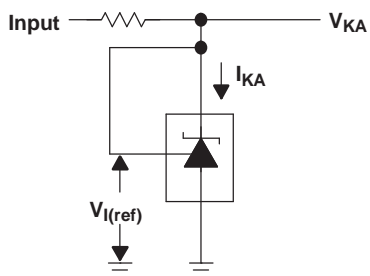


Figure 1. Test Circuit for  $V_{(KA)} = V_{ref}$

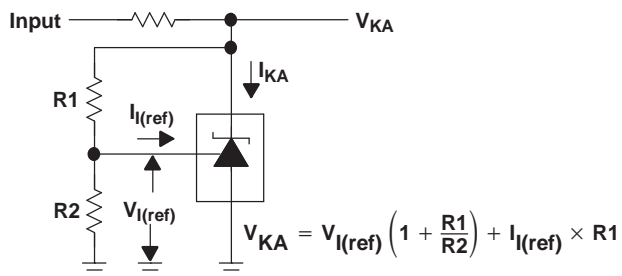


Figure 2. Test Circuit for  $V_{(KA)} > V_{ref}$

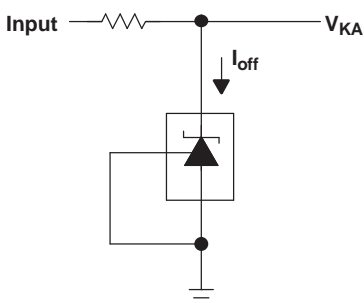


Figure 3. Test Circuit for  $I_{off}$

## TYPICAL CHARACTERISTICS<sup>(1)</sup>

- (1) Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TABLE OF GRAPHS

	FIGURE
Reference voltage vs Free-air temperature	4
Reference current vs Free-air temperature	5
Cathode current vs Cathode voltage	6, 7
Off-state cathode current vs Free-air temperature	8
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Equivalent input-noise voltage vs Frequency	10
Equivalent input-noise voltage over a 10-s period	11
Small-signal voltage amplification vs Frequency	12
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Pulse response	14
Stability boundary conditions	15

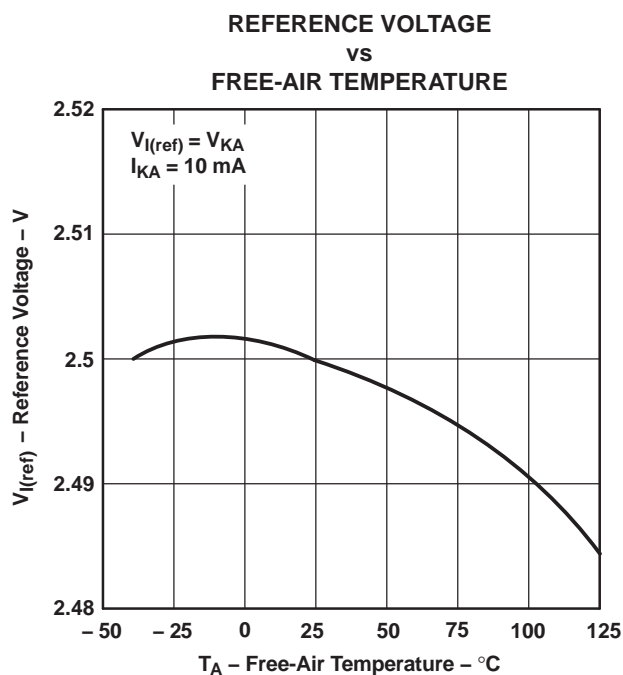


Figure 4.

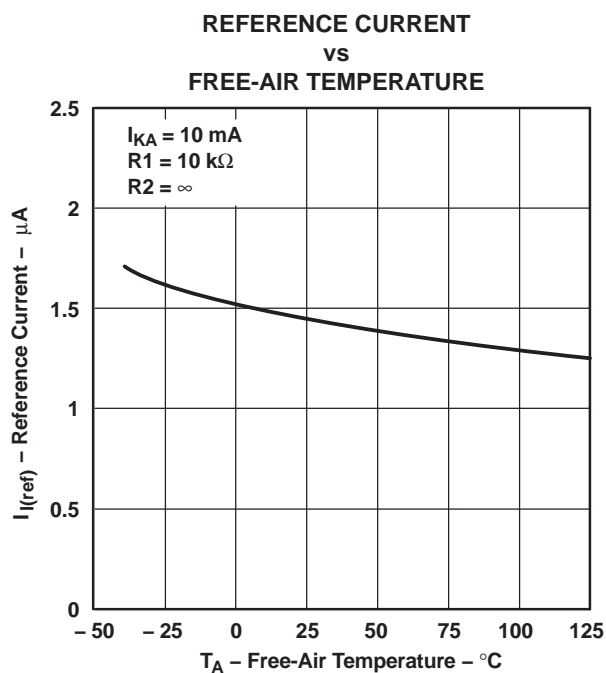


Figure 5.

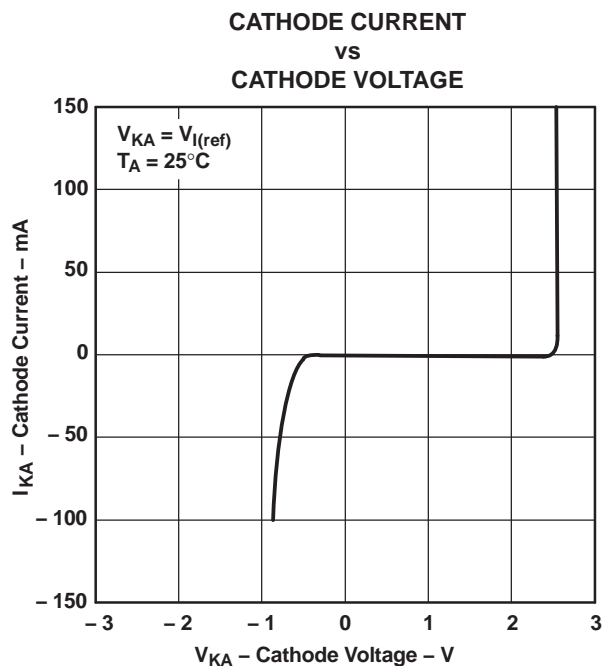


Figure 6.

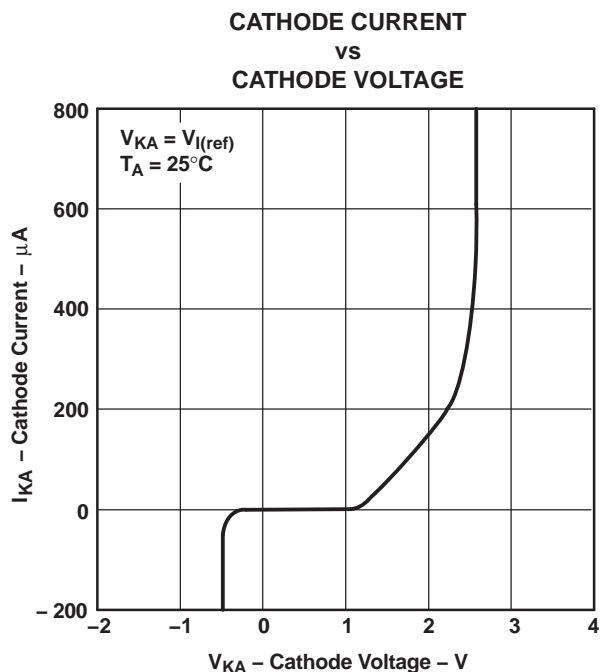


Figure 7.

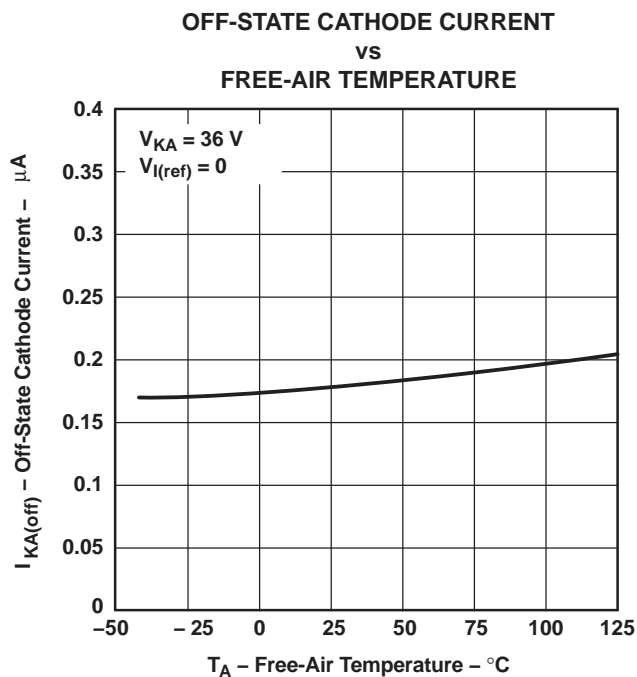


Figure 8.

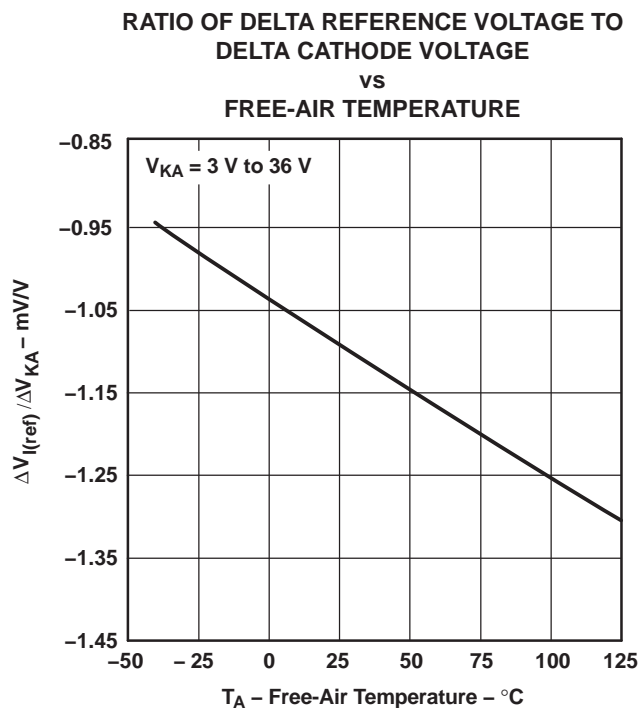


Figure 9.

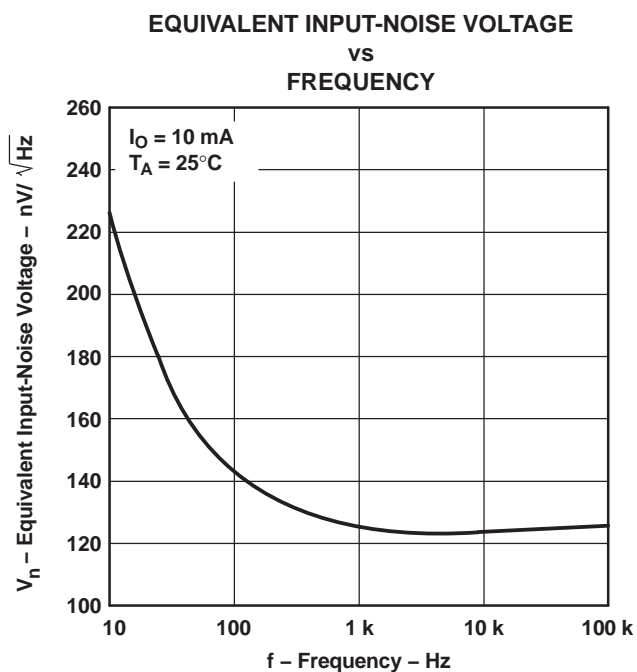
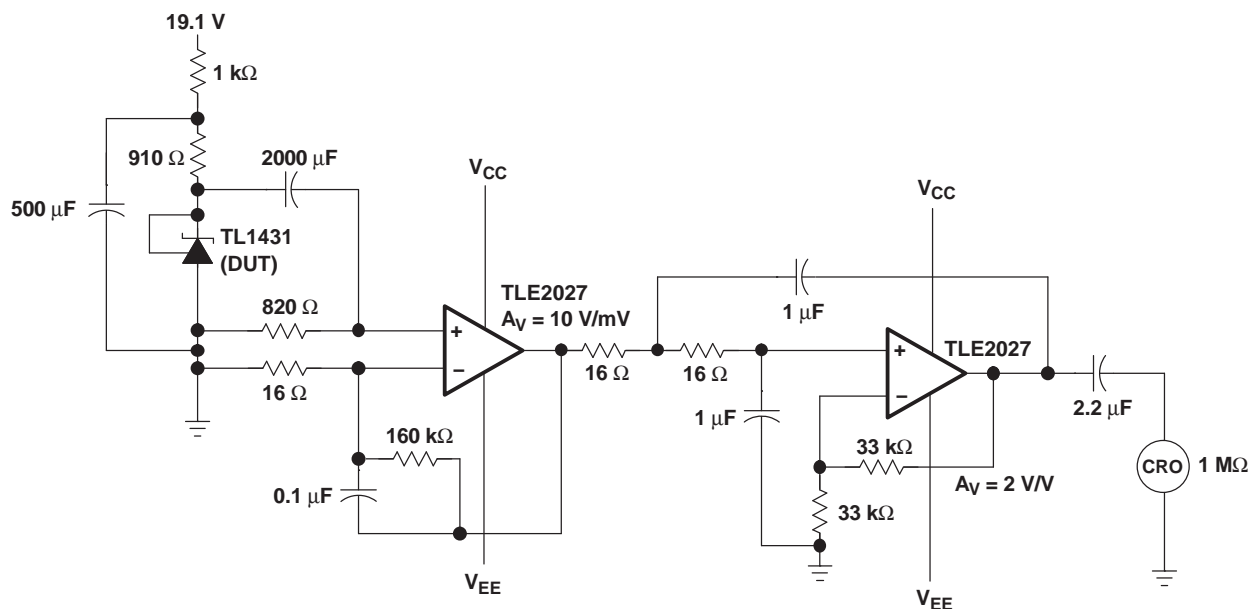
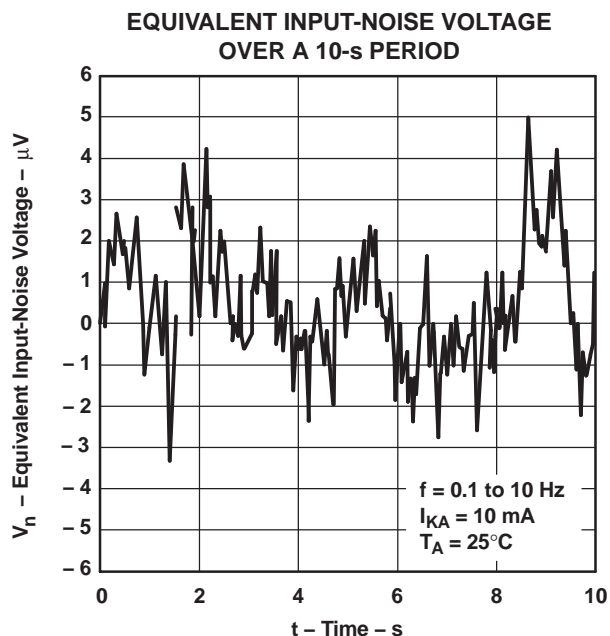


Figure 10.





TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT INPUT-NOISE VOLTAGE

Figure 11.

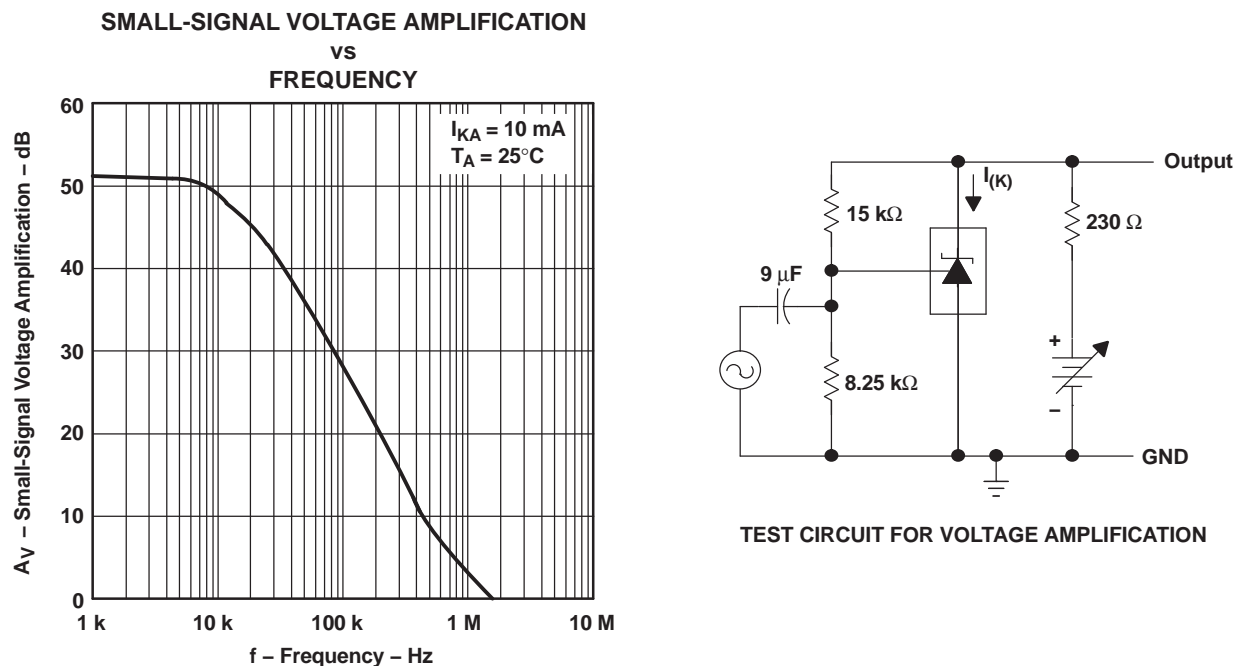


Figure 12.

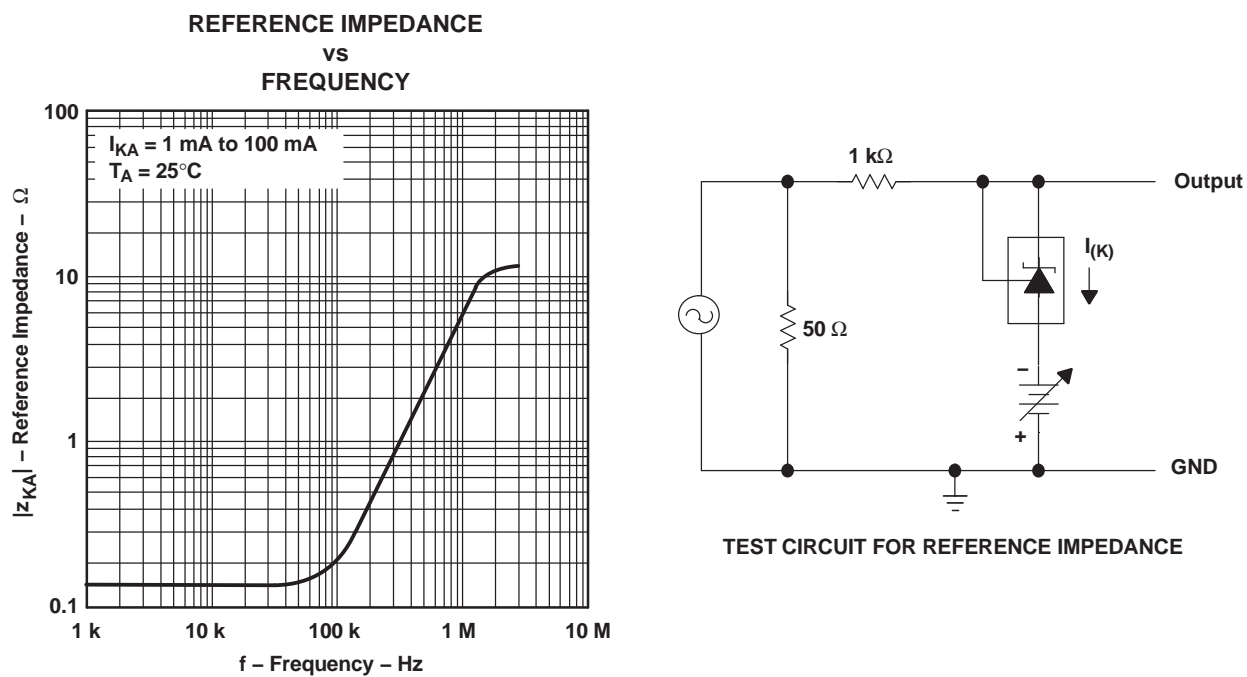


Figure 13.

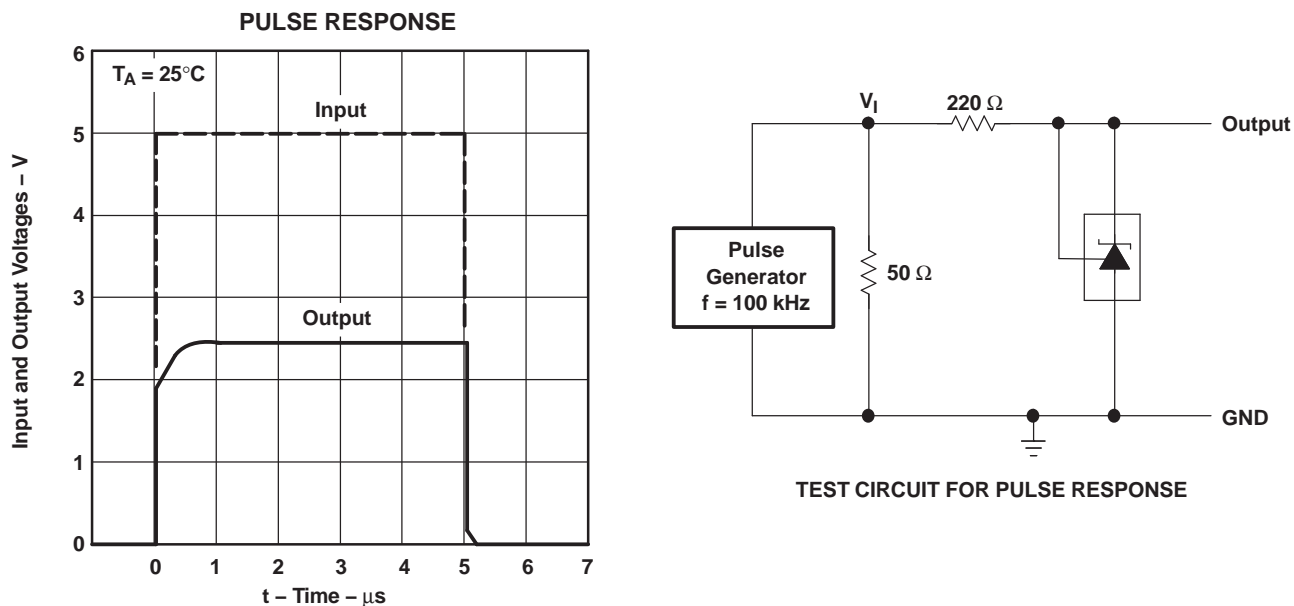
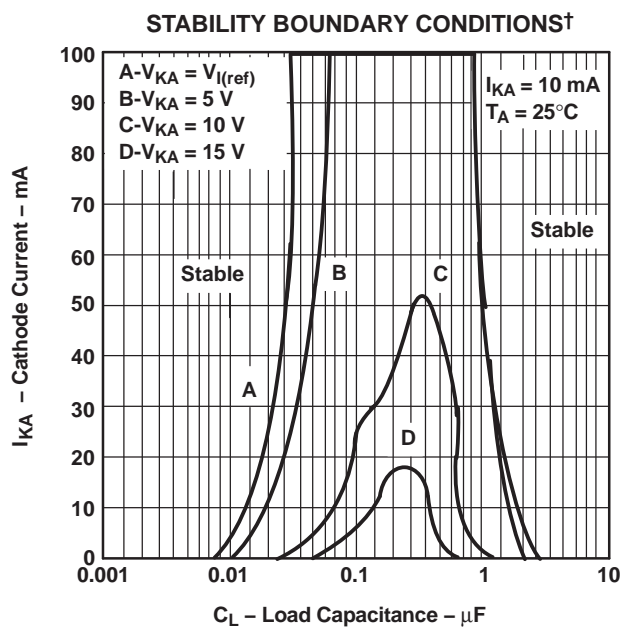


Figure 14.



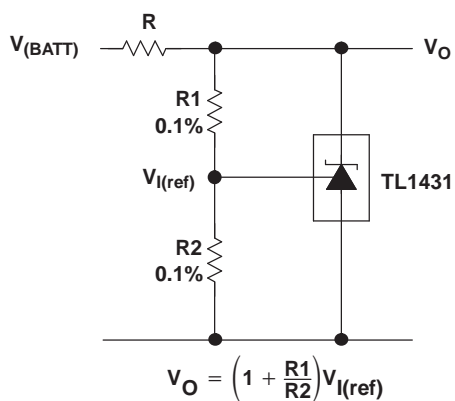
† The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ are adjusted to establish the initial VKA and IKA conditions, with CL = 0. VBATT and CL then are adjusted to determine the ranges of stability.

Figure 15.

## APPLICATION INFORMATION

### TABLE OF APPLICATION CIRCUITS

APPLICATION	FIGURE
Shunt regulator	16
Single-supply comparator with temperature-compensated threshold	17
Precision high-current series regulator	18
Output control of a three-terminal fixed regulator	19
Higher-current shunt regulator	20
Crowbar	21
Precision 5-V, 1.5-A, 0.5% regulator	22
5-V precision regulator	23
PWM converter with 0.5% reference	24
Voltage monitor	25
Delay timer	26
Precision current limiter	27
Precision constant-current sink	28



NOTE A: R should provide cathode current  $\geq 1$  mA to the TL1431 at minimum  $V_{(BATT)}$ .

Figure 16. Shunt Regulator

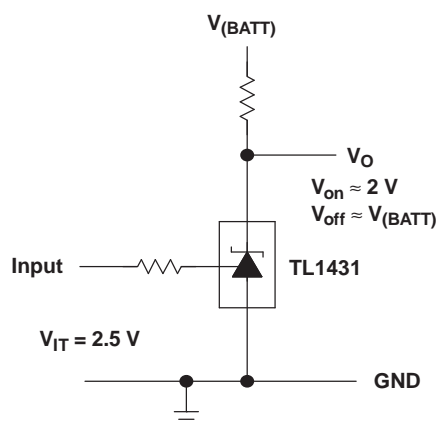
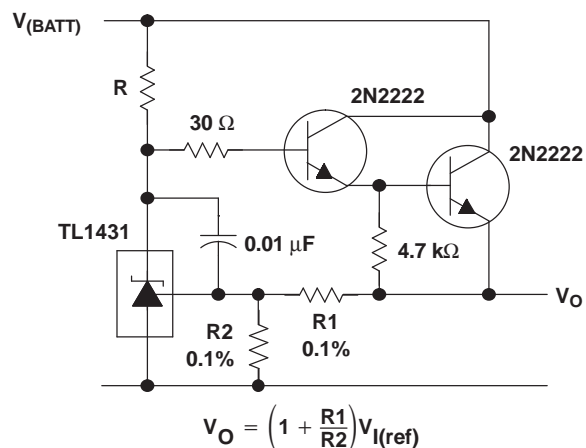


Figure 17. Single-Supply Comparator With Temperature-Compensated Threshold



NOTE A: R should provide cathode current  $\geq 1$  mA to the TL1431 at minimum  $V_{(\text{BATT})}$ .

Figure 18. Precision High-Current Series Regulator

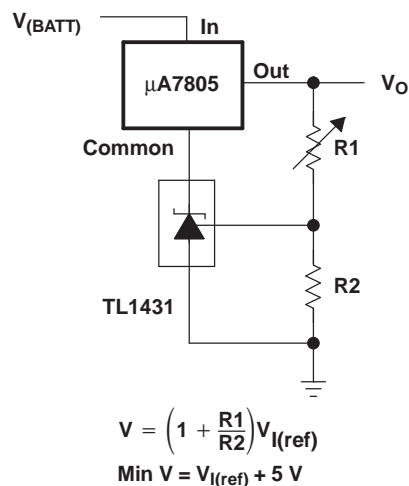


Figure 19. Output Control of a Three-Terminal Fixed Regulator

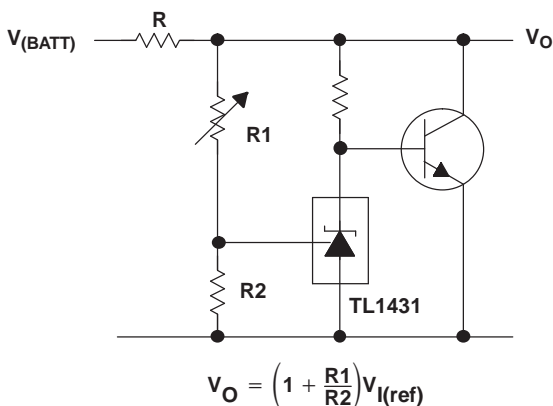
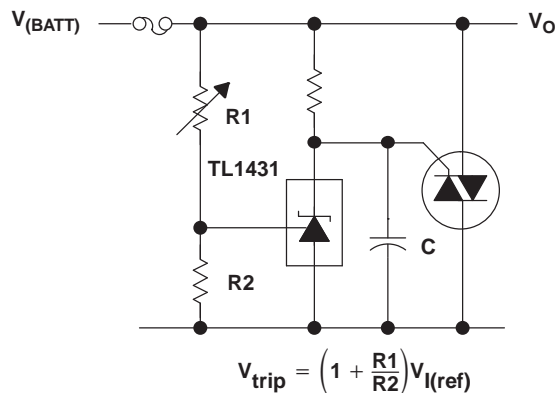


Figure 20. Higher-Current Shunt Regulator



NOTE A: Refer to the stability boundary conditions in Figure 15 to determine allowable values for C.

Figure 21. Crowbar

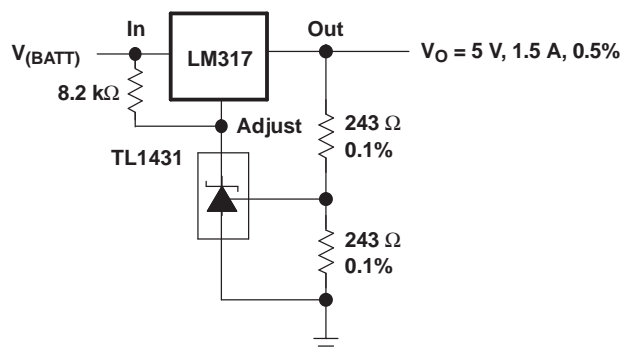
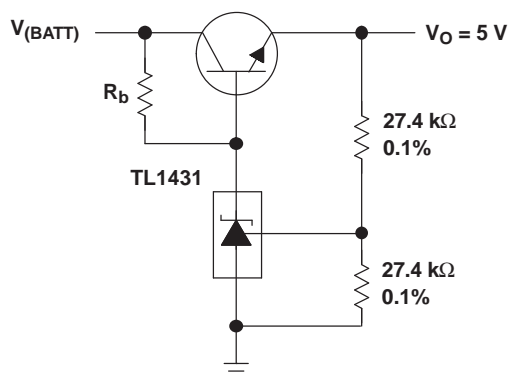


Figure 22. Precision 5-V, 1.5-A, 0.5% Regulator



NOTE A:  $R_b$  should provide cathode current  $\geq 1$  mA to the TL1431.

Figure 23. Precision Regulator

# TL1431-EP PRECISION PROGRAMMABLE REFERENCE

SLVS529C–APRIL 2004–REVISED DECEMBER 2006

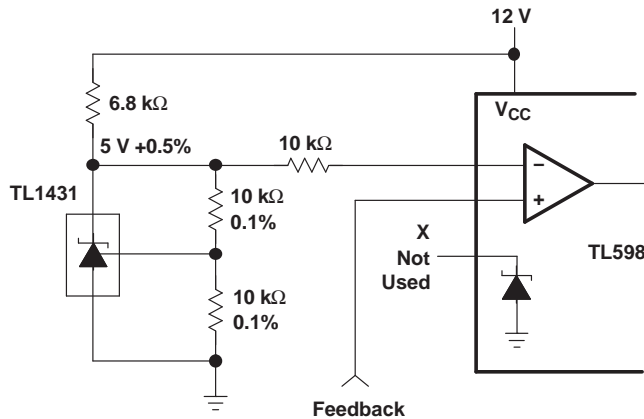


Figure 24. PWM Converter With 0.5% Reference

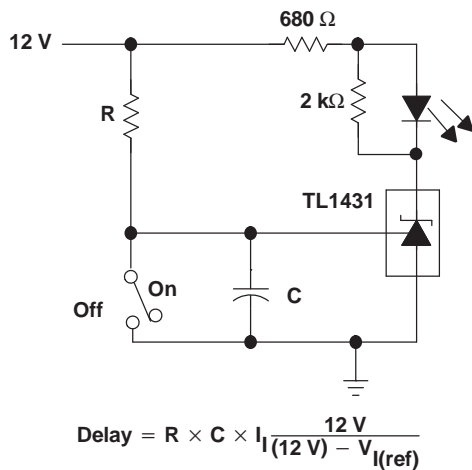
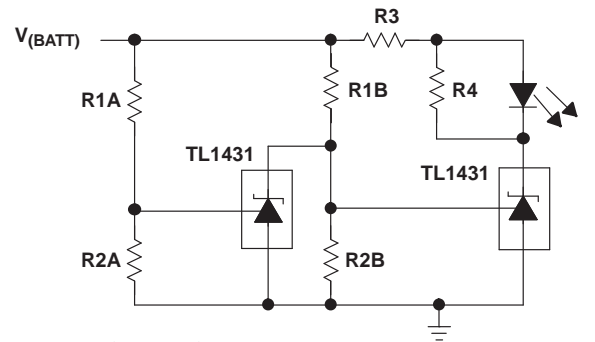


Figure 26. Delay Timer



$$\text{Low Limit} = \left(1 + \frac{R1B}{R2B}\right) V_{I(\text{ref})}$$

$$\text{High Limit} = \left(1 + \frac{R1A}{R2A}\right) V_{I(\text{ref})}$$

LED on When Low Limit < V(BATT) < High Limit

NOTE A: Select R3 and R4 to provide the desired LED intensity and cathode current  $\geq 1$  mA to the TL1431.

Figure 25. Voltage Monitor

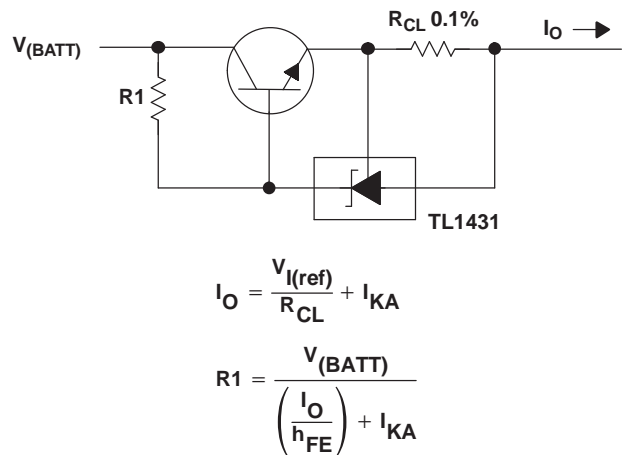


Figure 27. Precision Current Limiter

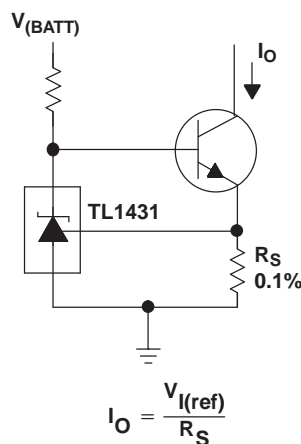


Figure 28. Precision Constant-Current Sink

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL1431MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431MDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431QDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04756-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04756-02XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

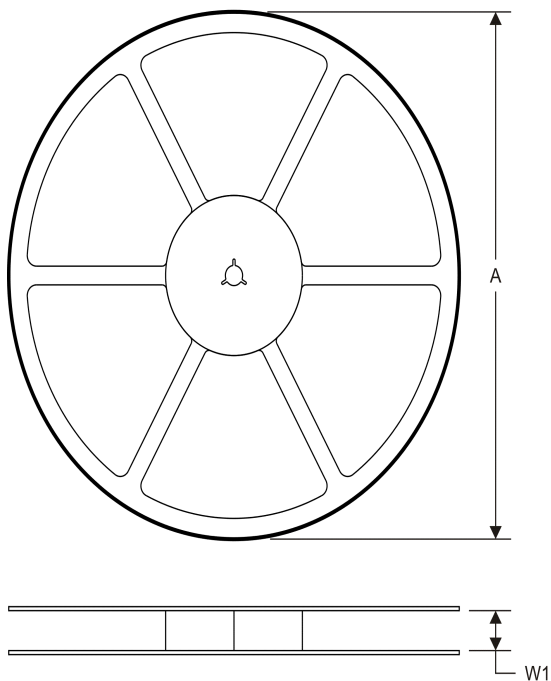
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF TL1431-EP :

- Catalog: [TL1431](#)
- Automotive: [TL1431-Q1](#)
- Military: [TL1431M](#)
- Space: [TL1431-SP](#)

### NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1431MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL1431QDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1431MDREP	SOIC	D	8	2500	367.0	367.0	35.0
TL1431QDREP	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.