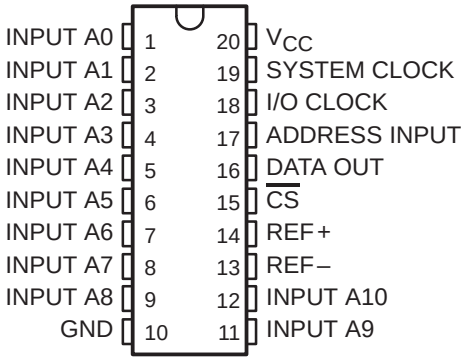
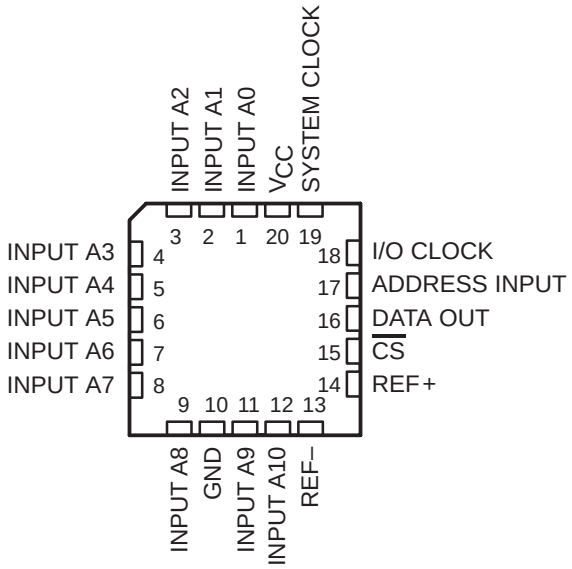
- **10-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Standalone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample-and-Hold Function**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **Pinout and Control Signals Compatible With TLC540 and TLC549 Families of 8-Bit A/D Converters**
- **CMOS Technology**

PARAMETER	VALUE
Channel Acquisition Sample Time	5.5 μs
Conversion Time (Max)	21 μs
Samples Per Second (Max)	32×10^3
Power Dissipation (Max)	6 mW

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC1541 is a CMOS A/D converter built around a 10-bit switched-capacitor successive-approximation A/D converter. The device is designed for serial interface to a microprocessor or peripheral using a 3-state output with up to four control inputs (including independent SYSTEM CLOCK, I/O CLOCK, chip select [$\overline{CS}$], and ADDRESS INPUT). A 2.1-MHz system clock for the TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates up to 32 258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip, 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage and a sample-and-hold function that operates automatically.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC1541CDW	TLC1541CFN	TLC1541CN
–40°C to 85°C	TLC1541IDW	TLC1541IFN	TLC1541IN

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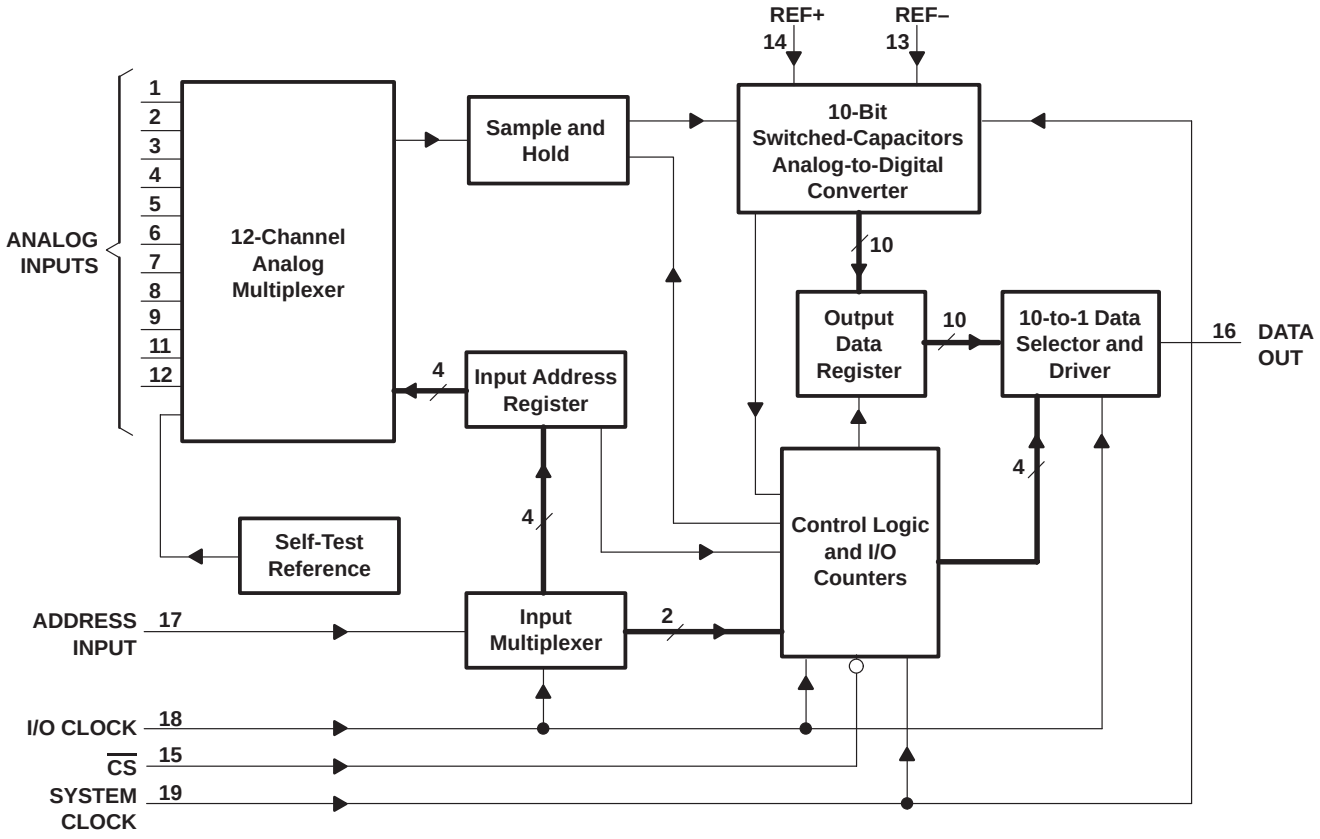
description (continued)

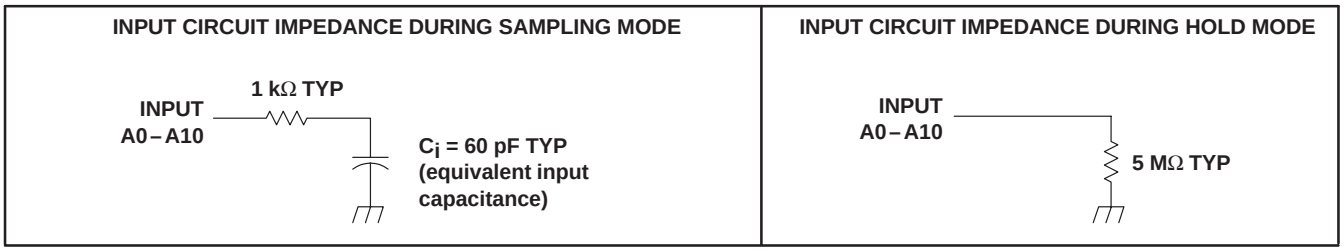
The converters incorporated in the TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error conversion in 21 μs over the full operating temperature range.

The TLC1541 is available in DW, FN, and N packages. The C-suffix versions are characterized for operation from 0°C to 70°C. The I-suffix versions are characterized for operation from –40°C to 85°C.

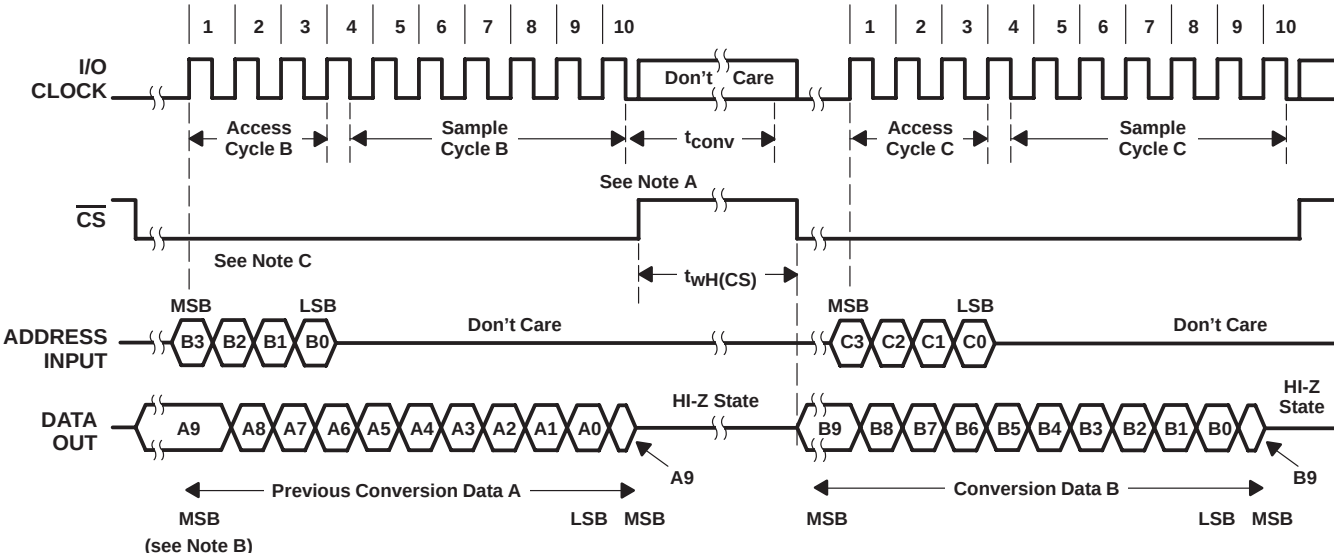
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 44 system clock periods, initiates on the tenth falling edge of the I/O clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. When $\overline{CS}$ is kept low during conversion, the I/O clock must remain low for at least 44 system clock cycles to allow the conversion to complete.

B. The most significant bit (MSB) is automatically placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8–A0) clock out on the first nine I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time elapses.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	–0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O	–0.3 V to V_{CC} + 0.3 V
Peak input current (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 10 seconds, T_C: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)			–0.1	0	2.5	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}			2			V
Low-level control input voltage, V_{IL}					0.8	V
Input/output clock frequency, $f_{clock(I/O)}$			0		1.1	MHz
System clock frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		2.1	MHz
Setup time, address bits before I/O CLOCK↑, $t_{su(A)}$			400			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Operating Sequence)			3			System clock cycles
Pulse duration, $\overline{CS}$ high during conversion, $t_{wH(CS)}$ (see Operating Sequence)			44			System clock cycles
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$			210			ns
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$			190			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			404			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \le 1048$ kHz			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20	
	I/O	$f_{clock(I/O)} \le 525$ kHz			100	ns
		$f_{clock(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A	C suffix		0		70	°C
	I suffix		–40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF– voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time elapses.

4. The amount of time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 1.1$ MHz, $f_{clock(SYS)} = 2.1$ MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (terminal 16)		V_{CC} = 4.75 V, I_{OH} = 360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 3.2 mA			0.4	V
I_{OZ}	High-impedance-state output current		$V_O = V_{CC}$, $\overline{CS}$ at V_{CC}			10	µA
			V_O = 0, $\overline{CS}$ at V_{CC}			–10	
I_{IH}	High-level input current		$V_I = V_{CC}$		0.005	2.5	µA
I_{IL}	Low-level input current		V_I = 0		–0.005	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	µA
			Selected channel at 0 V, Unselected channel at V_{CC}		–0.4	–1	
$I_{CC} + I_{ref}$	Supply and reference current		$V_{ref+} = V_{CC}$, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

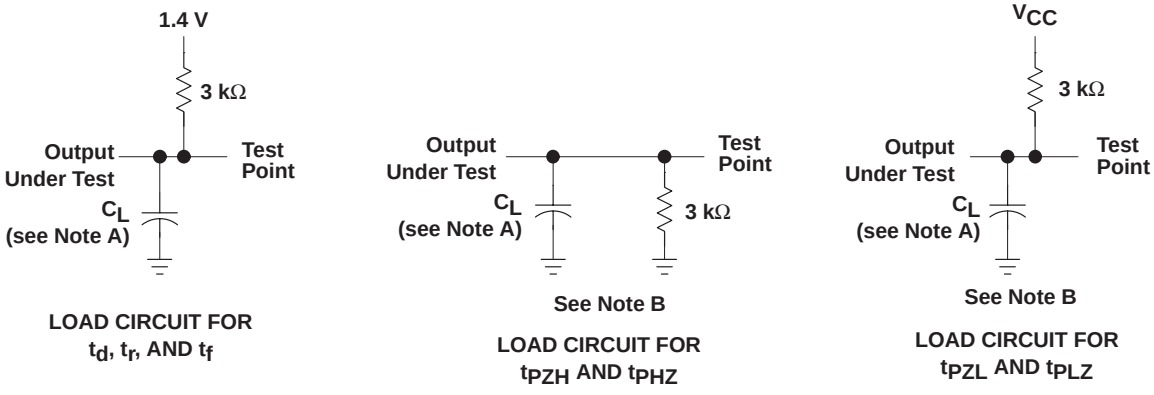
† All typical values are at V_{CC} = 5 V and T_A = 25°C.

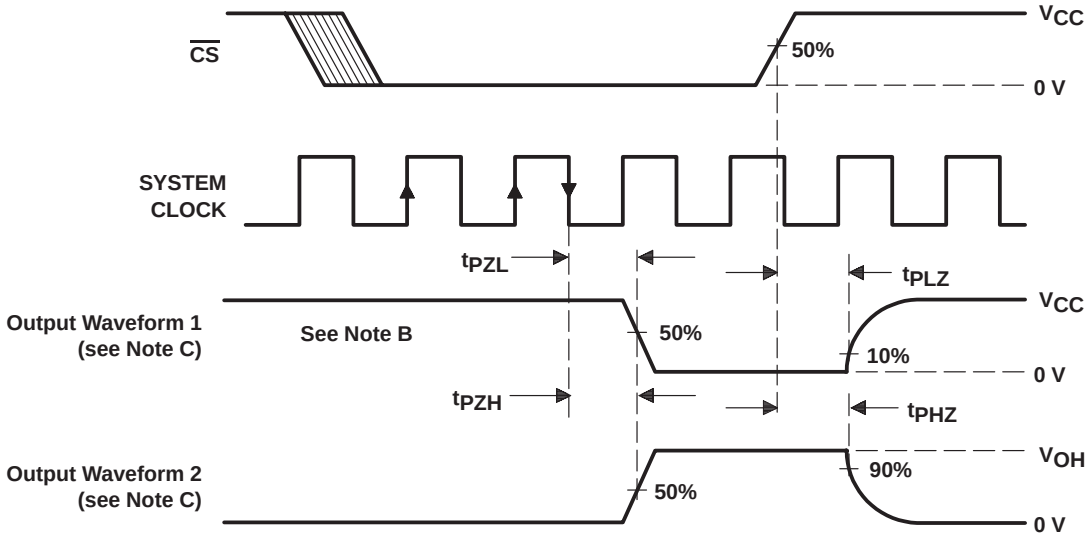
operating characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 1.1$ MHz, $f_{clock(SYS)} = 2.1$ MHz

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
E_L	Linearity error	See Note 5		±1	LSB
E_{ZS}	Zero-scale error	See Notes 2 and 6		±1	LSB
E_{FS}	Full-scale error	See Notes 2 and 6		±1	LSB
E_T	Total unadjusted error	See Note 7		±1	LSB
	Self-test output code	Input A11 address = 1011 (see Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time			21	µs
	Total access and conversion time			31	µs
	Channel acquisition time (sample cycle)	See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK↓		10		ns
t_d	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 1		400	ns
t_{en}	Output enable time			150	ns
t_{dis}	Output disable time			150	ns
$t_{r(bus)}$	Data bus rise time			300	ns
$t_{f(bus)}$	Data bus fall time			300	ns

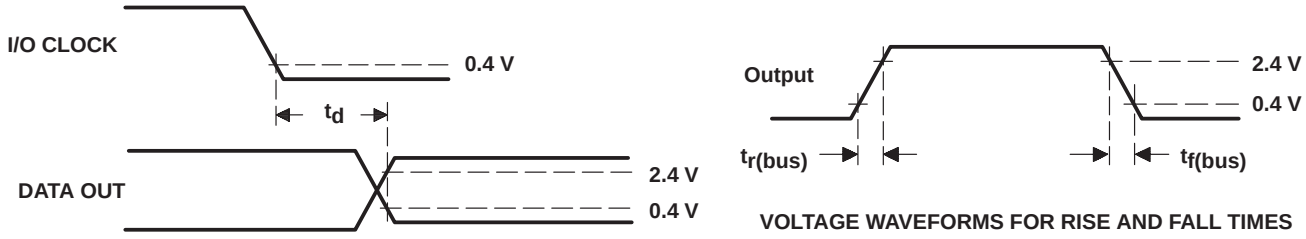
NOTES:
2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF– voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
7. Total unadjusted error includes linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and used for test purposes.

PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME

VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF
B. t_{en} = t_{PZH} or t_{PZL} and t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 2, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C \text{ (1/2 LSB)} = V_S - (V_S/2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time (t_c) gives

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

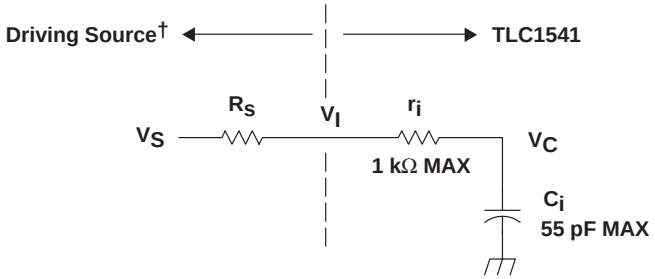
and

$$t_c \text{ (1/2 LSB)} = R_t \times C_i \times \ln(2048) \quad (4)$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_c \text{ (1/2 LSB)} = (R_S + 1\ \text{k}\Omega) \times 55\ \text{pF} \times \ln(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0 – A10
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion levels for the source must be at least equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 2. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC1541 is a complete data acquisition system on a single chip. The device includes such functions as sample and hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs: chip select ($\overline{CS}$), address input, I/O clock, and system clock. These control inputs and a TTL-compatible, 3-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1541 can complete conversions in a maximum of 21 μs, while complete input-conversion output cycles can be repeated at a maximum of 31 μs.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the SYSTEM CLOCK input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK drives the conversion-crunching circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of the $\overline{CS}$ terminal, to share a control logic point with its counterpart terminals on additional A/D devices when using additional TLC1541 devices. In this way, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low $\overline{CS}$ transition before recognizing the low transition. This technique protects the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address shifts in on the first four rising edges of I/O CLOCK. The MSB of the address shifts in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most-significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O CLOCK, and the sixth, seventh, eighth, ninth, and tenth conversion bits shift out on the negative edges of these clock cycles.
4. The final tenth-clock cycle is applied to the I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 44 system-clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. When glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, when $\overline{CS}$ goes high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 system-clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O CLOCK together in special situations in which controlling-circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. This device requires the first two clocks to recognize that $\overline{CS}$ is at a valid low level when the common clock signal is used as an I/O CLOCK. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low $\overline{CS}$ must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a $\overline{CS}$ transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the tenth valid (12 total) I/O CLOCK. Otherwise, additional common-clock cycles are recognized as I/O CLOCK cycles and shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth valid I/O CLOCK cycle, the hold function does not initiate until the negative edge of the tenth valid I/O CLOCK cycle. Thus, the control circuitry can leave the I/O CLOCK signal in its high state during the tenth valid I/O CLOCK cycle until the moment at which the analog signal must be converted. The TLC1541 continues sampling the analog input until the eighth valid falling edge of the I/O CLOCK. The control circuitry or software then immediately lowers the I/O CLOCK signal and holds the analog signal at the desired point in time and starts the conversion.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC1541CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLC1541CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLC1541CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLC1541CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLC1541CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	Request Free Samples
TLC1541CFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	Request Free Samples
TLC1541CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
TLC1541CNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
TLC1541IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLC1541IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLC1541IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLC1541IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TLC1541IFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	Request Free Samples
TLC1541IFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	Request Free Samples
TLC1541IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
TLC1541INE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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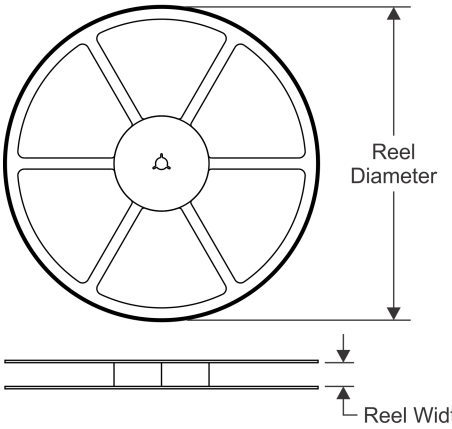
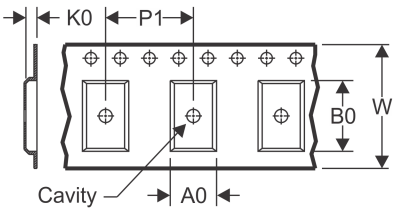
TAPE AND REEL INFORMATION

REEL DIMENSIONS

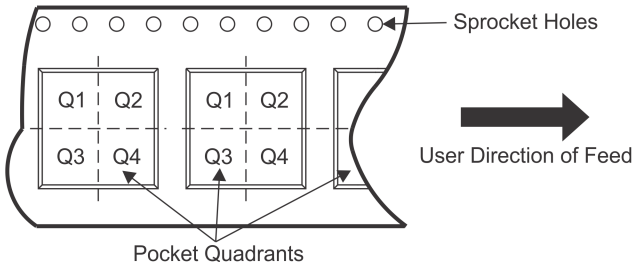


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

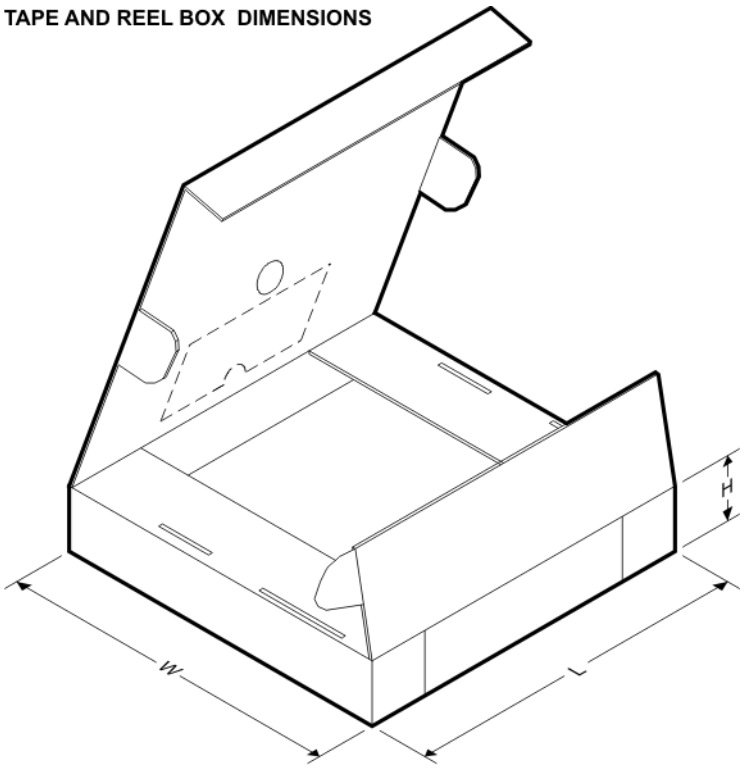
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC1541CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLC1541IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC1541CDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TLC1541IDWR	SOIC	DW	20	2000	367.0	367.0	45.0

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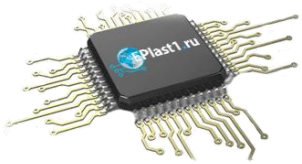

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