

# Short Form Specification

**mifare**<sup>®</sup>

**MF RC531**

ISO 14443 Reader IC

Short Form Specification

April 2005

Revision 3.2

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# ISO 14443A Reader IC

# MF RC531

## 1 INTRODUCTION

### 1.1 Scope

The MF RC531 is member of a new family of highly integrated reader ICs for contactless communication at 13.56 MHz. This reader IC family utilises an outstanding modulation and demodulation concept completely integrated for all kinds of passive contactless communication methods and protocols at 13.56 MHz. The MF RC531 is pin-compatible to the MF RC500, the MF RC530 and the SL RC400.

The Philips IC MF RC531 supports all layers of the ISO/IEC 14443A/B communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardised protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443 type B anticollision are correctly implemented. The use of this Philips IC according to ISO14443 Type B might infringe third party patent rights.

The MF RC531 supports contactless communication using MIFARE<sup>®</sup> Higher Baudrates. The internal transmitter part is able to drive an antenna designed for proximity operating distance (up to 100 mm) directly without additional active circuitry.

The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO14443 compatible transponders.

The digital part handles the complete ISO14443 framing and error detection (Parity & CRC). Additionally it supports the fast MIFARE<sup>®</sup> Classic security algorithm to authenticate MIFARE<sup>®</sup> Classic (e.g. MIFARE<sup>®</sup> Standard) products. A comfortable parallel interface, which can be directly connected to any 8-bit  $\mu$ -Processor gives high flexibility for the reader/terminal design. Additionally a SPI compatible interface is supported.

**A purchaser of this Philips IC has to take care for appropriate third party patent licenses.**

### 1.2 Features

- Highly integrated analog circuitry to demodulate and decode card response
- Buffered output drivers to connect an antenna with minimum number of external components

- Proximity operating distance (up to 100 mm)
- Supports ISO 14443
- Supports MIFARE<sup>®</sup> Dual Interface Card ICs and supports MIFARE<sup>®</sup> Classic protocol
- Supports contactless communication with higher baudrates up to 424kHz
- Crypto1 and secure non-volatile internal key memory
- Pin-compatible to the MF RC500, MF RC530 and the SL RC400
- Parallel  $\mu$ -Processor interface with internal address latch and IRQ line
- SPI compatible interface
- Flexible interrupt handling
- Automatic detection of the used  $\mu$ -Processor interface type
- Comfortable 64 byte send and receive FIFO-buffer
- Hard reset with low power function
- Power down mode per software
- Programmable timer
- Unique serial number
- Bit- and byte-oriented framing
- Internal oscillator buffer to connect 13.56 MHz quartz, optimised for low phase jitter
- 3.3 V to 5 V operation for transmitter (antenna driver) in short range and proximity applications
- 3.3 V or 5V operation for the digital part

### 1.3 Applications

The MF RC531 is tailored to fit the requirements of various applications using contactless communication based on ISO/IEC 14443 standard where cost-effectiveness, small size, high performance with a single voltage supply are important.

- Public transport terminals
- Handheld terminals
- On board units
- Contactless PC terminals
- Metering
- Contactless public phones

# ISO 14443A Reader IC

# MF RC531

## 2 BLOCK DIAGRAM

The block diagram shows the main internal parts of the MF RC531.

The parallel  $\mu$ Controller interface automatically detects the kind of 8 bit parallel interface connected to it. It includes a comfortable bi-directional FIFO buffer and a configurable interrupt output. This gives the flexibility to connect a variety of  $\mu$ C, even low cost devices, still meeting the requirements of high speed contactless transactions.

Additionally a SPI compatible interface will be supported. The MF RC531 acts as a slave during the SPI communication. The SPI clock SCK has to be generated by the master. The SPI interface includes a comfortable bi-directional FIFO buffer.

The Data processing part performs parallel serial conversion of the data. It supports framing including CRC and parity generation / checking. It

operates in full transparent mode thus supporting all layers of ISO 14443 A & B.

The status and control part allows configuration of the device to adapt to environmental influences and to adjust to operate with best performance.

For communication with MIFARE<sup>®</sup> Classic products like MIFARE<sup>®</sup> Standard or MIFARE<sup>®</sup> Light a high speed CRYPTO 1 stream cipher unit and a secure non-volatile key memory is implemented.

The analogue circuitry includes a transmitting part with a very low impedance bridge driver output. This allows an operating distance up to 100mm. The receiver is able to detect and decode even very weak responses. Due to a highly sophisticated implementation the receiver is no longer a limiting factor for the operating distance.

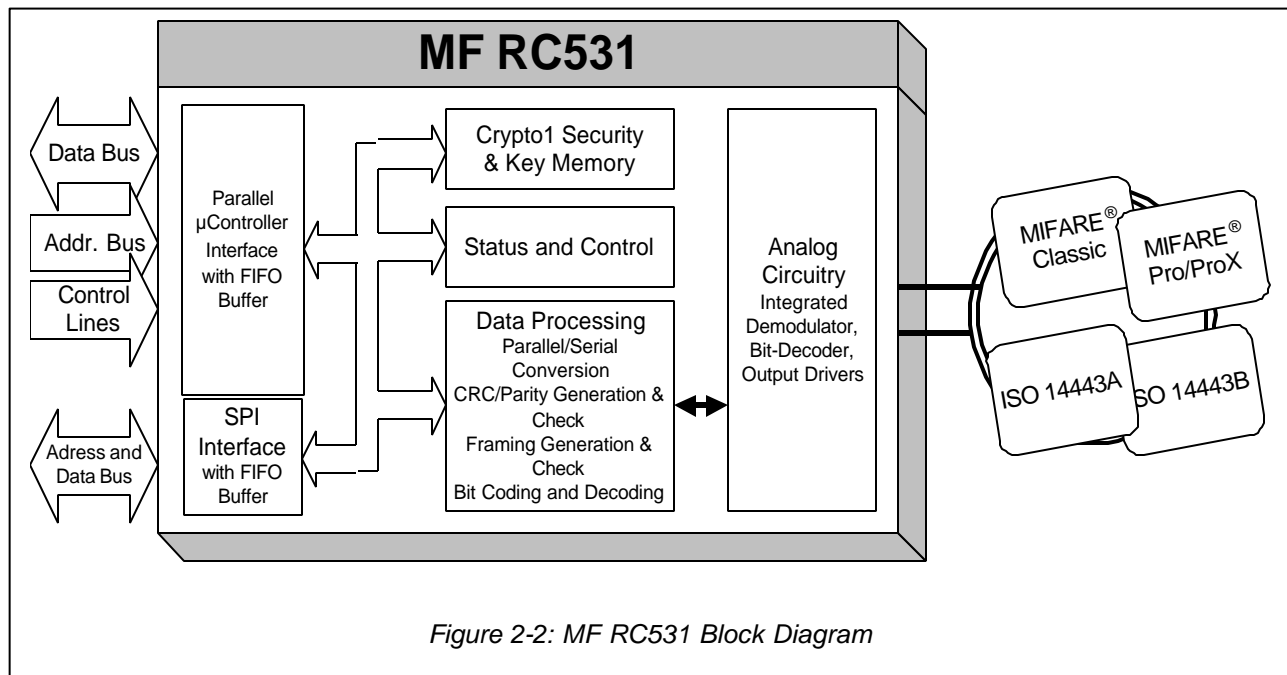


Figure 2-2: MF RC531 Block Diagram

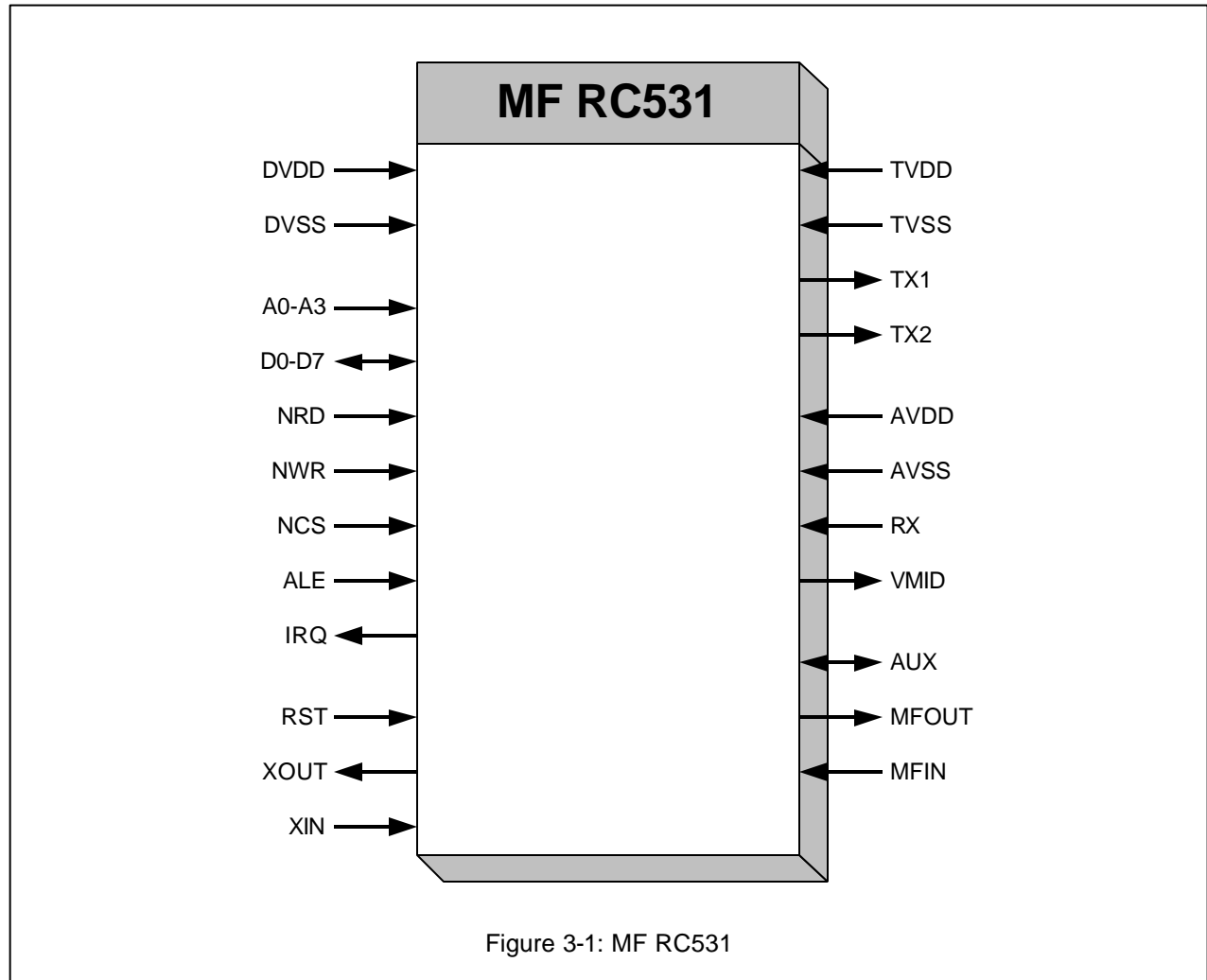
# ISO 14443A Reader IC

# MF RC531

## 3 MF RC531 PINNING

### 3.1 Pinning Diagram

The device is packaged in a 32 pin SO-package.



The device operates with 3 individual power supplies for best performance in terms of EMC behaviour and signal de-coupling. This gives outstanding RF performance and also maximum flexibility to adapt to different operating voltages of digital and analog part.

**ISO 14443A Reader IC****MF RC531****3.2 Pin Description****3.2.1 ANTENNA INTERFACE**

The contactless antenna interface basically uses four pins:

| Name     | Type       | Function             |
|----------|------------|----------------------|
| TX1, TX2 | O Buffered | Antenna Drivers      |
| VMID     | Analog     | Reference Voltage    |
| RX       | I Analog   | Antenna Input Signal |

To drive the antenna the MF RC531 provides the energy carrier of 13.56 MHz through TX1 and TX2. This signal is modulated by the transmitting data according to the register settings.

The card responds with load modulation of the RF field. The resulting signal picked up by the antenna is coupled out from the antenna matching circuit and forwarded to the RX-pin. Inside the MF RC531 the receiver senses and demodulates the signal and processes it according to the register settings. Data is passed further on to the parallel interface where it is accessible by the  $\mu$ -Controller.

The MF RC531 uses a separate power supply for the driver stage.

| Name | Type  | Function                   |
|------|-------|----------------------------|
| TVDD | Power | Transmitter Supply Voltage |
| TGND | Power | Transmitter Supply Ground  |

**3.2.2 ANALOG SUPPLY**

For best performance the MF RC531 analog part has a separate supply. It powers the oscillator, the analog demodulator and decoder circuitry.

| Name | Type  | Function                       |
|------|-------|--------------------------------|
| AVDD | Power | Analog Positive Supply Voltage |
| AGND | Power | Analog Supply Ground           |

**3.2.3 DIGITAL SUPPLY**

The MF RC531 uses a separate digital supply.

| Name | Type  | Function                        |
|------|-------|---------------------------------|
| DVDD | Power | Digital Positive Supply Voltage |
| DGND | Power | Digital Supply Ground           |

**3.2.4 AUXILLARY PIN**

Internal signals may be selected to drive this pin. It is used for design-in support and test purpose.

**ISO 14443A Reader IC****MF RC531****3.2.5 RESET PIN**

The reset pin disables internal current sources and clocks and detaches the MF RC531 virtually from the  $\mu$ C bus. If RST is released, the MF RC531 executes the power up sequence.

**3.2.6 OSCILLATOR**

| Name | Type | Function                 |
|------|------|--------------------------|
| XIN  | I    | Oscillator Buffer Input  |
| XOUT | O    | Oscillator Buffer Output |

The very fast on-chip oscillator buffer operates with a 13.56 MHz crystal connected to XIN and XOUT. If the device shall operate with an external clock it may be applied to pin XIN.

**3.2.7 MIFARE<sup>®</sup> INTERFACE**

The MF RC531 supports the active antenna concept of MIFARE<sup>®</sup>. It may handles the base-band signals NPAUSE and KOMP of MIFARE<sup>®</sup> Core Modules (MF CMxxx) at the pins MFIN and MFOUT.

| Name  | Type                   | Function                             |
|-------|------------------------|--------------------------------------|
| MFIN  | I with Schmitt Trigger | MIFARE <sup>®</sup> Interface Input  |
| MFOUT | O                      | MIFARE <sup>®</sup> Interface Output |

The MIFARE<sup>®</sup> interface may be used to communicate with either the analog or the digital part of the MF RC531 separately in the following ways:

- The analog circuit may be used stand-alone via the MIFARE<sup>®</sup> interface. In that case MFIN will be connected to the externally generated NPAUSE signal. The MFOUT pin provides the KOMP signal.
- The digital circuit may be used to drive an external analog circuit via the MIFARE<sup>®</sup> interface. In that case the MFOUT pin provides the internally generated NPAUSE signal and MFIN will be connected to the KOMP signal from the outside.

**3.2.8 PARALLEL INTERFACE**

16 pins control the parallel interface:

| Name      | Type                     | Function                   |
|-----------|--------------------------|----------------------------|
| D0 ... D7 | I/O with Schmitt Trigger | Bi-directional Data Bus    |
| A0 ... A2 | I/O with Schmitt Trigger | Address Lines              |
| NWR / RNW | I/O with Schmitt Trigger | Not Write / Read Not Write |
| NRD / NDS | I/O with Schmitt Trigger | Not Read / Not Data Strobe |
| NCS       | I/O with Schmitt Trigger | Not Chip Select            |
| ALE       | I/O with Schmitt Trigger | Address Latch Enable       |
| IRQ       | O                        | Interrupt Request          |

**ISO 14443A Reader IC****MF RC531****3.2.9 SPI COMPATIBLE INTERFACE**

4 pins control the SPI compatible interface.

| Name | Type                     | Function                                 |
|------|--------------------------|--|
| A0   | I/O with Schmitt Trigger | MOSI, master to slave communication      |
| A2   | I/O with Schmitt Trigger | SCK, clock to be generated by the master |
| D0   | I/O with Schmitt Trigger | MISO, slave to master communication      |
| ALE  | I/O with Schmitt Trigger | NSS, enables the SPI communication       |

**3.3 Applications****3.3.1 CONNECTING DIFFERENT  $\mu$ CONTROLLER'S**

The MF RC531 supports different parallel  $\mu$ C interfaces and a SPI compatible interface. An intelligent auto-detection logic automatically adapts the parallel interface to the respective bus system. Selection of the device is performed with signal NCS.

To connect  $\mu$ -Controllers using separated address and data bus pin ALE has to be connected to DVDD.

To connect  $\mu$ -Controllers using multiplexed address and data bus pin ALE has to be connected to the signal ALE of the  $\mu$ -Controller

To connect  $\mu$ -Controllers using RNW and NDS (instead of NWR and NRD) the  $\mu$ -Controller's RNW has to be connected to pin NWR and NDS to pin NRD.



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## 3.3.2 APPLICATION EXAMPLE

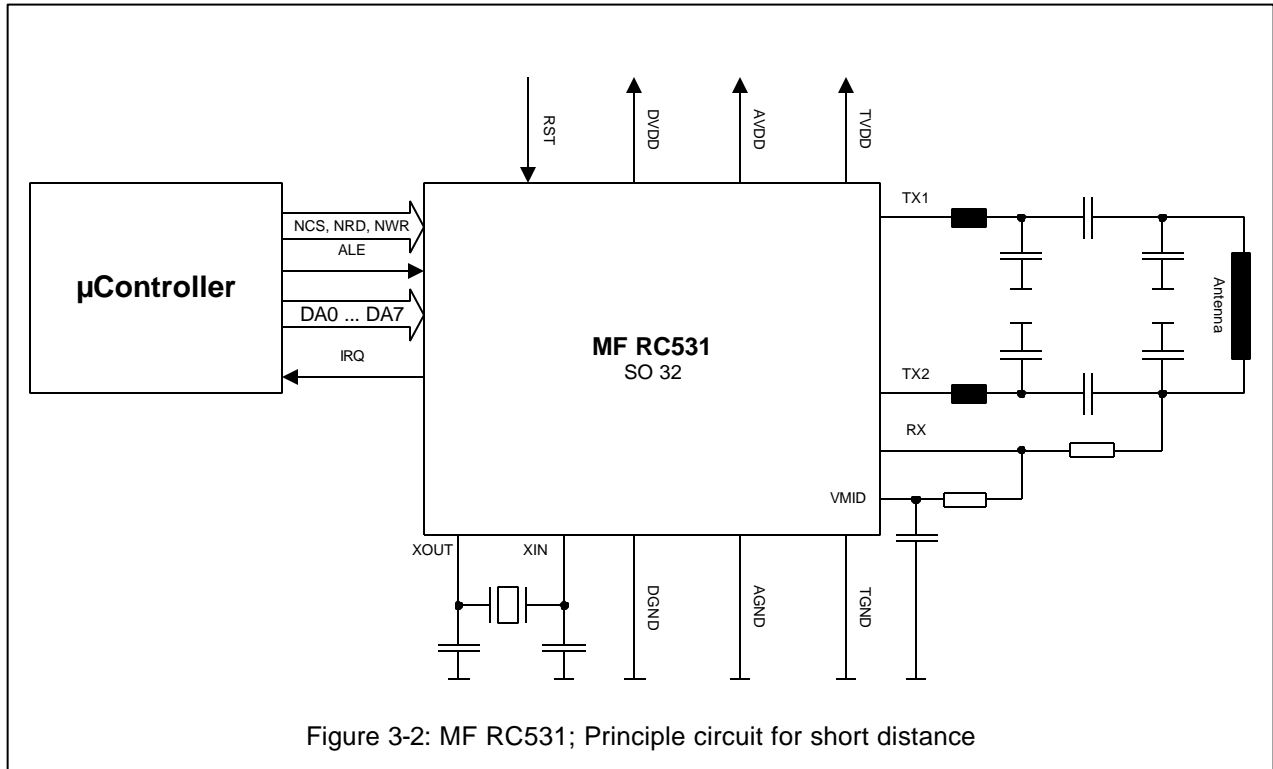


Figure 3-2: MF RC531; Principle circuit for short distance

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**ISO 14443A Reader IC****MF RC531**

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**4 MIFARE<sup>®</sup> CLASSIC RELATED ITEMS****4.1 CRYPTO I: Card Authentication**

For correct authentication of MIFARE<sup>®</sup> Classic products the fast CRYPTO 1 stream cipher is available. The corresponding keys have to be programmed into the secure non-volatile key memory of the MF RC531.

Only two commands need to be sent by application software to turn on CRYPTO 1 secured communication.

**4.1.1 INITIATING CARD AUTHENTICATION**

The correct key for the authentication has to be selected from the secure internal non-volatile key memory and loaded into the internal CRYPTO1 register. Next the authentication command is transmitted to the card.

After receiving the first message token from the card, the  $\mu$ -Controller has to check the

communication status flags. If communication so far has been successful the second part of the authentication procedure can be started.

**4.1.2 SECOND PART OF CARD AUTHENTICATION**

Data to be transmitted to the card in this phase are generated automatically by the internal CRYPTO 1 unit inside the MF RC531. To request this action the according command has to be triggered.

The card will respond with the second message token. Then the communication status flags have to be checked by the  $\mu$ -Controller. If authentication has been successful further communication with a MIFARE<sup>®</sup> Classic card continues CRYPTO 1 enciphered.

**ISO 14443A Reader IC****MF RC531****5 ELECTRICAL SPECIFICATION****5.1 DC Characteristics**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

## Voltage Supply

|      |                            |  |     |     |     |   |
|------|----------------------------|--|-----|-----|-----|---|
| DVDD | Digital Supply Voltage     |  | 4.5 | 5.0 | 5.5 | V |
|      |                            |  | 3.0 | 3.3 | 3.6 |   |
| AVDD | Analog Supply Voltage      |  | 4.5 | 5.0 | 5.5 | V |
| TVDD | Transmitter Supply Voltage |  | 3.3 | 5.0 | 5.5 | V |

## Current Consumption

|                   |  |                              |  |    |    |    |
|-------------------|--|------------------------------|--|----|----|----|
| I <sub>DVDD</sub> | Operating Digital Supply Current                 | Idle Command                 |  | 6  |    | mA |
| I <sub>AVDD</sub> | Operating Analog Supply Current                  | Idle Command,<br>Receiver On |  | 25 |    | mA |
| I <sub>TVDD</sub> | Operating Buffered Antenna Driver Supply Current | continuous wave              |  |    | 50 | mA |

**5.2 Start up Characteristics**

| Mode | CONDITIONS | Current | UNIT | Time | UNIT |
|------|------------|---------|------|------|------|
|------|------------|---------|------|------|------|

## Startup times and current consumption

|                                 |  |   |    |        |    |
|---------------------------------|--|---|----|--------|----|
| Power on                        |  | - | -  | < 1000 | μs |
| Hard Reset via Reset Pin        |  | 1 | μA | < 1000 | μs |
| Soft Reset via Register Setting |  | 1 | μA | < 1000 | μs |

**ISO 14443A Reader IC****MF RC531****6 REVISION HISTORY**

| REVISION | DATE         | CPCN | PAGE    | DESCRIPTION   |
|----------|--------------|------|---------|---|
| 3.2      | April 2005   |      | 3<br>12 | Update chapter 1.1 with 14443B patent infringement warning<br>Insert Revision History |
| 2.0      | June 2002    | -    |         | published version   |
| 1.0      | January 2002 | -    |         | internal version  |

*Table 0-1: Document Revision History*

## Definitions

|  |   |
|--|---|
| <b>Data sheet status</b>   |   |
| Objective specification  | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification  | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification  | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>   |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>   |   |
| Where application information is given, it is advisory and does not form part of the specification.  |   |

## Life support applications

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## **Contact Information**

For additional information please visit **<http://www.semiconductors.philips.com>**. Fax: **+31 40 27 24825**  
For sales offices addresses send e-mail to: **[sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)**.

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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.