UM10868

PCAL6524 demonstration board OM13526

Rev. 1 — 23 September 2015 **User manual**

Document information

Info	Content
Keywords	OM13320 Fm+ development kit, OM13260 Fm+ I2C bus development board, OM13303 GPIO target board
Abstract	Installation guide and User Manual for the OM13526 24-bit GPIO Daughter Card that connects to OM13260 Fm+ I2C bus development board. This daughter board makes it easy to test and design with the PCAL6524, an ultra low-voltage translating 24-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Fast-mode Plus (Fm+) I2C-bus interface. This daughter board, along with the Fm+ Development board, provides an easy to use evaluation platform.

Revision history

Rev	Date	Description
1	20150923	Initial version.

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

The PCAL6524 24-bit GPIO evaluation board allow bidirectional voltage-level translation and GPIO expansion between 0.8 V to 3.6 V on SCL/SDA and 1.8 V, 2.5 V, 3.3 V, 5.5 V on I/O Ports with active low reset input control and open-drain active low interrupt output indicator (red LED) plus one hardware address input setting to select one of four different slave address. A graphical interface allows the user to easily explore the different functions of the I/O expander.

The IC communicates to the host via the industry standard I^{2}C-bus/SMBus port. The evaluation software runs under Microsoft Windows PC platform.

2. Features of the OM13526 24-bit GPIO daughter board

- Direct connection to OM13260 Fm+ I^{2}C-bus Development board
- Easy to use GUI based software demonstrates the capabilities of the PCAL6524
- Jumper configuration for most features of PCAL6524
- Flexible power supply configuration: 3.3 V, 5 V or external supply
- Direct connection to OM13303 GPIO Target board for I/O visualization
- Convenient test points for easy scope measurements and signal access
- Jumper configuration of device I^{2}C address
- LED indicators for power and /INT
- No external power supply required and obtains +5 V power from PC USB port

3. Hardware description

3.1 Power supply jumpers

The power supply selection for the OM13526 is very flexible and allows for detailed analysis and evaluation of 24-bit GPIO device. J13 selects +5V_PWR supply from either the tester connector CN1 (pins 4 and 6, +5V_TSTR) or the Fm+ board connector CN2 (pins 7 and 12, +5V). J1 selects VDDP (U1 pin 27) supply from either +5V_PWR or +3V3 (CN2 pins 8 and 11) and J9 selects VDDI (U1 pin 31) supply from either +3V3 (CN2 pins 8 and 11) or +5V_PWR. If external power operation is desired from TP5 (VDDP-IN) and TP6 (VDDI), no jumper is required on J1 and J9. The D2 green LED is lit when VDDP is available.

3.2 SCL and SDA jumpers

The I^{2}C -bus signals SDA and SCL supplied to the device under test can be sourced from either the Fm+ board via CN2 or the tester via CN1. Jumpers J12 and J14 select the I^{2}C bus 1 or bus 2 signals from the Fm+ board, shorting pins 1 to 2 to select I^{2}C bus 1 while shorting pins 2 to 3 to select I^{2}C bus 2.

3.3 Device reset, interrupt and address pin selection

- **Reset** (U1, pin28), the device is resetting when shorting pin 1 to 2 on jumper J5
- **Interrupt** (U1, pin 32), open-drain interrupt (/INT) output is activated and D1 red LED is lit when any input state differs from its corresponding Input Port register state, TP1 can be used to monitor the /INT pin 32.

- **Address input** (U1, pin 26), jumper J10 is used to select device address as shorting pins 1 to 2 (VDD, address is 46h), shorting pins 3 to 4 (VSS, address is 44h), shorting pins 5 to 6 (SDA, address is 42h), shorting pins 7 to 8 (SCL, address is 40h).

3.4 Board layout viewer

Fig 1 shows all jumper locations and labels on PCB.

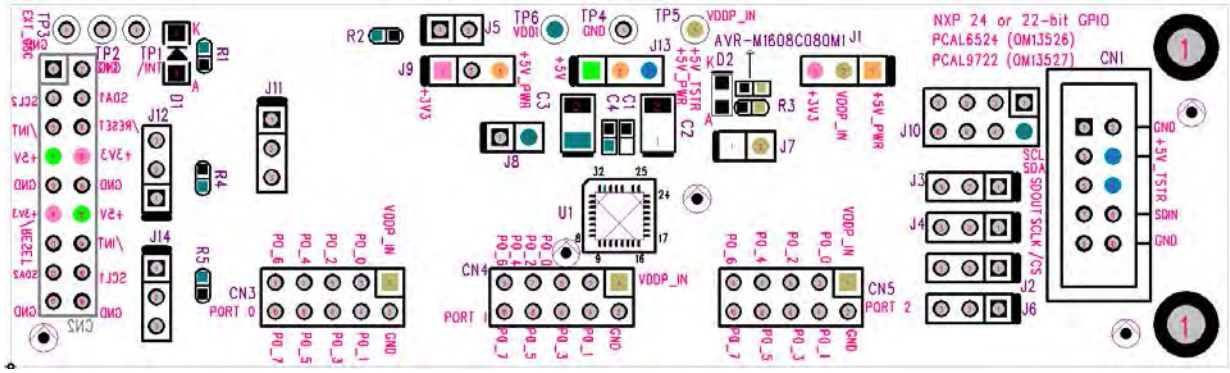


Fig 1. PCAL6524 demo board layout and Labels

3.5 Connector pinouts

- **CN1** (10-pin male tester connector) is connected to master which is driving either I^2C-bus for PCAL6524 or SPI-bus for PCAL9722. This is easily achieved with third party development tools from Total Phase (http://www.totalphase.com). There are two tools called Aardvark and Beagle that direct connect to this board through CN1.

Table 1. CN1 10-pin tester connector

CN1 Pin #	Function	Board connection
1	SCL	U1 pin 29 (PCAL6524)
2,10	GND	Ground
3	SDA	U1 pin 30 (PCAL6524)
4, 6	+5V_TSTR	J13 pin 3
5	SDOUT (MISO)	U1 pin 24 (PCAL9722)
7	SCLK	U1 pin 29 (PCAL9722)
8	SDIN (MOSI)	U1 pin 30 (PCAL9722)
9	/CS (SS)	U1 pin 23 (PCAL9722)

Note: Since SDA and SCL are both connected to the device (U1) under test, the Aardvark and the Fm+ Development board cannot be used simultaneously. The Beagle, a bus sniffer, does not have any issues.

- **CN2** (18-pin female connector) can connect directly to the OM13260 Fm+ Development board. This connector provides power, I^2C signals and other ancillary signals.

Table 2. CN2 18-pin Fm+ board connector

CN2 Pin #	Function	Board connection
1, 2, 9, 10, 17, 18	GND	Ground
3	SCL2	SCL Bus 2 to J12 pin 3
4	SDA1	SDA Bus 1 to J14 pin 1
5, 14	/INT	Interrupt to U1 pin 32, LED (D1) and TP1 (test point 1)
6, 13	RESET	U1 pin 28 and J5 pin 1
7, 12	+5V	J13 pin 1
8, 11	+3V3	J1 pin 3 and J9 pin 1
15	SDA2	SDA Bus 2 to J14 pin 3
16	SCL1	SCL Bus 1 to J12 pin 1

Note: The connector on the Fm+ board is a male, shrouded 14 pin type, while the connector on this 24-bit GPIO board is an 18-pin female. The reason lies with the shroud around the 14 pin connector. To ensure correct mating of the female with the male, two pin positions on both of the female sides are grounded.

- **CN3, CN4, CN5** (10-pin male connector) is connected to GPIO target board (OM13303) which consists of eight LEDs and eight switches and connects directly to this 24-bit GPIO board through CN3 (I/O of port 0), CN4 (I/O of port 1), CN5 (I/O of port2). These switches and LEDs on GPIO target board permit easy exercise of the I/O functionality of the device under test. The LEDs light red when the voltage on that channel is below VDDP x 0.3V and LEDs light green when the voltage is above VDDP x 0.7V. The LEDs remain off when the voltage is between those two levels.

Table 3. CN3, CN4, CN5 10-pin GPIO target board connector

CN[3:5] pin #	Function	Board connection
1	VDDP_IN	J1 pin 2 and TP5 (test point 5) and by J7 to VDDP (U1 pin 27)
2	GND	Ground
3	P[0:2]_0 (I/O 0)	U1 pin 1 (by J11), pin 9, pin 17
4	P[0:2]_1 (I/O 1)	U1 pin 2, pin 10, pin 18
5	P[0:2]_2 (I/O 2)	U1 pin 3, pin 11, pin 19
6	P[0:2]_3 (I/O 3)	U1 pin 4, pin 12, pin 20
7	P[0:2]_4 (I/O 4)	U1 pin 5, pin 13, pin 21
8	P[0:2]_5 (I/O 5)	U1 pin 6, pin 14, pin 22
9	P[0:2]_6 (I/O 6)	U1 pin 7, pin 15, pin 23 (by J6)
10	P[0:2]_7 (I/O 7)	U1 pin 8, pin 16, pin 24 (by J3)

Please note that CN4 and CN5 pins are incorrectly labeled. The labels show that both CN4 and CN5 pins are P0_[0:7], the correct labels are P1_[0:7] for CN4 and P2_[0:7] for CN5. The schematic is correct, only the labels are incorrect.

3.6 All jumpers default setting and test points

Fig 2 shows the PCAL6524 demo board.

- TP1 (/INT) is connected to interrupt output (U1 pin 32) for probing use.

- TP2 and TP4 are GND test points for probing use.
- TP3 (EXT_OSC) is external clock input to P0_0 (pin1) for debouncer circuit use
- TP5 (VDDP_IN) and TP6 (VDDI) are connected to external power inputs.
- All jumpers default settings and functions are shown in Table 4.

Table 4. All jumpers setting for test and evaluation

Jumper	Default setting	Comment
J1 (3-pin)	1-2 (VDDP_IN = +5V_PWR)	This jumper is used to select VDDP for U1 device (pin 27) 1-2: select +5V_PWR 2-3: select +3V3
J2 (3-pin)	2-3 (SCL)	This jumper is used to select clock either SCL (I^2C) or SCLK (SPI) for U1 device (pin 29) 1-2: select SCLK for SPI device 2-3: select SCL for I^2C device
J3 (3-pin)	2-3 (P2_7)	This jumper is used to select function either P2_7 (I^2C) or SDOUT (SPI) for U1 device (pin 24) 1-2: select SDOUT for SPI device 2-3: select P2_7 for I^2C device
J4 (3-pin)	2-3 (SDA)	This jumper is used to select data either SDA (I^2C) or SDIN (SPI) for U1 device (pin 30) 1-2: select SDIN for SPI device 2-3: select SDA for I^2C device
J5 (2-pin)	Open	Short: force /RESET (U1 pin 28) to GND Open: 10K pull-up /RESET (U1 pin 28) to VDDI
J6 (3-pin)	2-3 (P2_6)	This jumper is used to select function either P2_6 (I^2C) or /CS (SPI) for U1 device (pin 23) 1-2: select /CS for SPI device 2-3: select P2_6 for I^2C device
J7 (2-pin)	Short	Short: connect VDDP_IN to U1 device (pin 27) Open: connect current meter to measure the I_{DDP} on U1 device
J8 (2-pin)	Short	Short: connect VDDI to U1 device (pin 31) Open: connect current meter to measure the I_{DDI} on U1 device
J9 (3-pin)	1-2 (VDDI = +3V3)	This jumper is used to select VDDI for U1 device (pin 31) 1-2: select +3V3 (from Fm+ development board) 2-3: select +5V_PWR
J10 (4x2-pin)	1-2 (VDDI)[1]	This 4x2 jumper is used to select input value for ADDR (U1 pin 26) 1-2: select VDDI (address is 0x46 for PCAL6524; address is 0x42 for PCAL9722) 3-4: select VSS (address is 0x44 for PCAL6524; address is 0x40 for PCAL9722) 5-6: select SDA (address is 0x42 for PCAL6524; none for PCAL9722) 7-8: select SCL (address is 0x40 for PCAL6524; none for PCAL9722)
J11 (3-pin)	2-3 (P0_0)	This jumper is used to select function either P0_0 or EXT_OSC for U1 device (pin 1) 1-2: select external oscillator (EXT_OSC) input for debounce circuit use 2-3: select P0_0 input as normal operation

Jumper	Default setting	Comment
J12 (3-pin)	1-2 (SCL = SCL1)	This jumper is used to select SCL source for U1 device (pin 29) 1-2: select SCL1 (bus 1 from Fm+ development board) 2-3: select SCL2 (bus 2 from Fm+ development board)
J13 (3-pin)	1-2 (+5V = +5V_PWR)	This jumper is used to select +5V source 1-2: select +5V from Fm+ development board 2-3: select +5V_TSTR from tester (beagle) board
J14 (3-pin)	1-2 (SDA = SDA1)	This jumper is used to select SDA source for U1 device (pin 30) 1-2: select SDA1 (bus 1 from Fm+ development board) 2-3: select SDA2 (bus 2 from Fm+ development board)
[1] Default PCAL6524 slave address is set to 0x46		

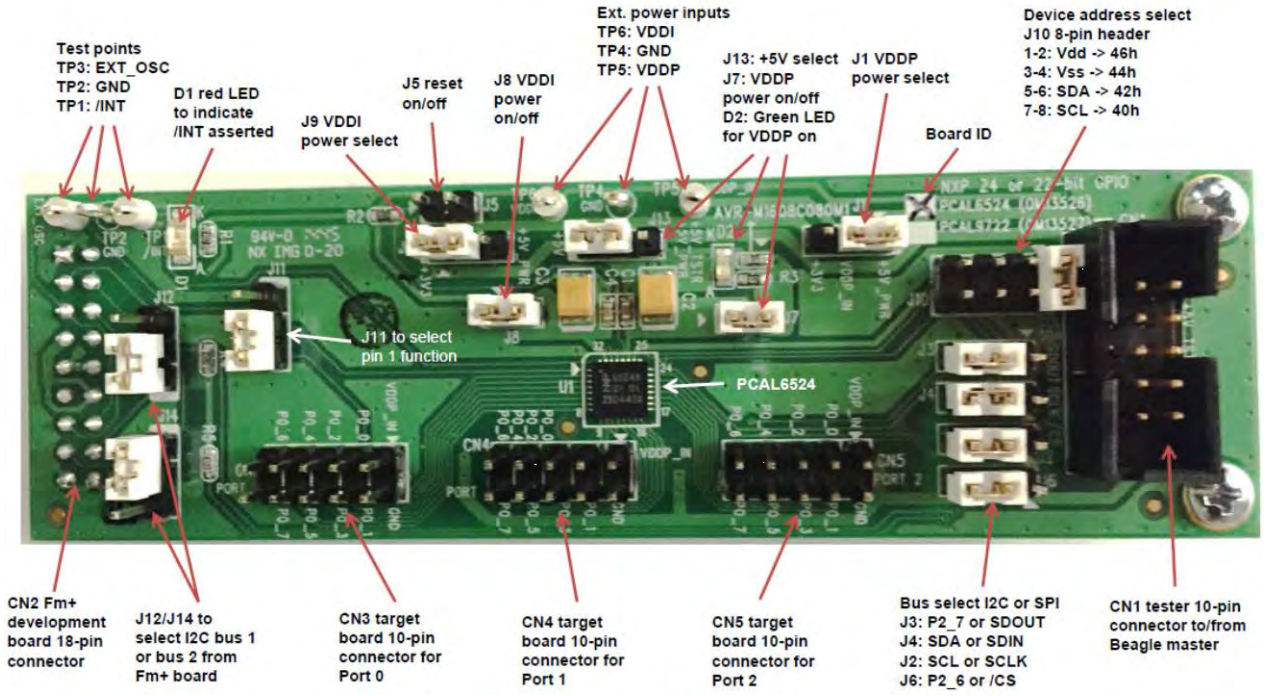


Fig 2. PCAL6524 demo board (OM13526)

4. Schematic

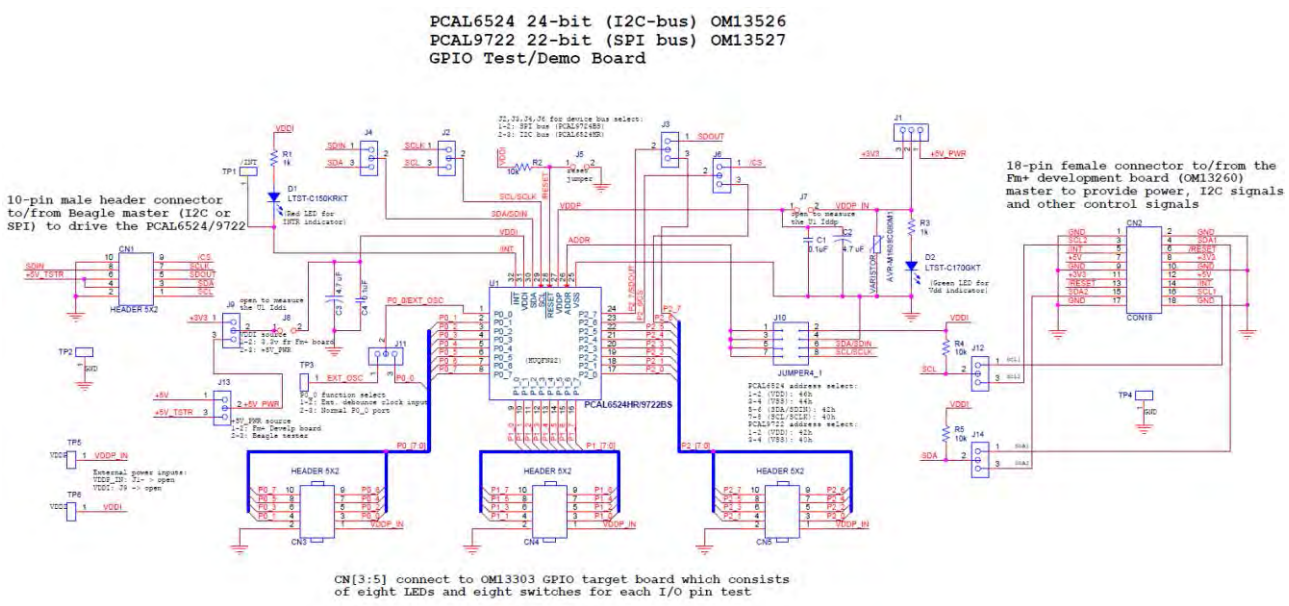


Fig 3. PCAL6524 demo board schematic

5. Installation

5.1 PCAL6524 demo board, Fm+ development board, GPIO target board

The OM13526 PCAL6524 24-bit GPIO demo board is a daughter card to the OM13260 Fm+ I2C bus development board which is part of the Fm+ development board kit (OM13320) and three I/O ports (8-bit × 3) on PCAL6524 are connected to GPIO target board for I/O visualization. You may download the software, user manual, and find ordering information at the NXP web site:

http://www.nxp.com/demoboard/OM13320.html#documentation

5.2 OM13526 connection to Fm+ I²C bus development board

The OM13260 Fm+ I2C bus development board should be disconnected from your PC before mounting the OM13526 board with GPIO target board on to it. The OM13526 board has an 18-pin female connector (CN2) that connects to CN4 14-pin male connector on the Fm+ development board (OM13260) as shown in Fig 4. Three GPIO Target boards (OM13303) through ribbon cables connect to 10-pin male connectors (CN3, CN4, CN5) on OM13526 PCAL6524 24-bit GPIO demo board for 8-bit I/O port 0, port1 and port2.

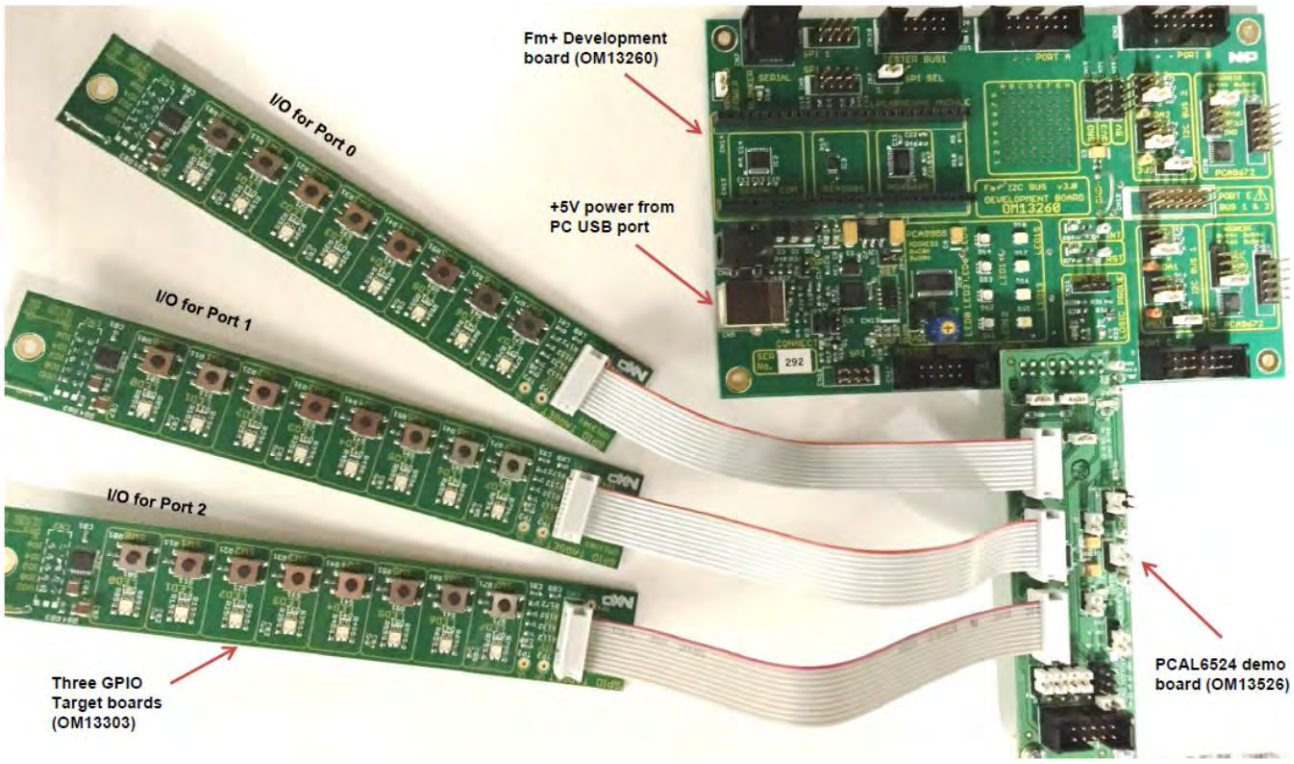


Fig 4. PCAL6524 demo board (OM13526) mounting to the Fm+ development board (OM13260) and connecting to three GPIO target boards (OM13303)

6. PCAL6524 evaluation steps with Fm+ development board

The PCAL6524 is controlled by Fm+ development board GUI in Expert mode as shown in Fig 5.

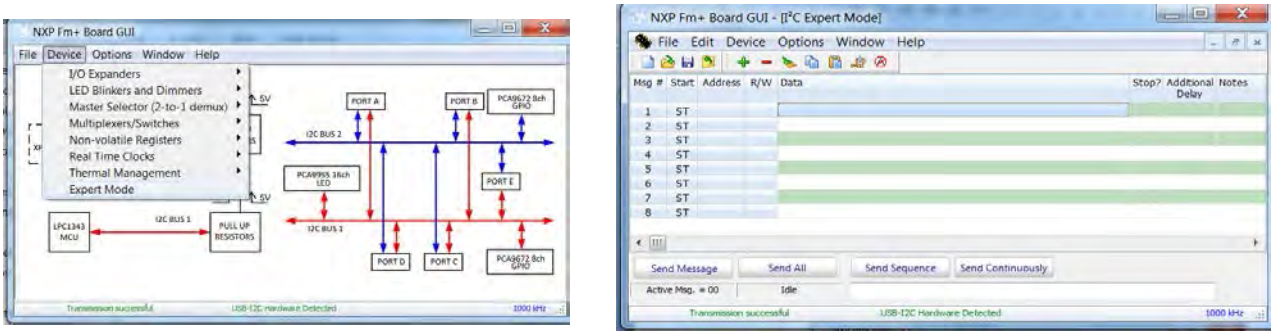


Fig 5. Select the Expert Mode from Fm+ development board GUI

Connect the hardware as described in Section 5.2. All jumpers are in default setting and device address is set to 0x46h on J10 (set ADDR = VDDI) for PCAL6524 demo board.

When you have correctly installed the software and the demonstration board hardware is connected and recognized by the computer, start the Fm+ development board software. As shown in the Fig 5, when the demonstration board hardware is correctly connected to the USB port and the computer recognizes it, the message “USB-I2C Hardware Detected” is displayed on the bottom of the window.

6.1 PCAL6524 output shifting pattern demo for all three ports

1. From the ‘Device’ drop-down menus select ‘Expert Mode’ as shown in Fig 5.
2. Copy the “output shifting pattern on all three ports” text file as shown below. From the ‘File’ drop-down menus select ‘Open’, and from the “open data file” window to select the “output shifting pattern on all three ports” text file.

   ==========

   Expert Mode Data File

   46,Write,Yes,200,0C,00,00,00,Comments: set all GPIOs as output ports

   46,Write,Yes,200,04,FF,FF,FF,Comments: write registers 04,05,06 to set all output ports to 1s

   46,Write,Yes,200,04,FE,FE,FE,Comments: set bit0 to 0 in all three ports

   46,Write,Yes,200,04,FD,FD,FD,Comments: set bit1 to 0 in all three ports

   46,Write,Yes,200,04,FB,FB,FB,Comments: set bit2 to 0 in all three ports

   46,Write,Yes,200,04,F7,F7,F7,Comments: set bit3 to 0 in all three ports

   46,Write,Yes,200,04,EF,EF,EF,Comments: set bit4 to 0 in all three ports

   46,Write,Yes,200,04,DF,DF,DF,Comments: set bit5 to 0 in all three ports

   46,Write,Yes,200,04,BF,BF,BF,Comments: set bit6 to 0 in all three ports

   46,Write,Yes,200,04,7F,7F,7F,Comments: set bit7 to 0 in all three ports

   Sequence:01,02,03,04,05,06,07,08,09,10

   ==========
3. After opening the “output shifting pattern on all three ports” text file, the “NXP Fm+ Board GUI” in Expert mode screen will be displayed as shown in Fig 6.
4. Click the ‘Send All’ button, all the valid messages on the screen will be sent in the order of the row number (Msg #). The action will be performed one time.

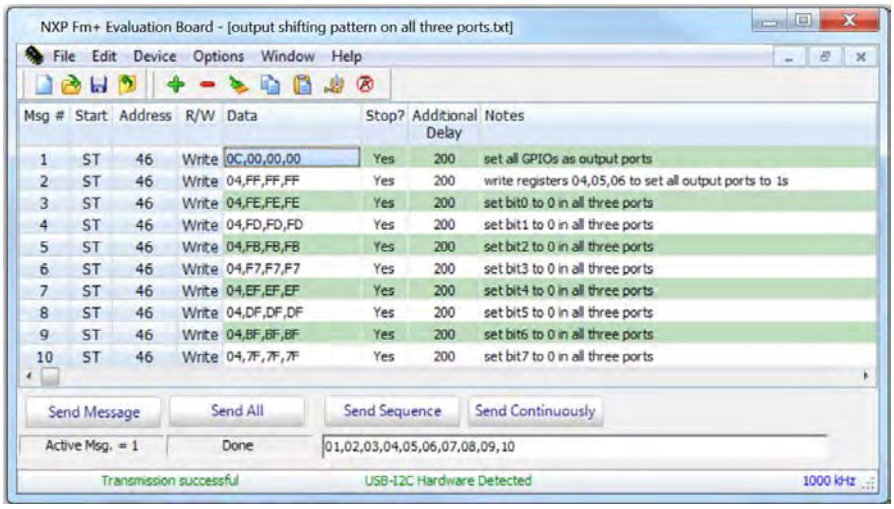


Fig 6. Message data in Expert mode to demo “output shifting pattern on all ports”

6.2 PCAL6524 registers are controlled by Fm+ board GUI

1. Select 24-bit PCAL6524 from I/O Expanders as shown in Fig 7.

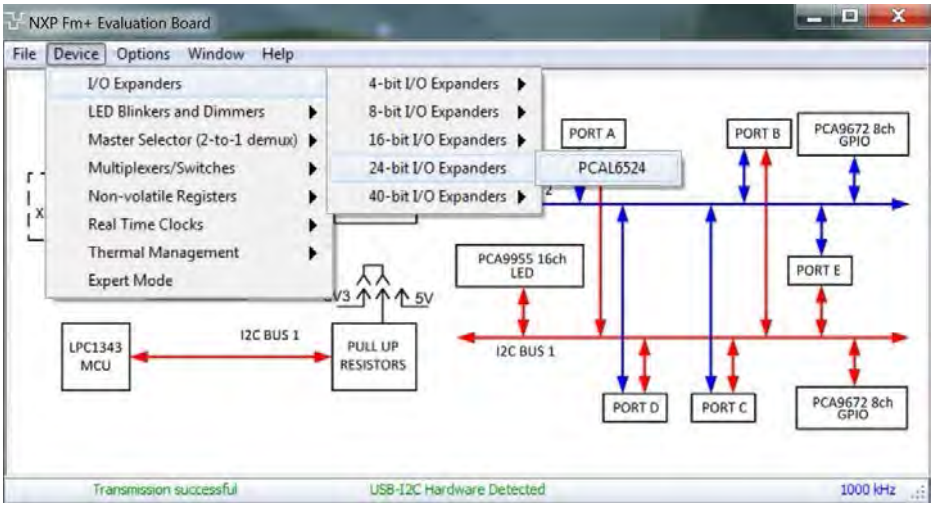


Fig 7. Device selection screen for PCAL6524

2. First group registers read or write are shown in Fig 8.

Fig 8. Device configuration screen for registers 00-02, 58-5A, 68-6E hex

3. Second group registers read or write are shown in Fig 9.

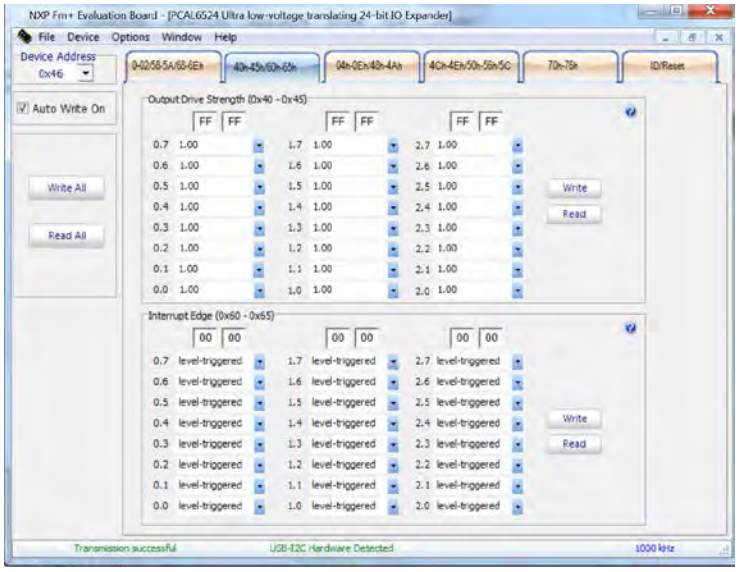


Fig 9. Device configuration screen for registers 40-45, 60-65 hex

4. Third group registers read or write are shown in Fig 10.

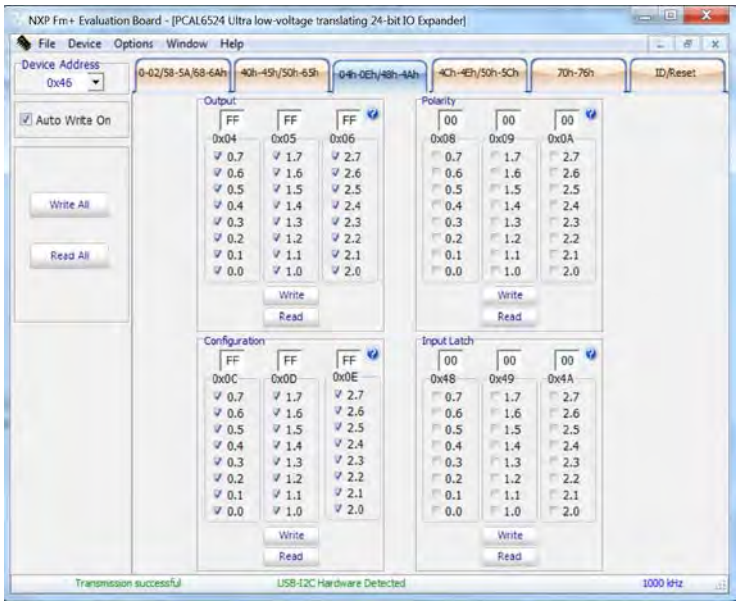


Fig 10. Device configuration screen for registers 04-0E, 48-4A hex

5. Fourth group registers read or write are shown in Fig 11.

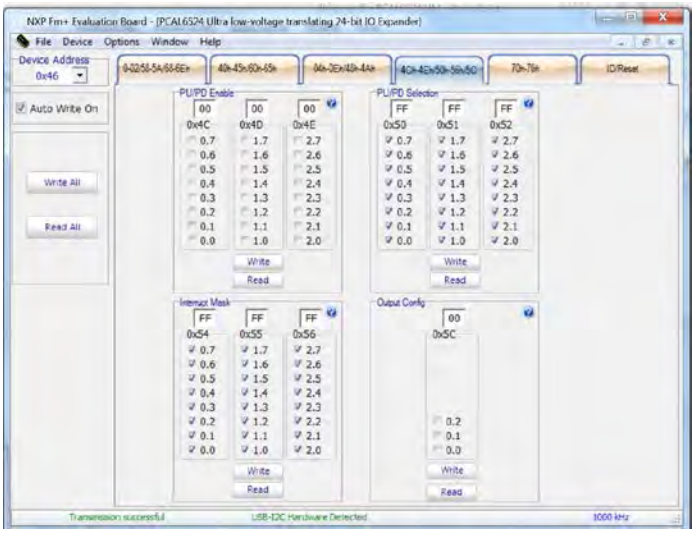


Fig 11. Device configuration screen for registers 4C-4E, 50-56, 5C hex

6. Fifth group registers read or write are shown in Fig 12.

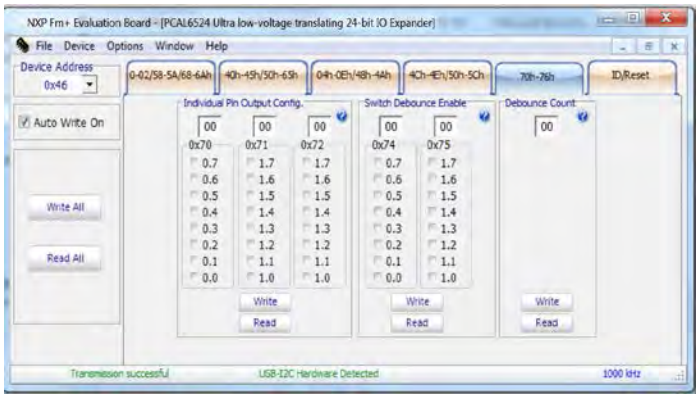


Fig 12. Device configuration screen for registers 70-76 hex

7. Sixth group registers read or write are shown in Fig 13.

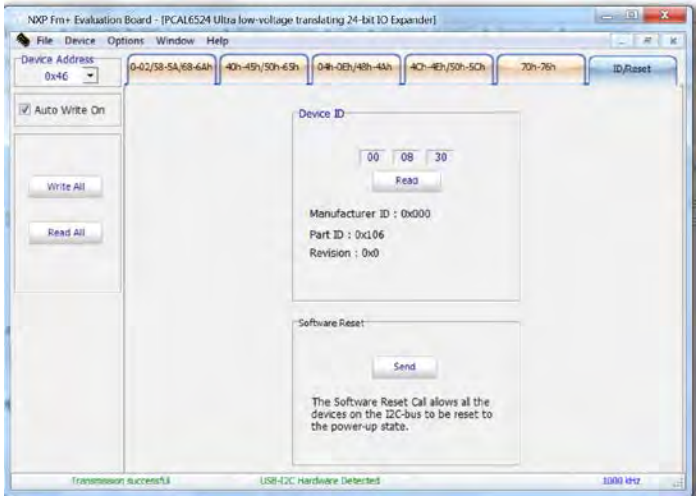


Fig 13. Device configuration screen for Device ID and Reset

7. Support

For support, please send an E-mail to: i2c.support@nxp.com

8. Abbreviations

Table 5. Abbreviations

Acronym	Description
ESD	Electro Static Discharge
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
I^2C-bus	Inter-integrated Circuit bus
LED	Light Emitting Diode
PC	Personal Computer
PCB	Printed-Circuit Board
SMBus	System Management Bus
USB	Universal Serial Bus

9. References

[1] PCAL6524, Ultra low-voltage translating 24-bit Fm+ I^2C-bus/SMBus I/O expander; Product data sheet; NXP Semiconductors

[2] UM10741, Fm+ Development Kit OM13320 User manual; NXP Semiconductors

10. Legal information

10.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

10.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

I²C-bus — logo is a trademark of NXP Semiconductors N.V.

11. List of figures

12. List of tables

13. Contents

For more information, please visit: http://www.nxp.com

Date of release: 23 September 2015

Document identifier: UM10868

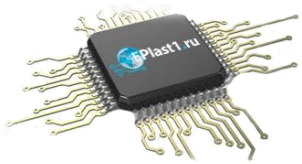
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.