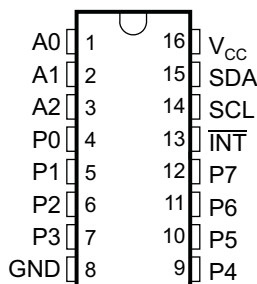


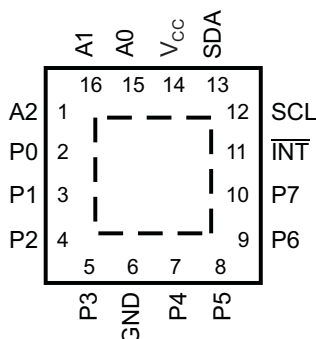
## FEATURES

- Low Standby Current Consumption of 1  $\mu$ A Max
- I<sup>2</sup>C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I<sup>2</sup>C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I<sup>2</sup>C/SMBus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Power-Up With All Channels Configured as Inputs
- No Glitch on Power-Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

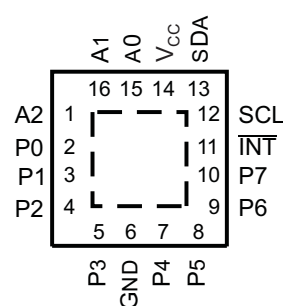
DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



RGV PACKAGE  
(TOP VIEW)



RGT PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This 8-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.3-V to 5.5-V V<sub>CC</sub> operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

The PCA9534 consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) register. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the PCA9534 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine.

The PCA9534 open-drain interrupt ( $\overline{\text{INT}}$ ) output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the PCA9534 can remain a simple slave device.

The device's outputs (latched) have high-current drive capability for directly driving LEDs. It has low current consumption.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# PCA9534

## REMOTE 8-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

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Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C address and allow up to eight devices to share the same I<sup>2</sup>C bus or SMBus.

The PCA9534 is pin-to-pin and I<sup>2</sup>C address compatible with the PCF8574. However, software changes are required due to the enhancements in the PCA9534 over the PCF8574.

The PCA9534 is a low-power version of the PCA9554. The only difference between the PCA9534 and PCA9554 is that the PCA9534 eliminates an internal I/O pullup resistor, which dramatically reduces power consumption in the standby mode when the I/Os are held low.

The PCA9534A and PCA9534 are identical, except for their fixed I<sup>2</sup>C address. This allows for up to 16 of these devices (8 of each) on the same I<sup>2</sup>C bus.

### ORDERING INFORMATION

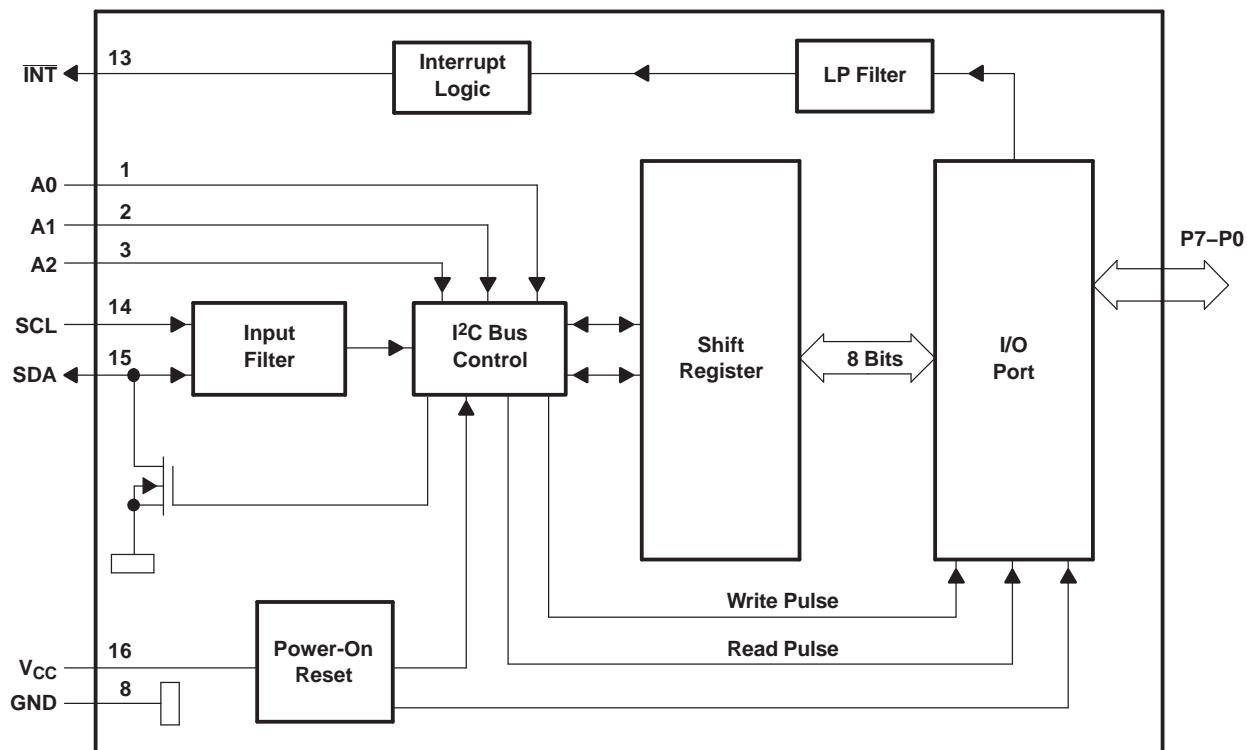
| T <sub>A</sub> | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGT              | Reel of 3000 | PCA9534RGTR           | PREVIEW          |
|                | QFN – RGV              | Reel of 2500 | PCA9534RGVR           | PREVIEW          |
|                | QSOP – DBQ             | Reel of 2500 | PCA9534DBQR           | PD534            |
|                | SOIC – DW              | Tube of 40   | PCA9534DW             | PCA9534          |
|                |                        | Reel of 2000 | PCA9534DWR            |                  |
|                | SSOP – DB              | Reel of 2000 | PCA9534DBR            | PD534            |
|                |                        | Tube of 80   | PCA9534DBT            |                  |
|                | TSSOP – PW             | Tube of 90   | PCA9534PW             | PD534            |
|                |                        | Reel of 2000 | PCA9534PWR            |                  |
|                | TVSOP – DGV            | Reel of 2000 | PCA9534DGVR           | PD534            |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## TERMINAL FUNCTIONS

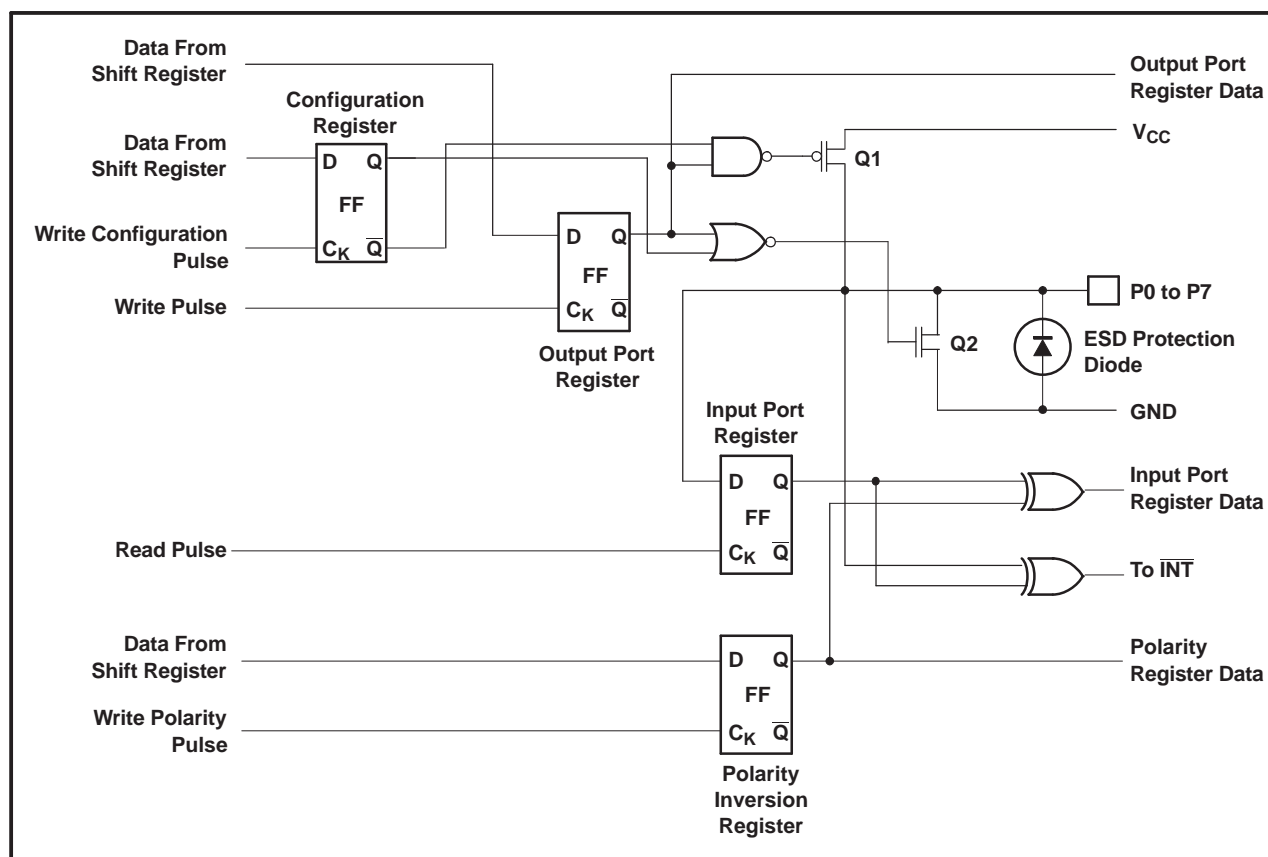
| NO. |   |                               | NAME            | DESCRIPTION   |
|-----|---|-------------------------------|-----------------|---|
|     | QSOP (DBQ),<br>SOIC (DW),<br>SSOP (DB),<br>TSSOP (PW), AND<br>TVSOP (DGV) | QFN (RGT)<br>AND<br>QFN (RGV) |                 |   |
| 1   |   | 15                            | A0              | Address input. Connect directly to V <sub>CC</sub> or ground.           |
| 2   |   | 16                            | A1              | Address input. Connect directly to V <sub>CC</sub> or ground.           |
| 3   |   | 1                             | A2              | Address input. Connect directly to V <sub>CC</sub> or ground.           |
| 4   |   | 2                             | P0              | P-port input/output. Push-pull design structure.                        |
| 5   |   | 3                             | P1              | P-port input/output. Push-pull design structure.                        |
| 6   |   | 4                             | P2              | P-port input/output. Push-pull design structure.                        |
| 7   |   | 5                             | P3              | P-port input/output. Push-pull design structure.                        |
| 8   |   | 6                             | GND             | Ground  |
| 9   |   | 7                             | P4              | P-port input/output. Push-pull design structure.                        |
| 10  |   | 8                             | P5              | P-port input/output. Push-pull design structure.                        |
| 11  |   | 9                             | P6              | P-port input/output. Push-pull design structure.                        |
| 12  |   | 10                            | P7              | P-port input/output. Push-pull design structure.                        |
| 13  |   | 11                            | INT             | Interrupt output. Connect to V <sub>CC</sub> through a pullup resistor. |
| 14  |   | 12                            | SCL             | Serial clock bus. Connect to V <sub>CC</sub> through a pullup resistor. |
| 15  |   | 13                            | SDA             | Serial data bus. Connect to V <sub>CC</sub> through a pullup resistor.  |
| 16  |   | 14                            | V <sub>CC</sub> | Supply voltage  |

## LOGIC DIAGRAM (POSITIVE LOGIC)



- A. Pin numbers shown are for DB, DBQ, DGV, DW, or PW package.  
B. All I/Os are set to inputs at reset.

## SIMPLIFIED SCHEMATIC OF P0 TO P7



A. At power-on reset, all registers return to default values.

## I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above  $V_{CC}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either  $V_{CC}$  or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

## I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 2).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

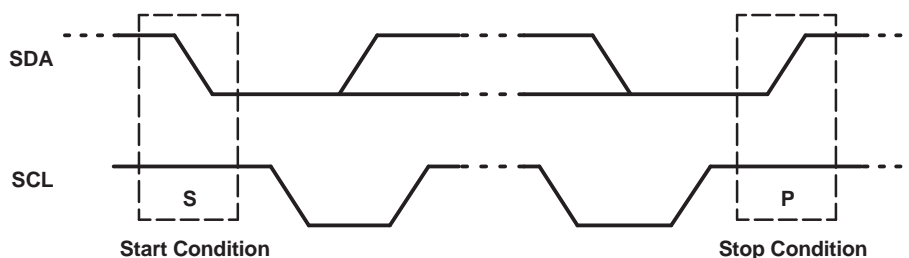


Figure 1. Definition of Start and Stop Conditions

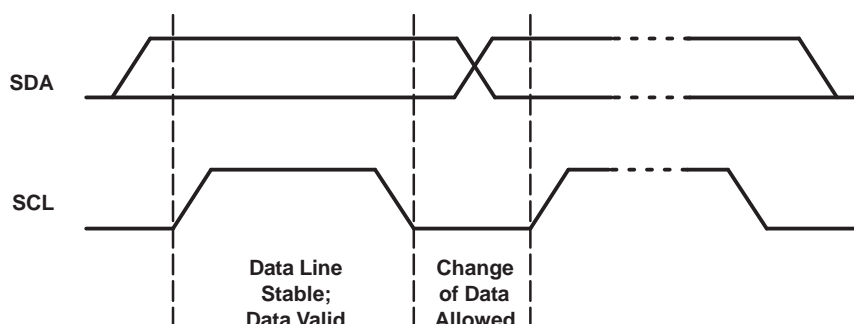


Figure 2. Bit Transfer

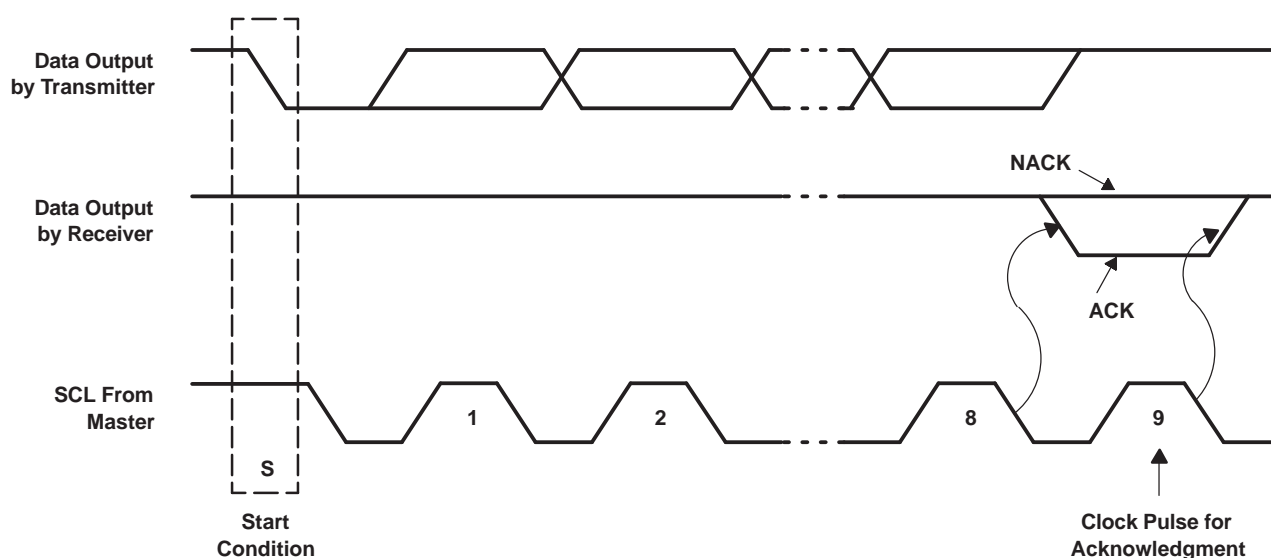


Figure 3. Acknowledgment on I<sup>2</sup>C Bus

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## REMOTE 8-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

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### Interface Definition

| BYTE                           | BIT     |    |    |    |    |    |    |                   |
|--------------------------------|---------|----|----|----|----|----|----|-------------------|
|                                | 7 (MSB) | 6  | 5  | 4  | 3  | 2  | 1  | 0 (LSB)           |
| I <sup>2</sup> C slave address | L       | H  | L  | L  | A2 | A1 | A0 | R/ $\overline{W}$ |
| Px I/O data bus                | P7      | P6 | P5 | P4 | P3 | P2 | P1 | P0                |

### Device Address

Figure 4 shows the address byte of the PCA9534.

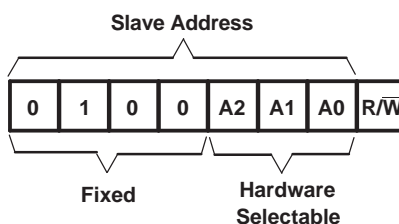


Figure 4. PCA9534 Address

### Address Reference

| INPUTS |    |    | I <sup>2</sup> C BUS SLAVE ADDRESS |
|--------|----|----|------------------------------------|
| A2     | A1 | A0 |                                    |
| L      | L  | L  | 32 (decimal), 20 (hexadecimal)     |
| L      | L  | H  | 33 (decimal), 21 (hexadecimal)     |
| L      | H  | L  | 34 (decimal), 22 (hexadecimal)     |
| L      | H  | H  | 35 (decimal), 23 (hexadecimal)     |
| H      | L  | L  | 36 (decimal), 24 (hexadecimal)     |
| H      | L  | H  | 37 (decimal), 25 (hexadecimal)     |
| H      | H  | L  | 38 (decimal), 26 (hexadecimal)     |
| H      | H  | H  | 39 (decimal), 27 (hexadecimal)     |

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

### Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the PCA9534. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

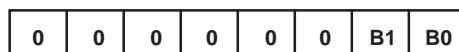


Figure 5. Control Register Bits

### Command Byte

| CONTROL REGISTER BITS |    | COMMAND BYTE (HEX) | REGISTER           | PROTOCOL        | POWER-UP DEFAULT |
|-----------------------|----|--------------------|--------------------|-----------------|------------------|
| B1                    | B0 |                    |                    |                 |                  |
| 0                     | 0  | 0x00               | Input Port         | Read byte       | xxxx xxxx        |
| 0                     | 1  | 0x01               | Output Port        | Read/write byte | 1111 1111        |
| 1                     | 0  | 0x02               | Polarity Inversion | Read/write byte | 0000 0000        |
| 1                     | 1  | 0x03               | Configuration      | Read/write byte | 1111 1111        |

## Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I<sup>2</sup>C device know that the Input Port register will be accessed next.

### Register 0 (Input Port Register)

| BIT     | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | X  | X  | X  | X  | X  | X  | X  | X  |

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

### Register 1 (Output Port Register)

| BIT     | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

### Register 2 (Polarity Inversion Register)

| BIT     | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

### Register 3 (Configuration Register)

| BIT     | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

## Power-On Reset

When power (from 0 V) is applied to V<sub>CC</sub>, an internal power-on reset holds the PCA9534 in a reset condition until V<sub>CC</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA9534 registers and I<sup>2</sup>C/SMBus state machine will initialize to their default states. After that, V<sub>CC</sub> must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

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## REMOTE 8-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

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### Interrupt Output ( $\overline{\text{INT}}$ )

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time,  $t_{IV}$ , the signal  $\overline{\text{INT}}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt or in a Stop event. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. In a Stop event,  $\overline{\text{INT}}$  is cleared after the rising edge of SDA. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The  $\overline{\text{INT}}$  output has an open-drain structure and requires pull-up resistor to  $V_{CC}$ .

### Bus Transactions

Data is exchanged between the master and PCA9534 through write and read commands.

#### Writes

Data is transmitted to the PCA9534 by sending the device address and setting the least-significant bit to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 6 and Figure 7). There is no limitation on the number of data bytes sent in one write transmission.

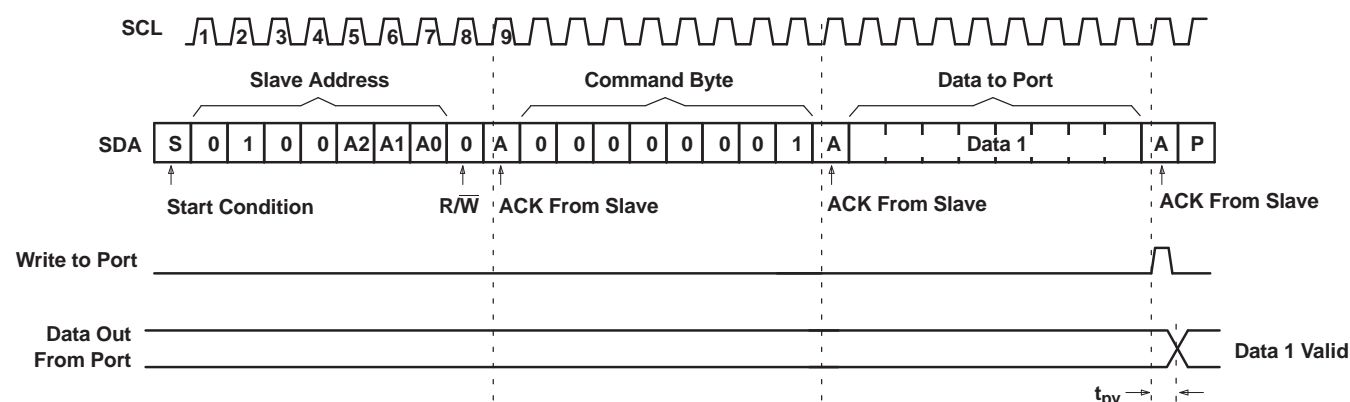


Figure 6. Write to Output Port Register

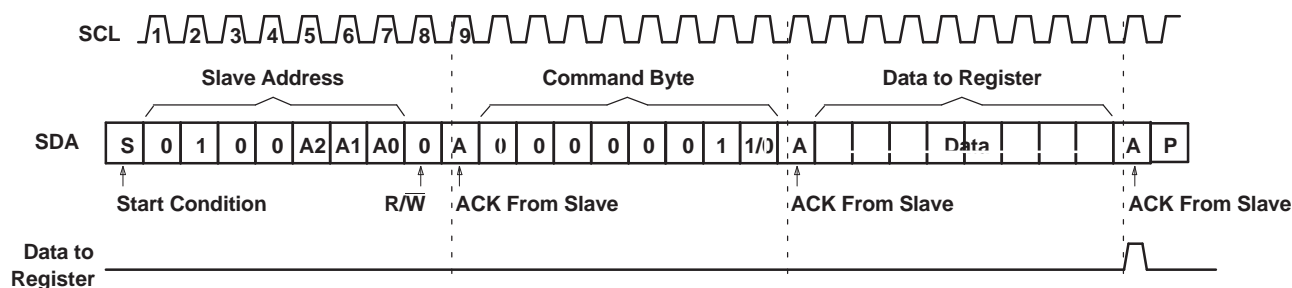


Figure 7. Write to Configuration or Polarity Inversion Registers



## Reads

The bus master first must send the PCA9534 address with the least-significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9534 (see Figure 8 and Figure 9). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

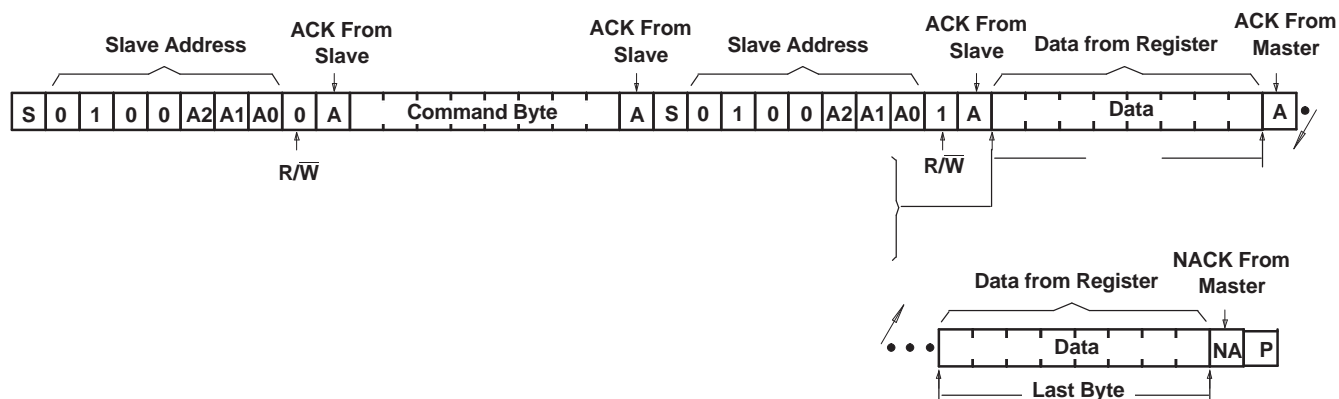
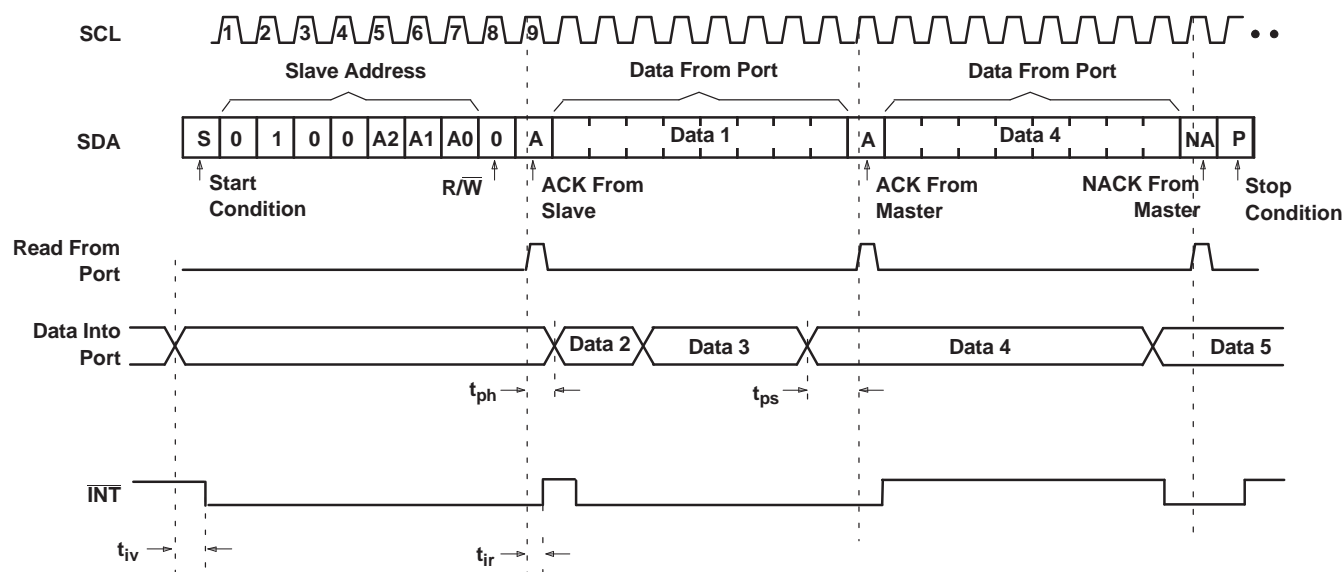


Figure 8. Read From Register



- This figure assumes that the command byte has previously been programmed with 00h.
- Transfer of data can be stopped at any moment by a stop condition.
- This figure eliminates the command byte transfer, a restart and slave address call between the initial slave address call and the actual data transfer from the P Port. See Figure 8 for these details.

Figure 9. Read Input Port Register

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## REMOTE 8-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

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### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |  | MIN  | MAX | UNIT    |
|------------------|--|--|-----|---------|
| V <sub>CC</sub>  | Supply voltage range                       | –0.5   | 6   | V       |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>         | –0.5   | 6   | V       |
| V <sub>O</sub>   | Output voltage range <sup>(2)</sup>        | –0.5   | 6   | V       |
| I <sub>IK</sub>  | Input clamp current                        | V <sub>I</sub> < 0                                     |     | –20 mA  |
| I <sub>OK</sub>  | Output clamp current                       | V <sub>O</sub> < 0                                     |     | –20 mA  |
| I <sub>IOK</sub> | Input/output clamp current                 | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |     | ±20 mA  |
| I <sub>OL</sub>  | Continuous output low current              | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |     | 50 mA   |
| I <sub>OH</sub>  | Continuous output high current             | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |     | –50 mA  |
| I <sub>CC</sub>  | Continuous current through GND             |  |     | –250 mA |
|                  | Continuous current through V <sub>CC</sub> |  |     | 160     |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(3)</sup>   | DB package   | 82  | °C/W    |
|                  |  | DBQ package  | 90  |         |
|                  |  | DGV package  | 86  |         |
|                  |  | DW package   | 46  |         |
|                  |  | N package  | 67  |         |
|                  |  | PW package   | 88  |         |
|                  |  | RGT package  | TBD |         |
|                  |  | RGV package  | TBD |         |
| T <sub>stg</sub> | Storage temperature range                  | –65  | 150 | °C      |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions

|                 |                                | MIN               | MAX                   | UNIT |
|-----------------|--------------------------------|-------------------|-----------------------|------|
| V <sub>CC</sub> | Supply voltage                 | 2.3               | 5.5                   | V    |
| V <sub>IH</sub> | High-level input voltage       | SCL, SDA          | 0.7 × V <sub>CC</sub> | V    |
|                 |                                | A0, A1, A2, P7–P0 | 2                     |      |
| V <sub>IL</sub> | Low-level input voltage        | SCL, SDA          | –0.5                  | V    |
|                 |                                | A0, A1, A2, P7–P0 | 0.3 × V <sub>CC</sub> |      |
| I <sub>OH</sub> | High-level output current      | P7–P0             | –10                   | mA   |
| I <sub>OL</sub> | Low-level output current       | P7–P0             | 25                    | mA   |
| T <sub>A</sub>  | Operating free-air temperature | –40               | 85                    | °C   |

## Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER        |   | TEST CONDITIONS  | V <sub>CC</sub>  | MIN  | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|---|--|------------------|------|--------------------|------|------|
| V <sub>IK</sub>  | Input diode clamp voltage                       | I <sub>I</sub> = −18 mA  | 2.3 V to 5.5 V   | −1.2 |                    |      | V    |
| V <sub>POR</sub> | Power-on reset voltage                          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0  | V <sub>POR</sub> |      | 1.5                | 1.65 | V    |
| V <sub>OH</sub>  | P-port high-level output voltage <sup>(2)</sup> | I <sub>OH</sub> = −8 mA  | 2.3 V            | 1.8  |                    |      | V    |
|                  |   |  | 3 V              | 2.6  |                    |      |      |
|                  |   |  | 4.5 V            | 4.1  |                    |      |      |
|                  |   |  | 4.75 V           | 4.1  |                    |      |      |
|                  |   | I <sub>OH</sub> = −10 mA   | 2.3 V            | 1.7  |                    |      |      |
|                  |   |  | 3 V              | 2.5  |                    |      |      |
|                  |   |  | 4.5 V            | 4    |                    |      |      |
|                  |   |  | 4.75 V           | 4    |                    |      |      |
| I <sub>OL</sub>  | SDA   | V <sub>OL</sub> = 0.4 V  | 2.3 V to 5.5 V   | 3    | 8                  |      | mA   |
|                  | P port <sup>(3)</sup>                           | V <sub>OL</sub> = 0.5 V  | 2.3 V            | 8    | 10                 |      |      |
|                  |   |  | 3 V              | 8    | 14                 |      |      |
|                  |   |  | 4.5 V            | 8    | 17                 |      |      |
|                  |   |  | 4.75 V           | 8    | 35                 |      |      |
|                  |   | V <sub>OL</sub> = 0.7 V  | 2.3 V            | 10   | 13                 |      |      |
|                  |   |  | 3 V              | 10   | 19                 |      |      |
|                  |   |  | 4.5 V            | 10   | 24                 |      |      |
|                  |   |  | 4.75 V           | 10   | 45                 |      |      |
|                  | INT   | V <sub>OL</sub> = 0.4 V  | 2.3 V to 5.5 V   | 3    | 10                 |      |      |
| I <sub>I</sub>   | SCL, SDA  | V <sub>I</sub> = V <sub>CC</sub> or GND  | 2.3 V to 5.5 V   |      |                    | ±1   | μA   |
|                  | A0, A1, A2                                      |  |                  |      |                    | ±1   |      |
| I <sub>IH</sub>  | P port  | V <sub>I</sub> = V <sub>CC</sub>   | 2.3 V to 5.5 V   |      |                    | 1    | μA   |
| I <sub>IL</sub>  | P port  | V <sub>I</sub> = GND   | 2.3 V to 5.5 V   |      |                    | −1   | μA   |
| I <sub>CC</sub>  | Operating mode                                  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0,<br>I/O = inputs, f <sub>SCL</sub> = 400 kHz | 5.5 V            |      | 104                | 175  | μA   |
|                  |   |  | 3.6 V            |      | 50                 | 90   |      |
|                  |   |  | 2.7 V            |      | 20                 | 65   |      |
|                  |   | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0,<br>I/O = inputs, f <sub>SCL</sub> = 100 kHz | 5.5 V            |      | 60                 | 150  |      |
|                  |   |  | 3.6 V            |      | 15                 | 40   |      |
|                  |   |  | 2.7 V            |      | 8                  | 20   |      |
|                  | Standby mode                                    | V <sub>I</sub> = GND, I <sub>O</sub> = 0,<br>I/O = inputs, f <sub>SCL</sub> = 0 kHz                      | 5.5 V            |      | 0.25               | 1    |      |
|                  |   |  | 3.6 V            |      | 0.2                | 0.9  |      |
|                  |   |  | 2.7 V            |      | 0.1                | 0.8  |      |
| ΔI <sub>CC</sub> | Additional current in standby mode              | One input at V <sub>CC</sub> − 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND                          | 2.3 V to 5.5 V   |      |                    | 1.5  | mA   |
|                  |   | All LED I/Os at V <sub>I</sub> = 4.3 V,<br>f <sub>SCL</sub> = 0 kHz                                      | 5.5 V            |      |                    | 1    |      |
| C <sub>i</sub>   | SCL   | V <sub>I</sub> = V <sub>CC</sub> or GND  | 2.3 V to 5.5 V   |      | 4                  | 5    | pF   |
| C <sub>io</sub>  | SDA   | V <sub>IO</sub> = V <sub>CC</sub> or GND   | 2.3 V to 5.5 V   |      | 5.5                | 6.5  | pF   |
|                  | P port  |  |                  |      | 8                  | 9.5  |      |

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

(2) The total current sourced by all I/Os must be limited to 85 mA.

(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7–P0) must be limited to a maximum current of 200 mA.

# PCA9534

## REMOTE 8-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

SCPS124B–SEPTEMBER 2006–REVISED FEBRUARY 2007

### I<sup>2</sup>C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see [Figure 10](#))

|                       |  |  | STANDARD MODE<br>I <sup>2</sup> C BUS |      | FAST MODE<br>I <sup>2</sup> C BUS     |     | UNIT |
|-----------------------|--|--|---------------------------------------|------|---------------------------------------|-----|------|
|                       |  |  | MIN                                   | MAX  | MIN                                   | MAX |      |
| f <sub>scl</sub>      | I <sup>2</sup> C clock frequency                         |  | 0                                     | 100  | 0                                     | 400 | kHz  |
| t <sub>sch</sub>      | I <sup>2</sup> C clock high time                         |  | 4                                     |      | 0.6                                   |     | μs   |
| t <sub>scl</sub>      | I <sup>2</sup> C clock low time                          |  | 4.7                                   |      | 1.3                                   |     | μs   |
| t <sub>sp</sub>       | I <sup>2</sup> C spike time                              |  |                                       | 50   |                                       | 50  | ns   |
| t <sub>sds</sub>      | I <sup>2</sup> C serial-data setup time                  |  | 250                                   |      | 100                                   |     | ns   |
| t <sub>sdh</sub>      | I <sup>2</sup> C serial-data hold time                   |  | 0                                     |      | 0                                     |     | ns   |
| t <sub>icr</sub>      | I <sup>2</sup> C input rise time                         |  |                                       | 1000 | 20 + 0.1C <sub>b</sub> <sup>(1)</sup> | 300 | ns   |
| t <sub>icf</sub>      | I <sup>2</sup> C input fall time                         |  |                                       | 300  | 20 + 0.1C <sub>b</sub> <sup>(1)</sup> | 300 | ns   |
| t <sub>ocf</sub>      | I <sup>2</sup> C output fall time                        | 10-pF to 400-pF bus                      |                                       | 300  | 20 + 0.1C <sub>b</sub> <sup>(1)</sup> | 300 | ns   |
| t <sub>buf</sub>      | I <sup>2</sup> C bus free time between stop and start    |  | 4.7                                   |      | 1.3                                   |     | μs   |
| t <sub>sts</sub>      | I <sup>2</sup> C start or repeated start condition setup |  | 4.7                                   |      | 0.6                                   |     | μs   |
| t <sub>sth</sub>      | I <sup>2</sup> C start or repeated start condition hold  |  | 4                                     |      | 0.6                                   |     | μs   |
| t <sub>sps</sub>      | I <sup>2</sup> C stop condition setup                    |  | 4                                     |      | 0.6                                   |     | μs   |
| t <sub>vd(data)</sub> | Valid data time  | SCL low to SDA output valid              | 300                                   |      | 50                                    |     | ns   |
| t <sub>vd(ack)</sub>  | Valid data time of ACK condition                         | ACK signal from SCL low to SDA (out) low | 0.3                                   | 3.45 | 0.1                                   | 0.9 | μs   |
| C <sub>b</sub>        | I <sup>2</sup> C bus capacitive load                     |  |                                       | 400  |                                       | 400 | ns   |

(1) C<sub>b</sub> = total capacitive of one bus in pF

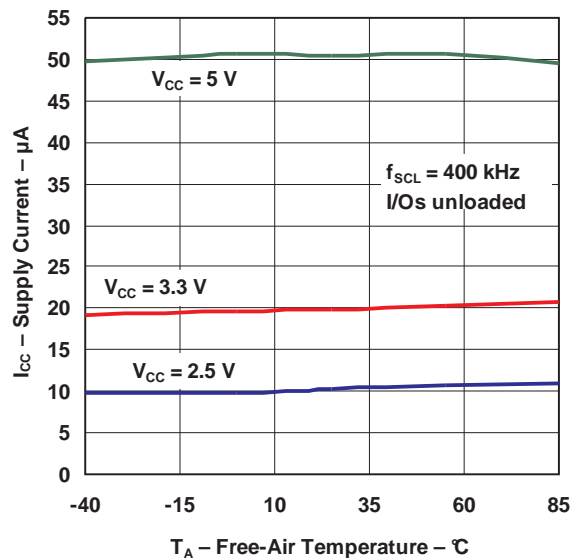
### Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see [Figure 11](#) and [Figure 12](#))

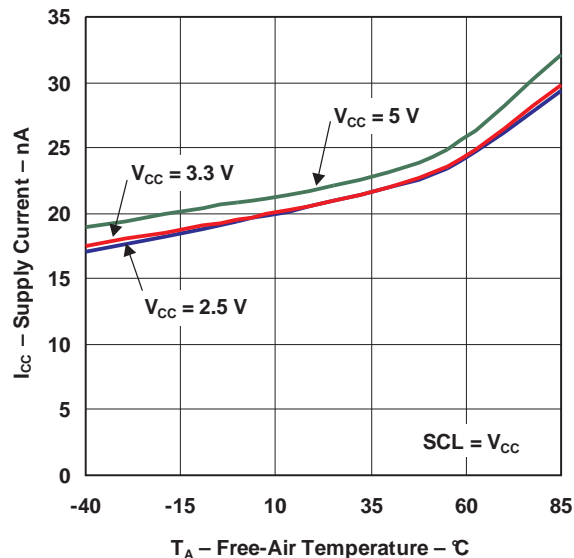
| PARAMETER       |                            | FROM<br>(INPUT) | TO<br>(OUTPUT)          | STANDARD MODE<br>I <sup>2</sup> C BUS |     | FAST MODE<br>I <sup>2</sup> C BUS |     | UNIT |
|-----------------|----------------------------|-----------------|-------------------------|---------------------------------------|-----|-----------------------------------|-----|------|
|                 |                            |                 |                         | MIN                                   | MAX | MIN                               | MAX |      |
| t <sub>iv</sub> | Interrupt valid time       | P port          | $\overline{\text{INT}}$ |                                       | 4   |                                   | 4   | μs   |
| t <sub>ir</sub> | Interrupt reset delay time | SCL             | $\overline{\text{INT}}$ |                                       | 4   |                                   | 4   | μs   |
| t <sub>pV</sub> | Output data valid          | SCL             | P7–P0                   |                                       | 200 |                                   | 200 | ns   |
| t <sub>ps</sub> | Input data setup time      | P port          | SCL                     | 100                                   |     | 100                               |     | ns   |
| t <sub>ph</sub> | Input data hold time       | P port          | SCL                     | 1                                     |     | 1                                 |     | μs   |

## TYPICAL CHARACTERISTICS

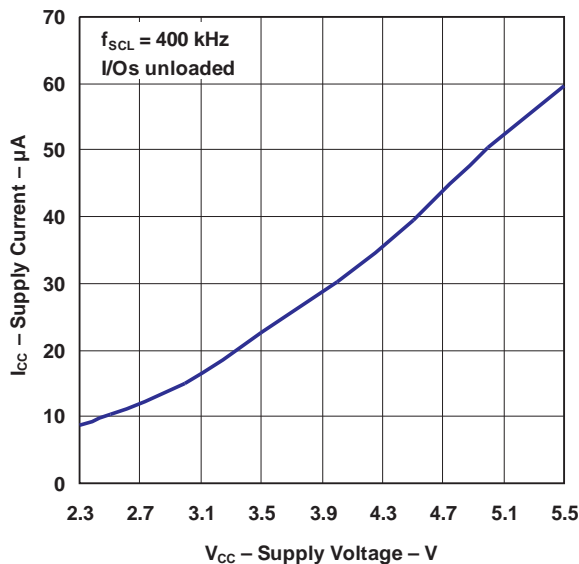
SUPPLY CURRENT  
vs  
TEMPERATURE



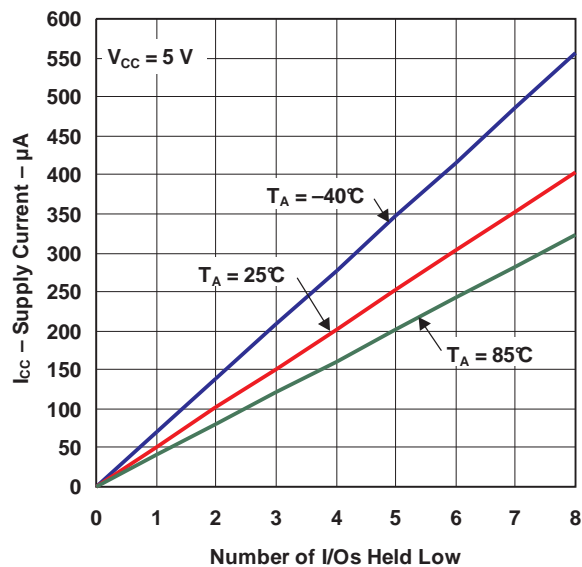
QUIESCENT SUPPLY CURRENT  
vs  
TEMPERATURE



SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE

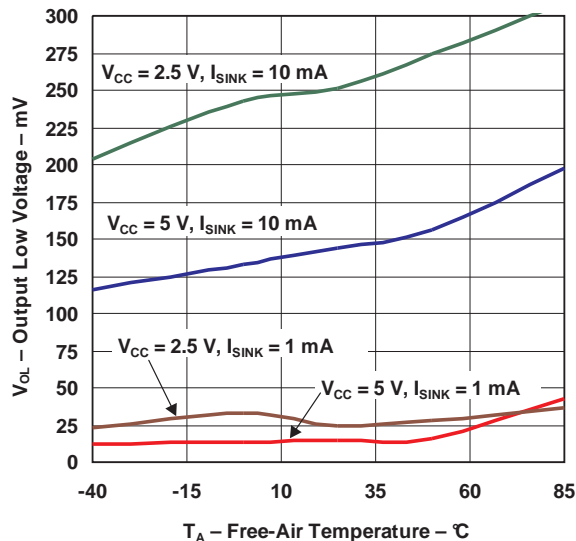


SUPPLY CURRENT  
vs  
NUMBER OF I/Os HELD LOW

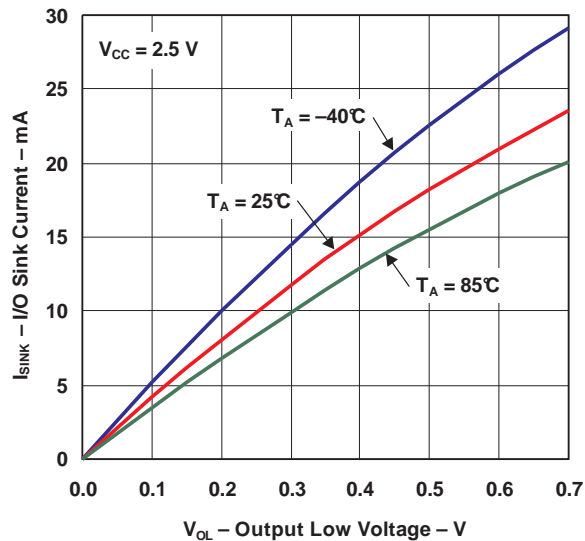


## TYPICAL CHARACTERISTICS (continued)

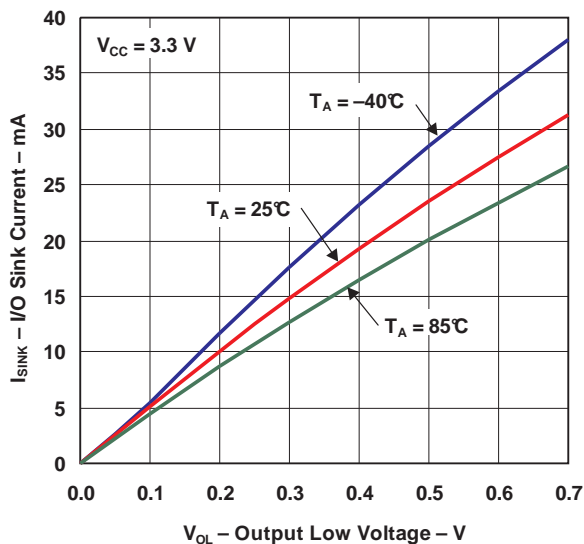
I/O OUTPUT LOW VOLTAGE  
vs  
TEMPERATURE



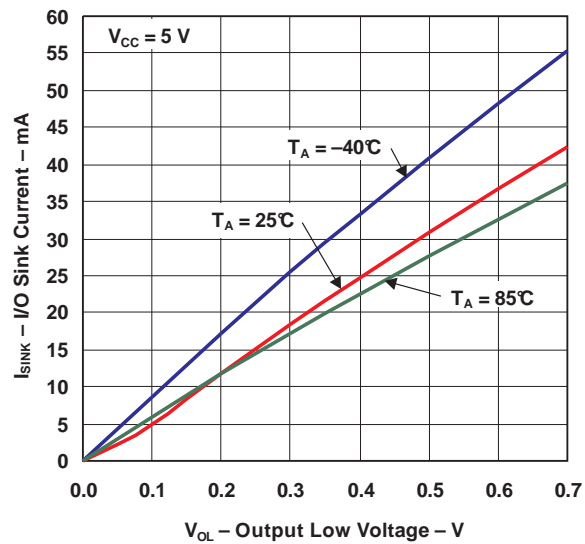
I/O SINK CURRENT  
vs  
OUTPUT LOW VOLTAGE



I/O SINK CURRENT  
vs  
OUTPUT LOW VOLTAGE

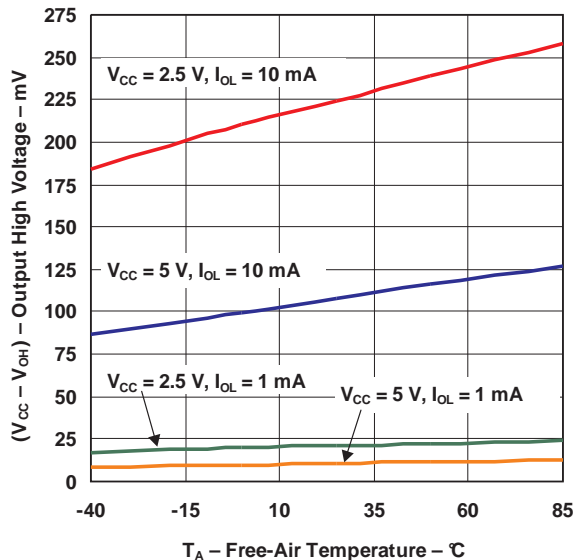


I/O SINK CURRENT  
vs  
OUTPUT LOW VOLTAGE

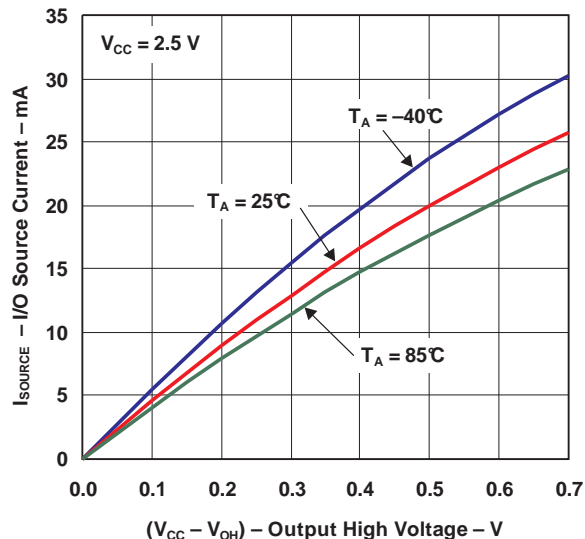


# TYPICAL CHARACTERISTICS (continued)

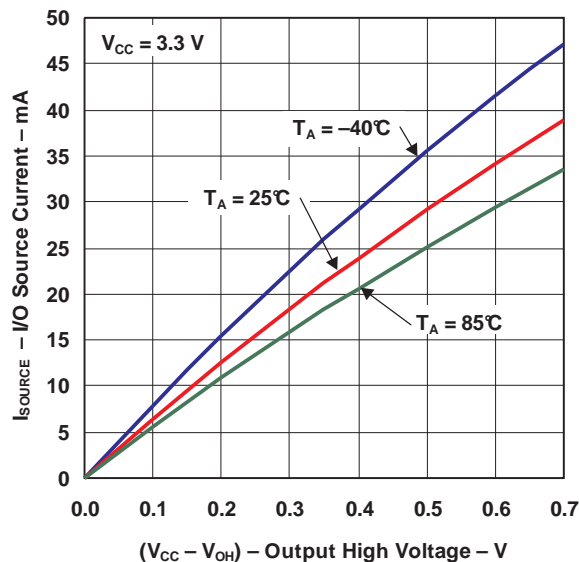
I/O OUTPUT HIGH VOLTAGE  
vs  
TEMPERATURE



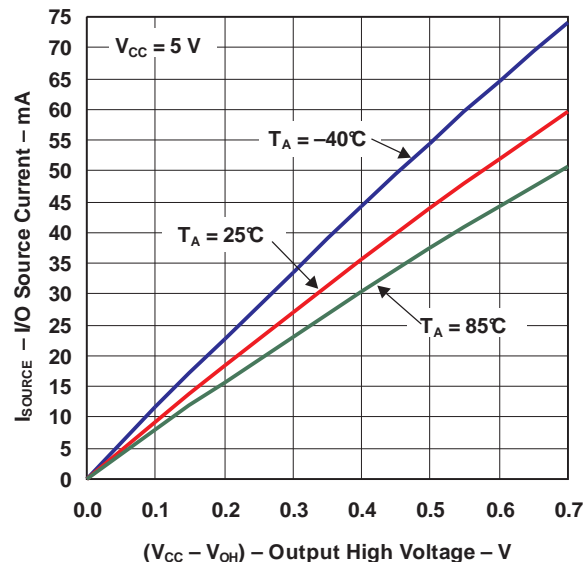
I/O SOURCE CURRENT  
vs  
OUTPUT HIGH VOLTAGE



I/O SOURCE CURRENT  
vs  
OUTPUT HIGH VOLTAGE

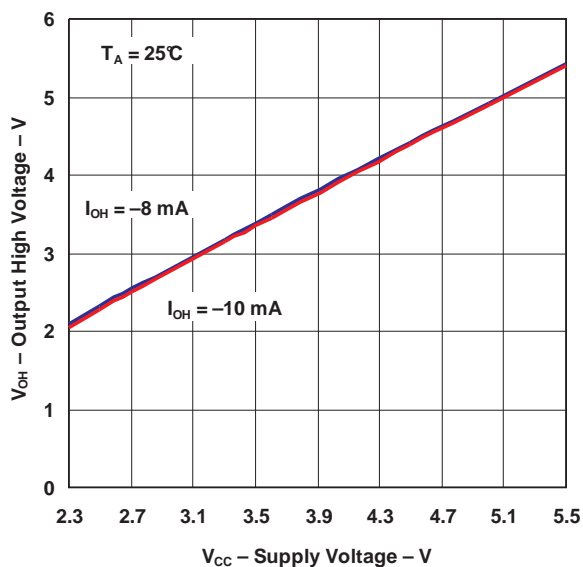


I/O SOURCE CURRENT  
vs  
OUTPUT HIGH VOLTAGE



## TYPICAL CHARACTERISTICS (continued)

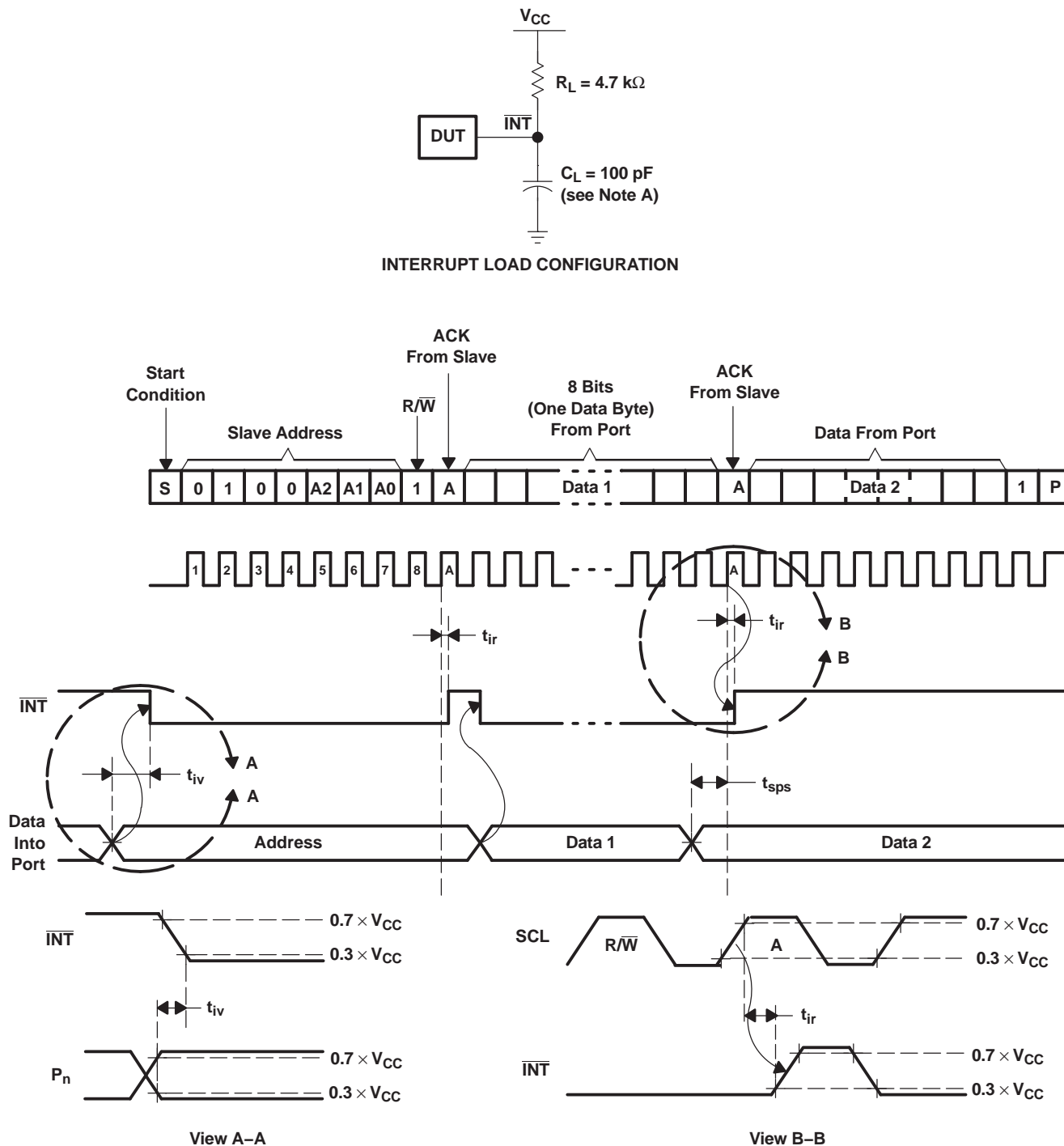
OUTPUT HIGH VOLTAGE  
vs  
SUPPLY VOLTAGE







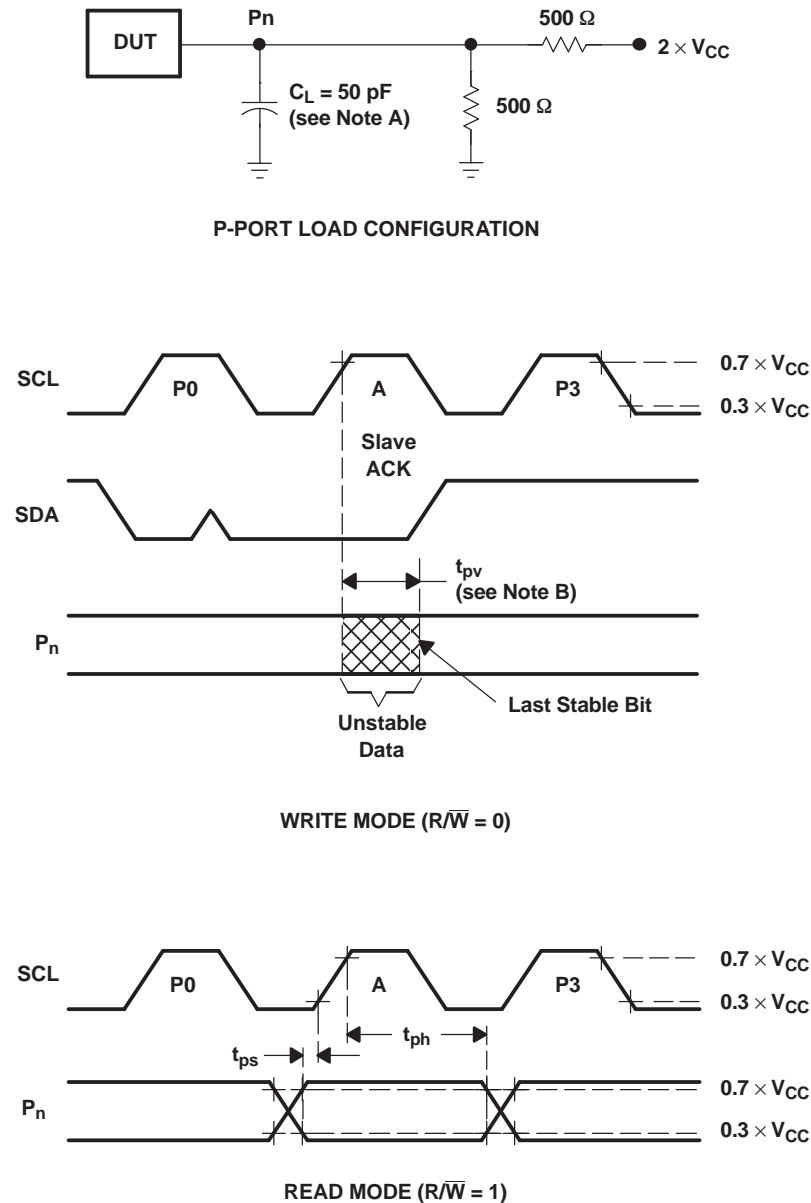
## PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

**Figure 11. Interrupt Load Circuit and Voltage Waveforms**

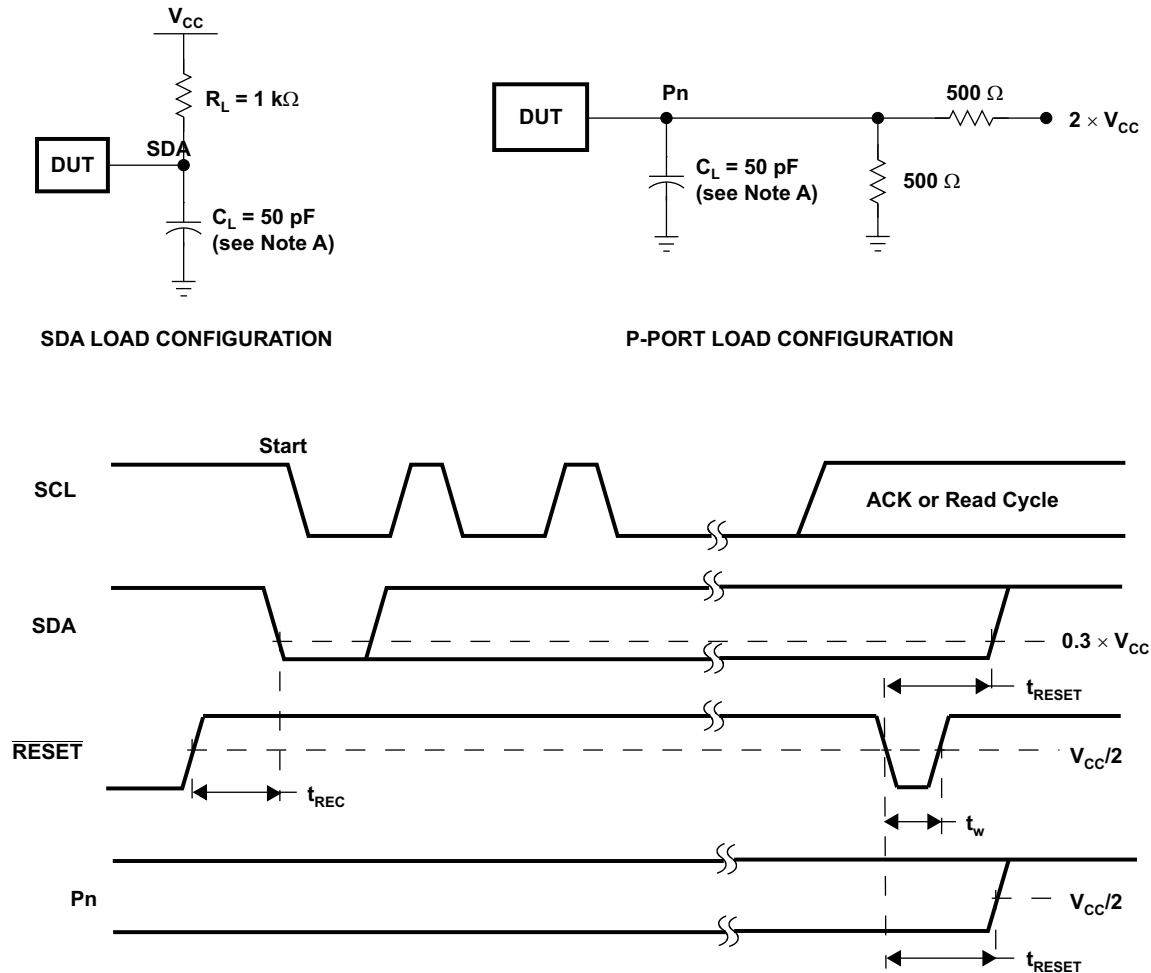
## PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 12. P-Port Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)

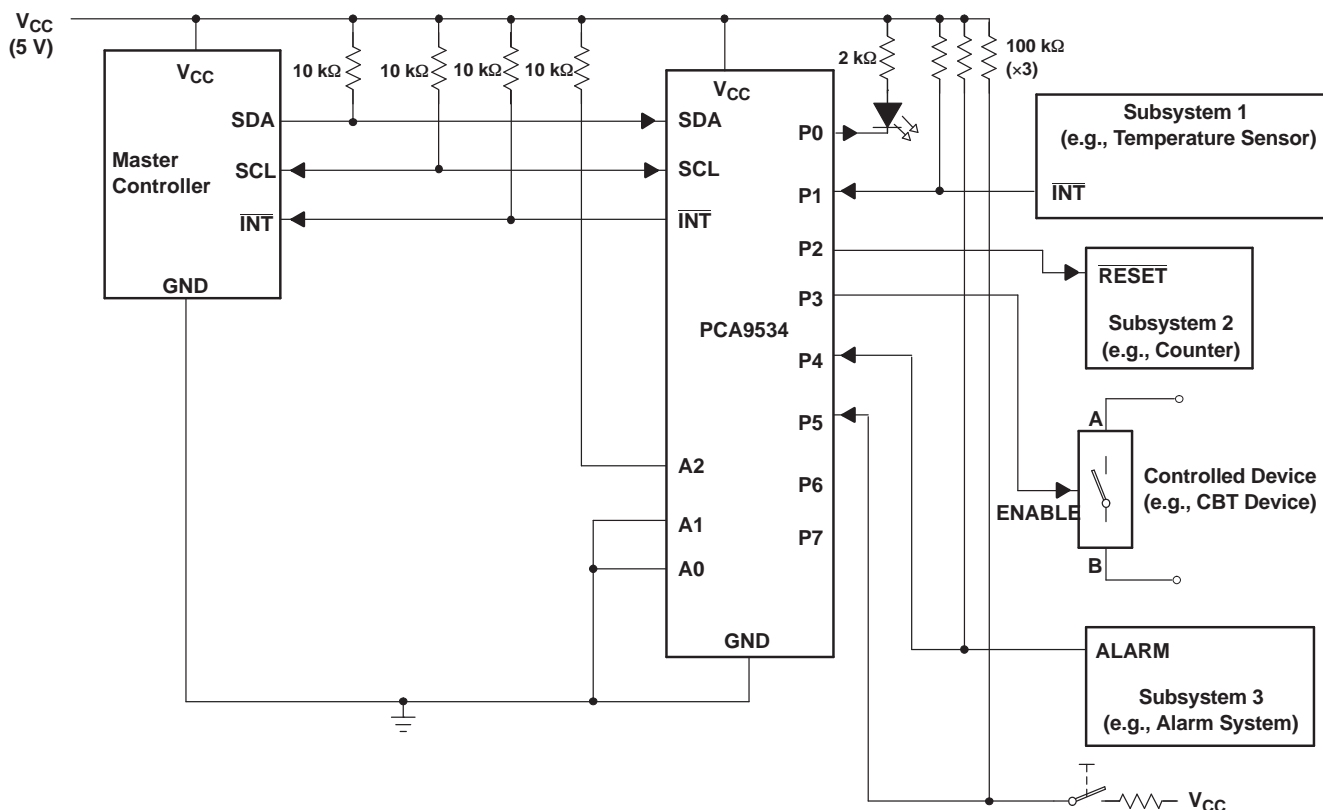


- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. I/Os are configured as inputs.
- D. All parameters and waveforms are not applicable to all devices.

**Figure 13. Reset Load Circuits and Voltage Waveforms**

## APPLICATION INFORMATION

Figure 14 shows an application in which the PCA9534 can be used.



- A. Device address is configured as 0100100 for this example.
- B. P0, P2, and P3 are configured as outputs.
- C. P1, P4, and P5 are configured as inputs.
- D. P6 and P7 are not used and must be configured as outputs.

**Figure 14. Typical Application**

## APPLICATION INFORMATION (continued)

### Minimizing $I_{CC}$ When the I/O Controls LEDs

When the I/Os are used to control LEDs, they are normally connected to  $V_{CC}$  through a resistor, as shown in Figure 14. Because the LED acts as a diode, when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The supply current,  $I_{CC}$ , increases as  $V_{IN}$  becomes lower than  $V_{CC}$  and is specified as  $\Delta I_{CC}$  in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of the I/O pins is greater than or equal to  $V_{CC}$  when the LED is off to minimize current consumption. Figure 15 shows a high-value resistor in parallel with the LED. Figure 16 shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{CC}$  and prevents additional supply-current consumption when the LED is off.

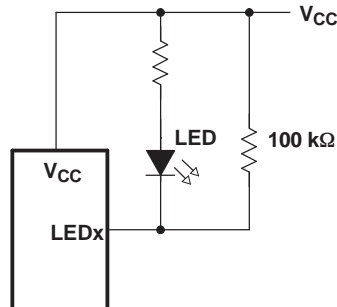


Figure 15. High-Value Resistor in Parallel With the LED

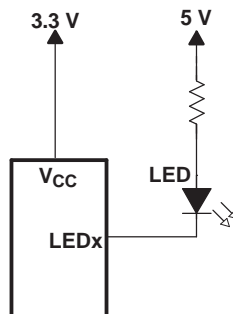


Figure 16. Device Supplied by a Lower Voltage

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PCA9534DB        | ACTIVE                | SSOP         | DB              | 16   | 80          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534DBG4      | ACTIVE                | SSOP         | DB              | 16   | 80          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534DBQR      | PREVIEW               | SSOP/QSOP    | DBQ             | 16   | 2500        | TBD                     | Call TI          | Call TI                      |
| PCA9534DBR       | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534DBG4      | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534DGVR      | ACTIVE                | TVSOP        | DGV             | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534DGVRG4    | ACTIVE                | TVSOP        | DGV             | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534DW        | ACTIVE                | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534DWR       | ACTIVE                | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534PW        | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534PWG4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534PWR       | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534PWRG4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9534RGTR      | PREVIEW               | QFN          | RGT             | 16   | 3000        | TBD                     | Call TI          | Call TI                      |
| PCA9534RGVR      | PREVIEW               | QFN          | RGV             | 16   | 2500        | TBD                     | Call TI          | Call TI                      |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

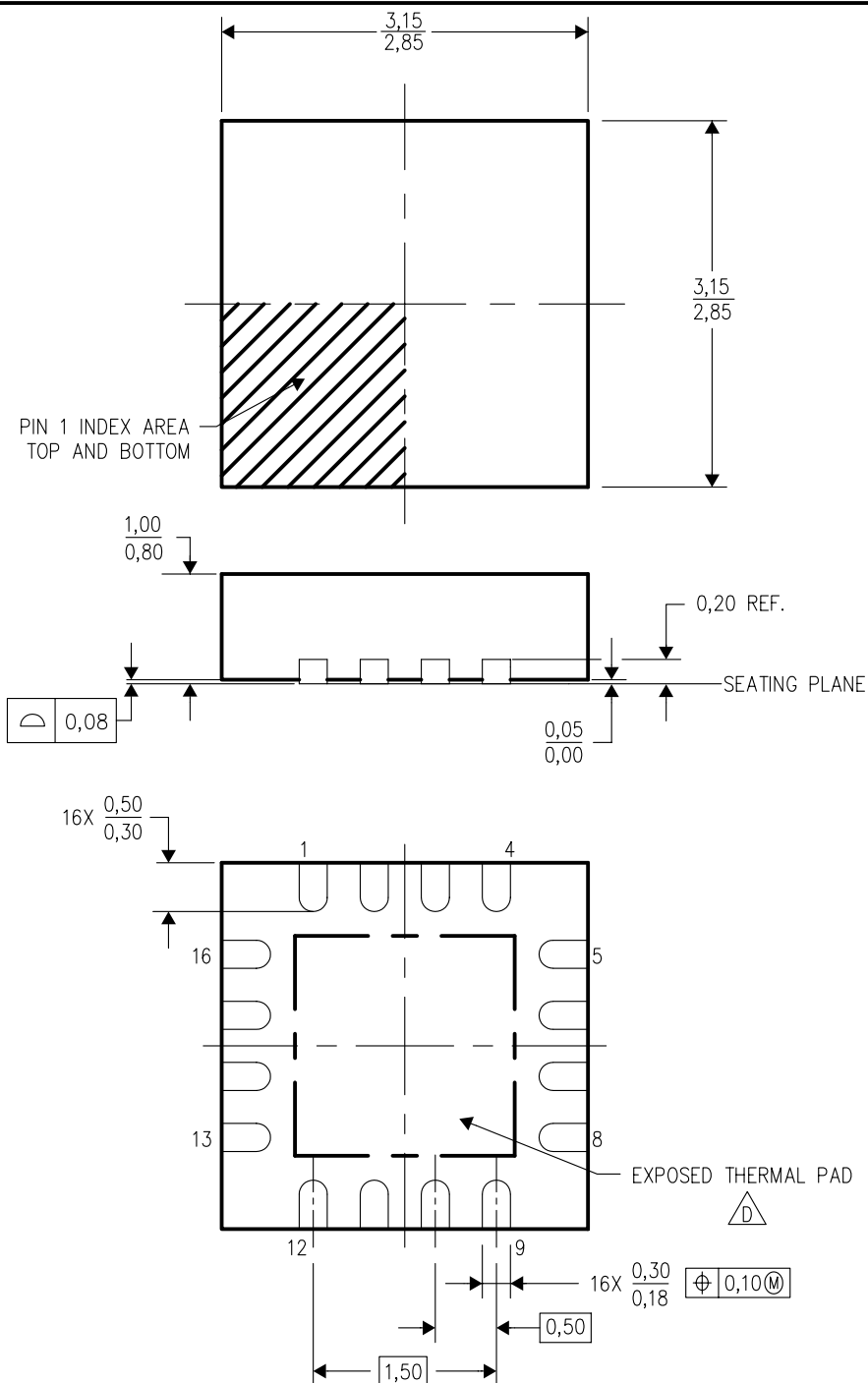
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

RGT (S-PQFP-N16)

PLASTIC QUAD FLATPACK

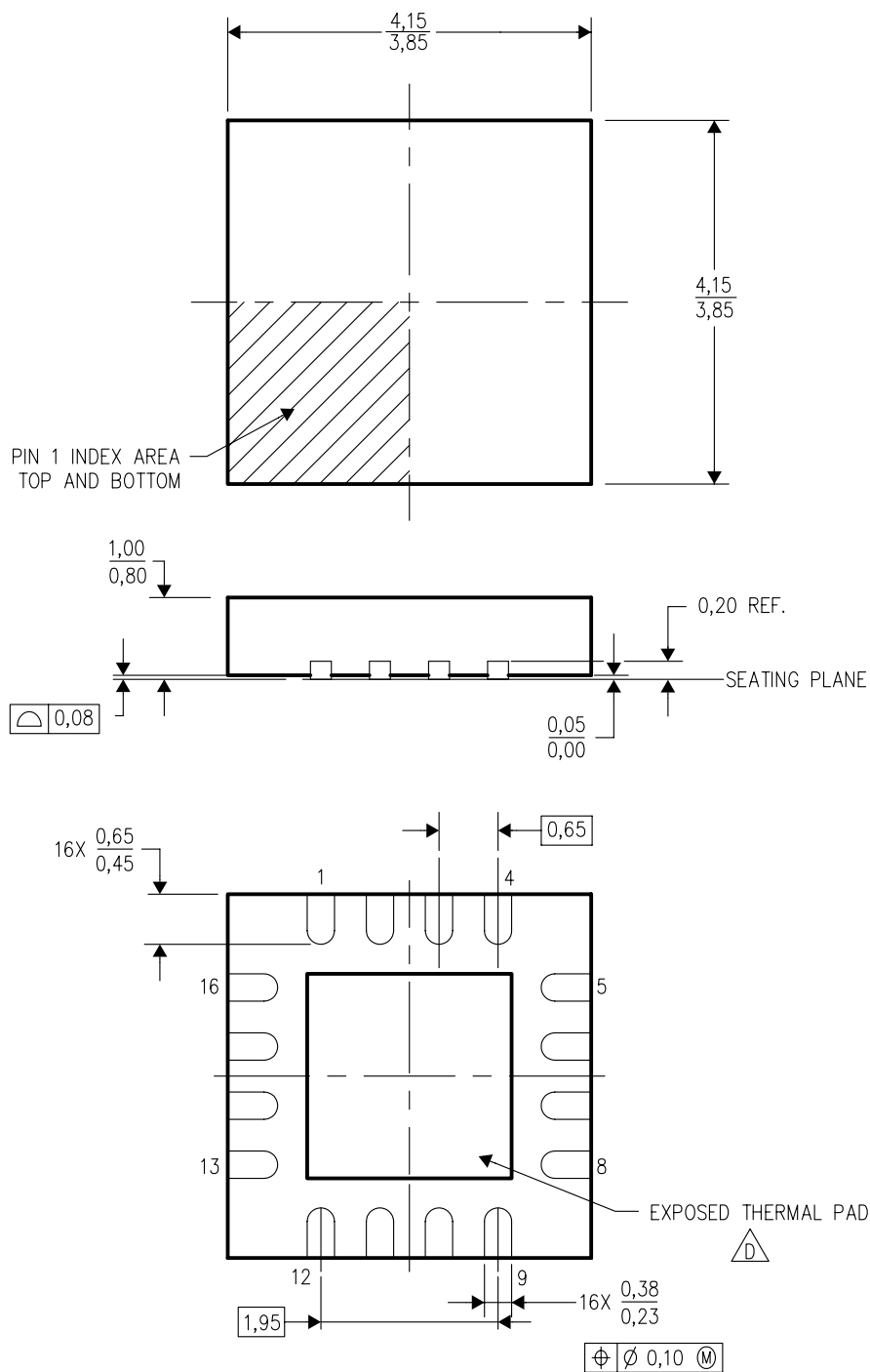


4203495/E 11/04


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - $\triangle D$  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

## RGV (S-PQFP-N16)

## PLASTIC QUAD FLATPACK

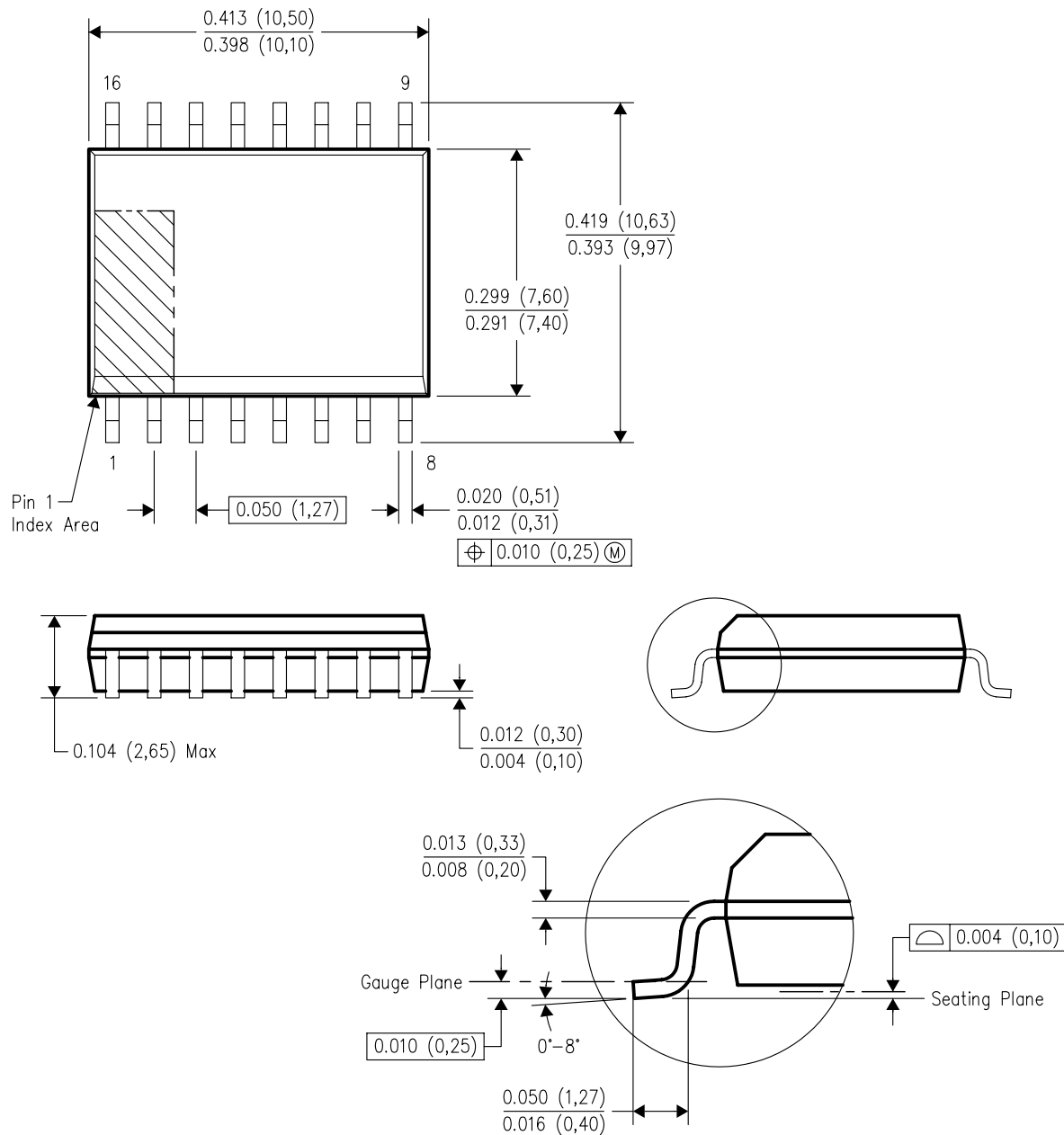


4203497/D 11/04

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE

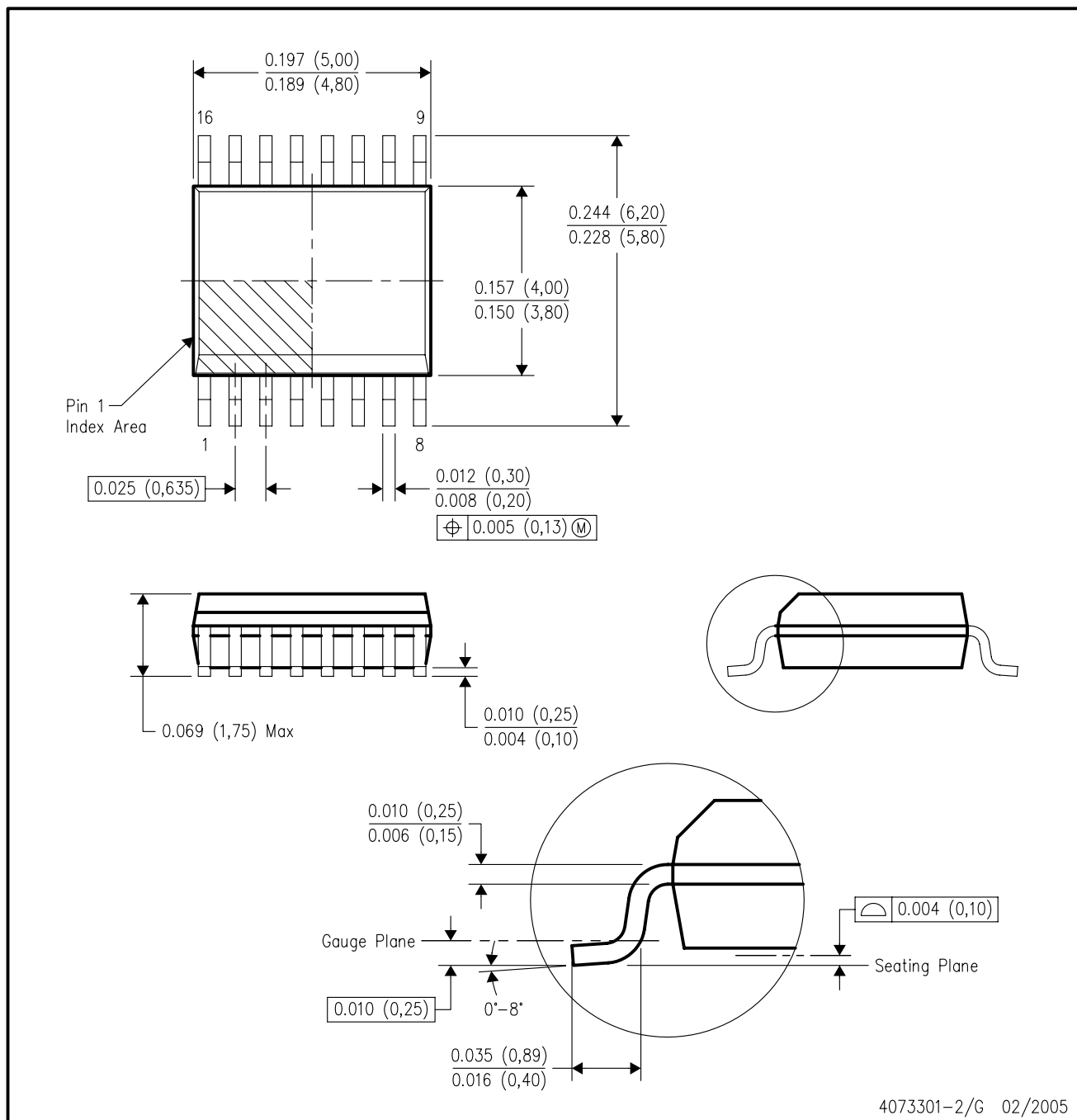


4040000-2/F 06/2004

- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-013 variation AA.

## DBQ (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AB.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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#### Как с нами связаться

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