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RapID Platform DLR Network Interface

Module Datasheet

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TABLE OF CONTENTS

1. Module Overview 5
2. Physical Dimensions and Connector Pinout 6
   2.1 Physical Constraints 6
   2.2 Signal Interface Connector 8
   2.3 Connector Pinout 10
   2.4 Power requirements 15
   2.5 Reset Requirements 15
3. Communication Interfaces between the Host Processor and DLR Network Interface Module 15
   3.1 UART Host Interface 15
   3.2 Parallel Host Interface 16
4. Considerations for Production and Maintenance 17
   4.1 Boot Loader 18
   4.2 JTAG 18
5. For Additional Information 20
6. Revision History 20

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LIST OF FIGURES

Figure 1 – Overview of Module Components and Interfaces.....5
Figure 2 - Dimensions of the DLR Network Interface Module (Plane View).....7
Figure 3 - Dimensions of the DLR Network Interface Module (Cross-section) 7
Figure 4 - Socket dimensions to mate the DLR Network Interface Module 8
Figure 5 - Location of X1 connector and Pin A1.....9
Figure 6 - Summary of Connector Pin Names.....10
Figure 7 – UART Host Interface Connection 16
Figure 8 – Parallel Host Interface Connection.....16
Figure 9 – Programming Connections and Devices 17

LIST OF TABLES

Table 1 – DLR Network Interface Module Connector Pin Definition – X1-A Connector.....11
Table 2 – DLR Network Interface Module Connector Pin Definition – X1-B Connector.....12
Table 3 – DLR Network Interface Module Connector Pin Definition – X1-C Connector.....13
Table 4 – DLR Network Interface Module Connector Pin Definition – X1-D Connector.....14
Table 5 – Document Revision History for IA211130109.....20

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1. Module Overview

The RapID Platform DLR Network Interface module contains everything needed including the communications controller, protocol stacks, Flash, RAM, and analog driver. Figure 1 provides an overview of the module.

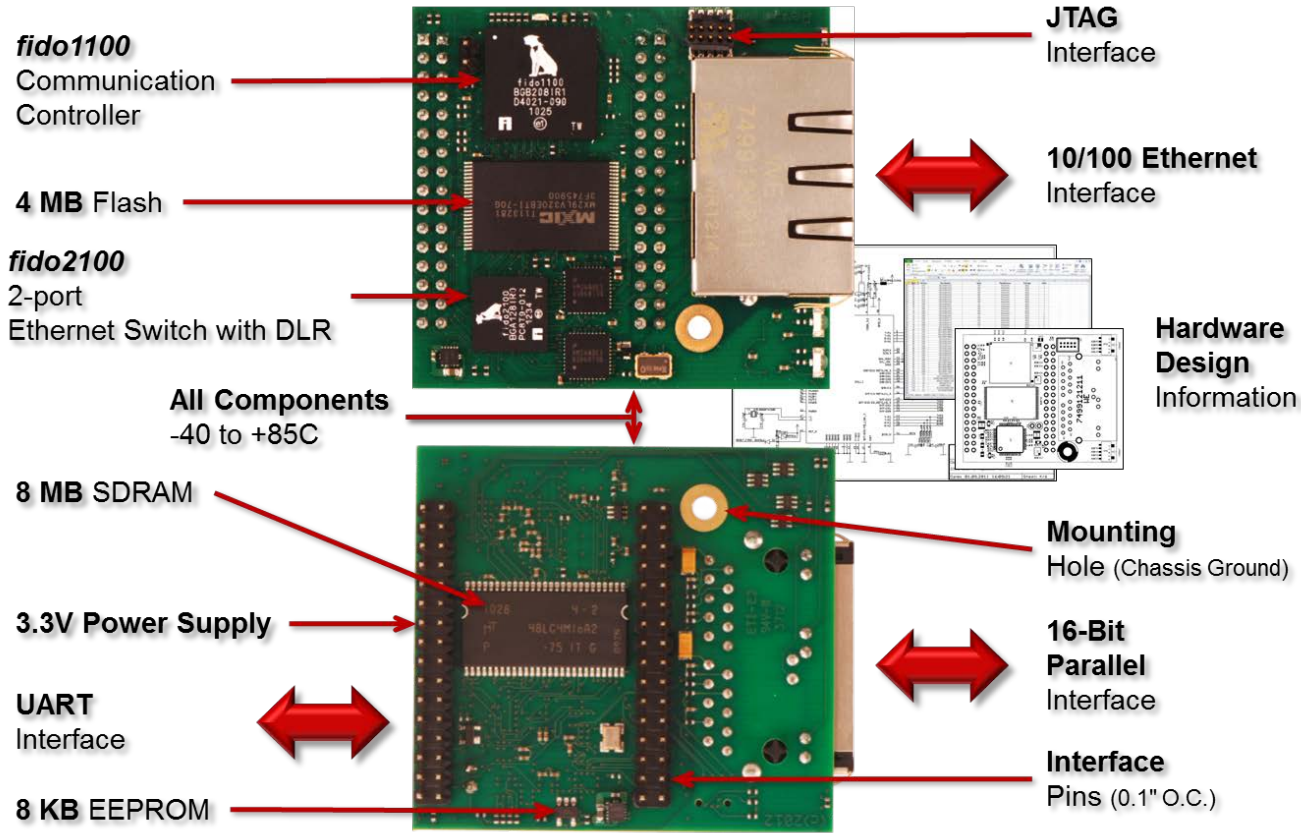

Figure 1 – Overview of Module Components and Interfaces

The remainder of this document provides technical details for the DLR Network Interface module and the information necessary to integrate the module into a circuit card.

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2. Physical Dimensions and Connector Pinout

This paragraph describes the process for installing the DLR Network Interface module in a field device's application hardware. The process is straightforward and consists of designing a low-cost socket into the application hardware to provide signal interface and power connections. Only a single +3.3V power supply is required. In addition, a UART or parallel interface is used to communicate with a host processor.

Any unused module inputs may be left floating. The appropriate pull-up resistors are included on the module.

2.1 Physical Constraints

The DLR Network Interface module is 2.028" (51,5mm) x 2.216" (56,3mm) as shown in Figure 2. The module height from the X1 seating plane is 0.715" (18,2mm) as shown in Figure 3. The RJ45 (Ethernet) connector and all LEDs are conveniently located along one edge of the PC board for easy access. The RJ45 extends 3.0mm past the edge of the PC board to allow for installation in an enclosure. The LEDs are flush with the PC board edge. The Link/Activity LEDs for Ethernet ports 1 and 2 are located inside the RJ45 connector. The power and bi-color LED indicators are on the top side of the PC board as shown in Figure 3.

All components on the bottom of the PC board are above the X1 connector seating plane, as shown in Figure 3. All components on the application hardware that are within the DLR Network Interface module outline should be shorter than the target system's X1 mating connector to prevent physical interference. The recommended mating connector defined in the next paragraph (SSW-116-21-F-D) has a height of 0.335" (8,51mm). If the recommended mating connector is used, all components within the DLR Network Interface module outline should be shorter than 0.335" (8,51mm).

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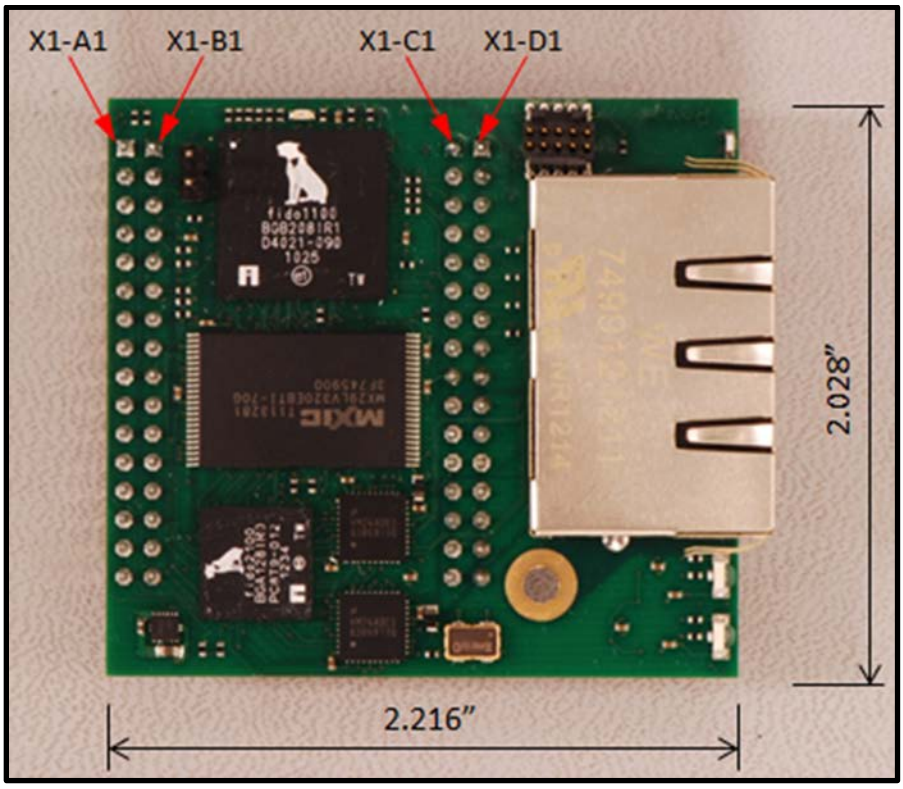

Figure 2 - Dimensions of the DLR Network Interface Module (Plane View)

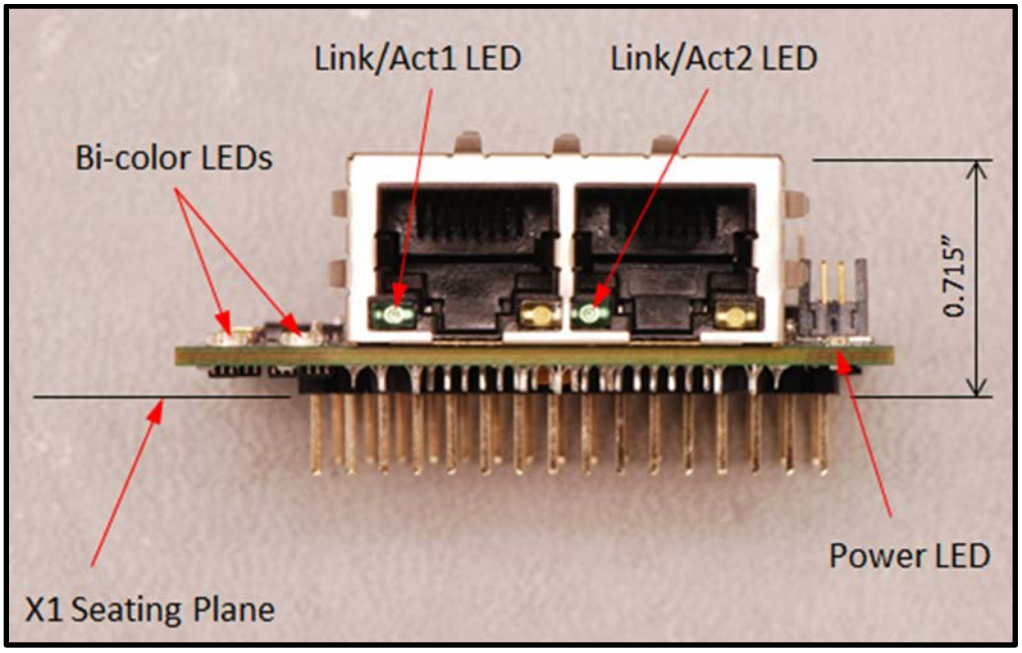

Figure 3 - Dimensions of the DLR Network Interface Module (Cross-section)

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2.2 Signal Interface Connector

The module is installed into the target system using a 64 pin, 0.1” (2,54mm) pitch socket. This socket consists of 4 rows of 16 pins, as shown in Figure 4. The connector reference designator in the DLR Network Interface module schematic is X1. The 4 rows are designated A, B, C and D. Rows A and B are on 0.1” (2,54mm) centers, as are rows C and D. The connector can be implemented by using 2 dual row connectors, 1 for rows A and B, and 1 for rows C and D. The recommended connector for each of these is Samtec part number SSW-116-21-F-D.

The additional plated through hole shown in Figure 4 is a mounting hole. It is connected to chassis ground on the DLR Network Interface module. This plated through hole is a 0.125” (3,175mm) hole with a 0.250” (6,35mm) pad.

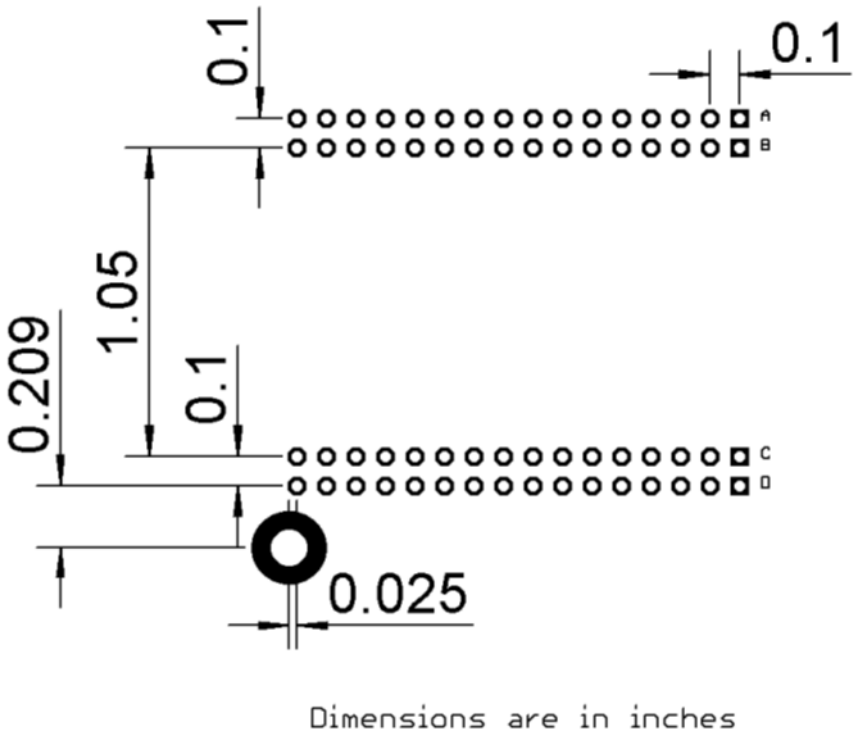

Figure 4 - Socket dimensions to mate the DLR Network Interface Module

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Figure 5 shows the location of the X1 connector relative to the DLR Network Interface board outline. The dimensions are referenced to the center of pin X1-A1 and the upper right corner of the PC board.

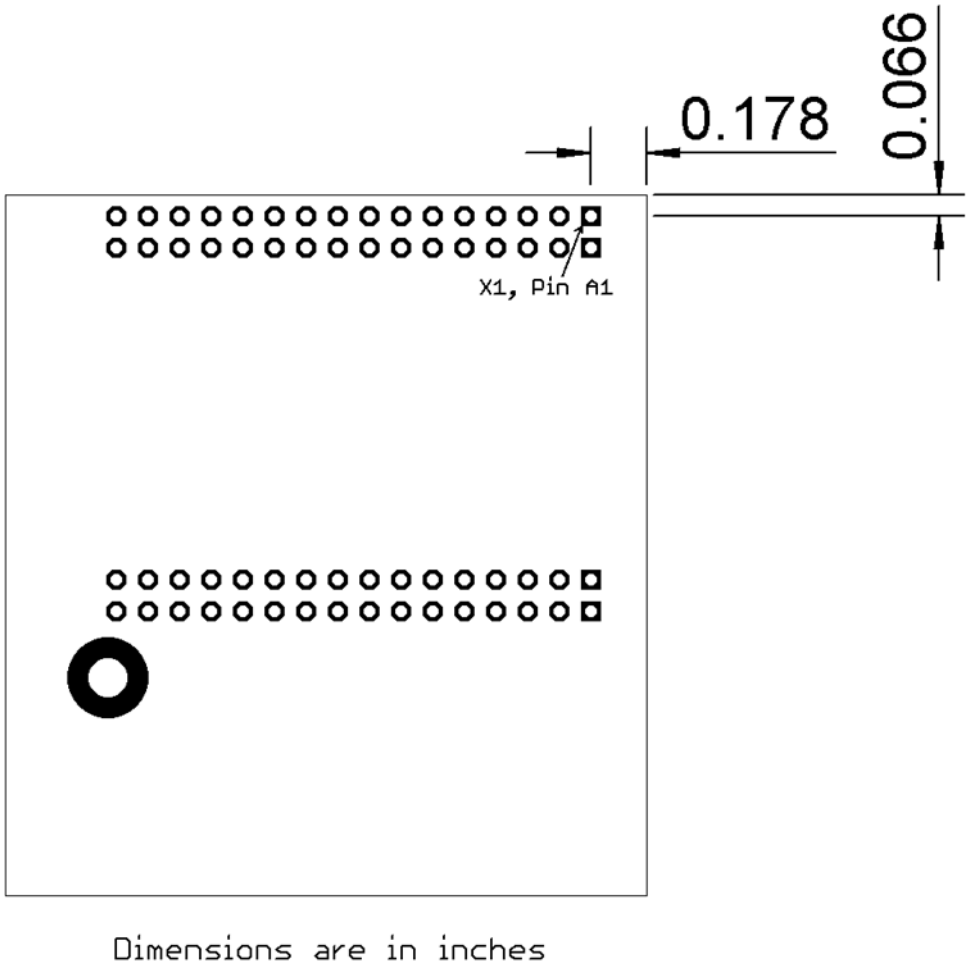

Figure 5 - Location of X1 connector and Pin A1

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2.3 Connector Pinout

A summary on the pinout is shown in Figure 6 and the detailed pin definition is provided in Table 1 through Table 4. All signals are 3.3V logic levels. All inputs **except MAN_RESET_N** are 5 volt tolerant. MAN_RESET_N is **not** 5 volt tolerant, and must be supplied by a +3.3V signal.

Chassis ground is provided on pin X1-C10 for additional shielding of the Ethernet network components.

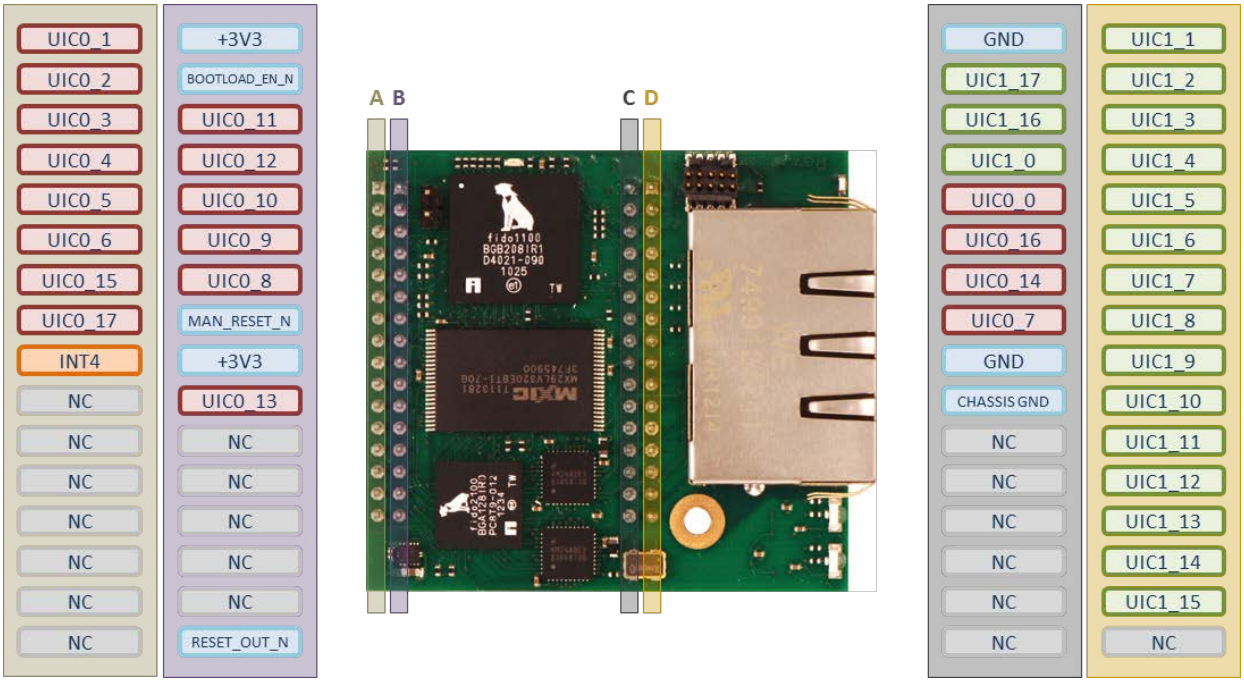

Figure 6 - Summary of Connector Pin Names

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Table 1 – DLR Network Interface Module Connector Pin Definition – X1-A Connector

X1 Pin	Signal Name	Direction	Function
A1	UIC0_1	Input	Write Data Bit 1 for Parallel Host Interface
A2	UIC0_2	Input	Write Data Bit 2 for Parallel Host Interface
A3	UIC0_3	Input	Write Data Bit 3 for Parallel Host Interface
A4	UIC0_4	Input	Write Data Bit 4 for Parallel Host Interface
A5	UIC0_5	Input	Write Data Bit 5 for Parallel Host Interface
A6	UIC0_6	Input	Write Data Bit 6 for Parallel Host Interface
A7	UIC0_15	Input	Write Data Bit 15 for Parallel Host Interface
A8	UIC0_17	Output	“INT4”connection for Parallel Host Interface
A9	INT4	Input	Interrupt 4, has 10K pull-up resistor on module; “USED” for Parallel Host Interface
A10	NC	Not Connected	Do Not Connect
A11	NC	Not Connected	Do Not Connect
A12	NC	Not Connected	Do Not Connect
A13	NC	Not Connected	Do Not Connect
A14	NC	Not Connected	Do Not Connect
A15	NC	Not Connected	Spare pin
A16	NC	Not Connected	Spare pin

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Table 2 – DLR Network Interface Module Connector Pin Definition – X1-B Connector

X1 Pin	Signal Name	Direction	Function
B1	+3V3	Power	+3.3V Power Supply Input
B2	BOOTLOAD_EN_N	Input	Bootload Enable (active low), has 10K pull-up resistor on module
B3	UIC0_11	Input	Write Data Bit 11 for Parallel Host Interface
B4	UIC0_12	Input	Write Data Bit 12 for Parallel Host Interface
B5	UIC0_10	Input	Write Data Bit 10 for Parallel Host Interface
B6	UIC0_9	Input	Write Data Bit 9 for Parallel Host Interface
B7	UIC0_8	Input	Write Data Bit 8 for Parallel Host Interface
B8	MAN_RESET_N	Input	Manual Reset Input to FIDO's supervisor IC (active low); ***Not 5V Tolerant***
B9	+3V3	Power	+3.3V Power Supply Input
B10	UIC0_13	Input	Write Data Bit 13 for Parallel Host Interface
B11	NC	Not Connected	Do Not Connect
B12	NC	Not Connected	Do Not Connect
B13	NC	Not Connected	Do Not Connect
B14	NC	Not Connected	Do Not Connect
B15	NC	Not Connected	Do Not Connect
B16	RESET_OUT_N	Output	FIDO's reset output

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Table 3 – DLR Network Interface Module Connector Pin Definition – X1-C Connector

X1 Pin	Signal Name	Direction	Function
C1	GND	Ground	Signal Ground
C2	UIC1_17	Output	"FIFONOTEMPTY_N" for Parallel Host Interface
C3	UIC1_16	Input	TX for UART Host Interface (Connect to Host RX); or "RD_SEL_N" for Parallel Host Interface
C4	UIC1_0	Output	RX for UART Host Interface (Connect to Host TX); or Read Data Bit 0 for Parallel Host Interface
C5	UIC0_0	Input	Write Data Bit 0 for Parallel Host Interface
C6	UIC0_16	Input	"WR_SEL_N" for Parallel Host Interface
C7	UIC0_14	Output	Write Data Bit 14 for Parallel Host Interface
C8	UIC0_7	Output	Write Data Bit 7 for Parallel Host Interface
C9	GND	Ground	Signal Ground
C10	CHASSIS GND	Chassis Ground	Ethernet line-side isolated ground
C11	NC	Not Connected	Do Not Connect
C12	NC	Not Connected	Do Not Connect
C13	NC	Not Connected	Do Not Connect
C14	NC	Not Connected	Do Not Connect
C15	NC	Not Connected	Do Not Connect
C16	NC	Not Connected	Spare pin

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Table 4 – DLR Network Interface Module Connector Pin Definition – X1-D Connector

X1 Pin	Signal Name	Direction	Function
D1	UIC1_1	Output	Read Data Bit 1 for Parallel Host Interface
D2	UIC1_2	Output	Read Data Bit 2 for Parallel Host Interface
D3	UIC1_3	Output	Read Data Bit 3 for Parallel Host Interface
D4	UIC1_4	Output	Read Data Bit 4 for Parallel Host Interface
D5	UIC1_5	Output	Read Data Bit 5 for Parallel Host Interface
D6	UIC1_6	Output	Read Data Bit 6 for Parallel Host Interface
D7	UIC1_7	Output	Read Data Bit 7 for Parallel Host Interface
D8	UIC1_8	Output	Read Data Bit 8 for Parallel Host Interface
D9	UIC1_9	Output	Read Data Bit 9 for Parallel Host Interface
D10	UIC1_10	Output	Read Data Bit 10 for Parallel Host Interface
D11	UIC1_11	Output	Read Data Bit 11 for Parallel Host Interface
D12	UIC1_12	Output	Read Data Bit 12 for Parallel Host Interface
D13	UIC1_13	Output	Read Data Bit 13 for Parallel Host Interface
D14	UIC1_14	Output	Read Data Bit 14 for Parallel Host Interface
D15	UIC1_15	Output	Read Data Bit 15 for Parallel Host Interface
D16	NC	Not Connected	Spare pin

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2.4 Power requirements

The DLR Network Interface module consumes approximately 1.5W, supplied from a single +3.3V supply. The power supply requirements for voltage and current are +3.3V ± 10%, 500mA. The 3.3V power is supplied to pins X1-B1 and X1-B9 and ground is connected to pins X1-C1 and X1-C9.

2.5 Reset Requirements

The DLR Network Interface module may be reset by the application hardware. Module signal X1-B8, referred to as MAN_RESET_N is the reset input to the DLR Network Interface module. This input is connected to the manual reset input of the on-board reset supervisor (U2). U2 is a TC1270A voltage supervisor chip which requires a low pulse for a minimum of 10uS in order to generate a valid reset.

Since the module does have an on-board supervisor IC, it may be allowed to initialize without an external reset source. Module signal X1-B16, referred to as RESET_OUT_N, is an output that indicates if the module is in a reset state. The signal will go low to indicate the reset state is active.

Regardless of how the module is reset, it will not be available for communication until the software has initialized the module and entered the operating state. The time required for the module to enter the operating state is 1.0 second after the receipt of a valid reset pulse or after power is valid if no external reset source is used.

3. Communication Interfaces between the Host Processor and DLR Network Interface Module

The DLR Network Interface module requires a host processor, and may interface to the host via a UART (serial) or a 16 bit parallel interface. Implementation of each of these interfaces is described in the following paragraphs.

3.1 UART Host Interface

The UART Host Interface is implemented using two pins from the DLR Network Interface. These pins are X1-C3 and X1-C4. The signal names for these pins, as shown in Table 3, are UIC1_16 and UIC1_0, respectively. UIC1_16 is the DLR Network Interface TX signal, and UIC1_0 is the DLR Network Interface RX signal. The DLR Network Interface TX signal must be connected to the Host Processor RX signal, and the DLR Network Interface RX signal must be connected to the Host Processor TX signal. Figure 7 provides an overview of these signal connections.

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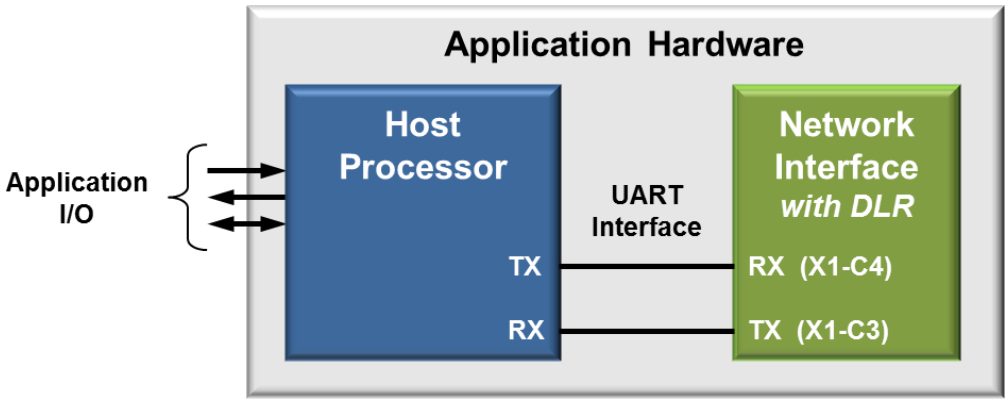

Figure 7 – UART Host Interface Connection

3.2 Parallel Host Interface

The Parallel Host Interface is implemented as a 16-bit read FIFO and a 16-bit write FIFO. Support circuitry between the Host Processor and DLR Network Interface is required and must be designed into the application hardware. The host processor connects to a 16-bit data bus and must use 4 control signals to either read data from the DLR Network Interface or write data to the DLR Network Interface. The DLR Network Interface connects to a 16-bit write data bus, a 16-bit read data bus, and 5 control signals. Figure 8 provides an overview of these connections.

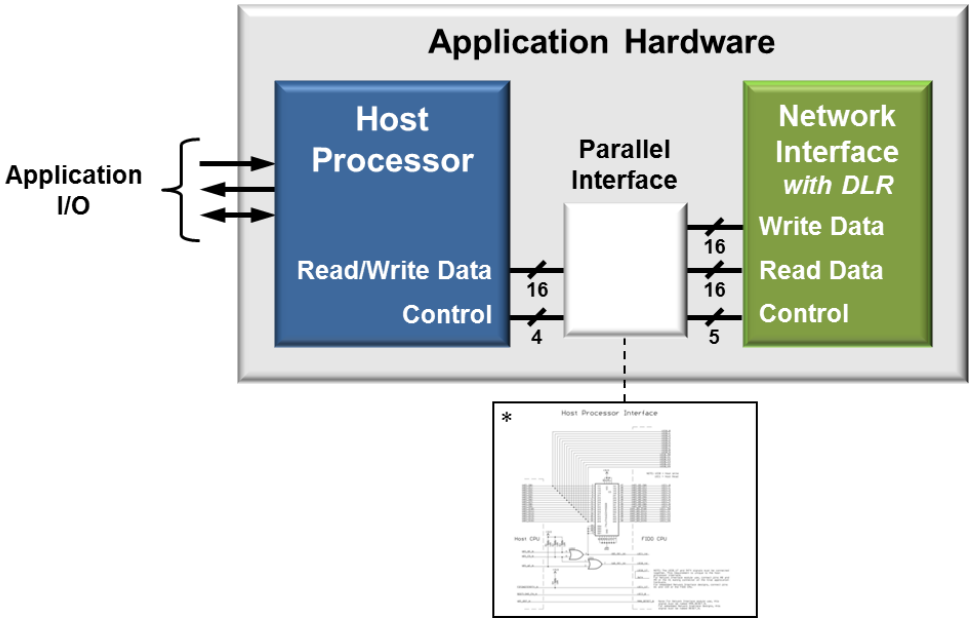

Figure 8 – Parallel Host Interface Connection

Refer to the "HPI Personality Module" schematic (SCH-NI_100-EDB-001) for details on the circuitry required for the Parallel Host Interface. Table 1 through Table 4 may be used to

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understand the signal names in the schematic. The 16-bit data bus on the host side of the interface is referred to as HPI_D0 through HPI_D15. The four control signals are referred to as HPI_OE_N, HPI_CS_N, HPI_WE_N, and FIFONOTEMPTY_N. As noted in the schematics, it is important that signal pins X1-A9 and X1-A8 on the DLR Network Interface connector be tied together when integrating the module on the application hardware.

Refer to the "Host Processor Interface User Guide.pdf" for a detailed description of the Parallel Host Interface. These documents are found on the DLR Network Interface Tools page in the Developer Portal on the Innovasic website.

4. Considerations for Production and Maintenance

There are three methods for configuring and programming the DLR Network Interface during production of end use systems. These methods are:

1. **Bootloader**
2. **JTAG**
3. **Flash Programmer**

The Bootloader and JTAG methods can also be used to perform field updates during maintenance for the end devices. The subparagraphs below provide an overview of these methods. Figure 9 shows the connections and devices involved for all three methods for either a module or embedded design.

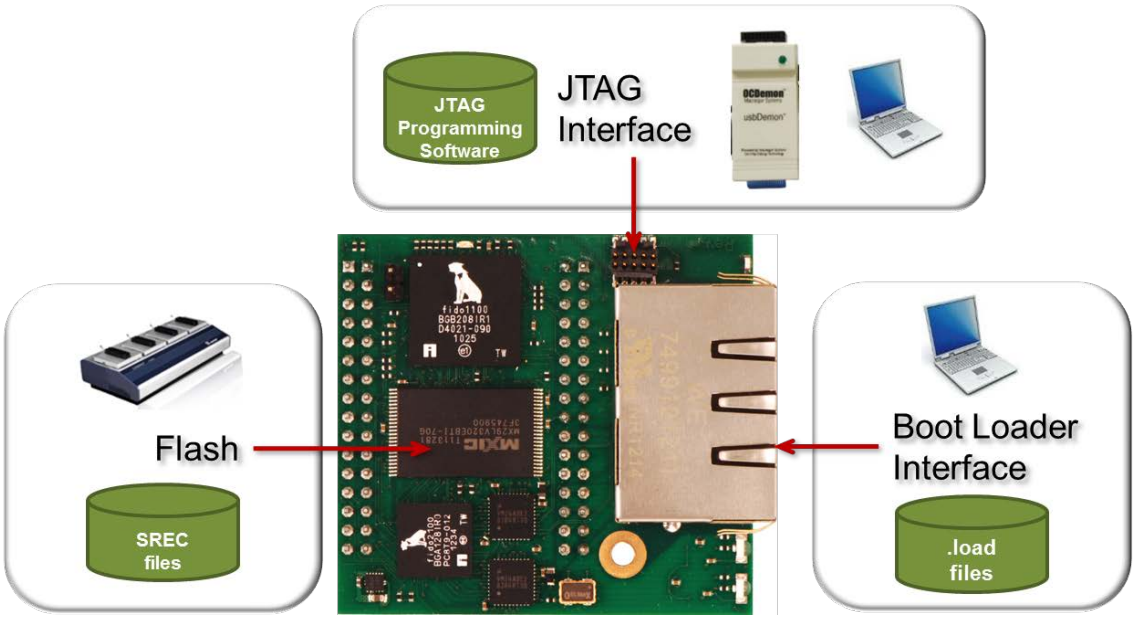

Figure 9 – Programming Connections and Devices

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4.1 Boot Loader

Innovasic supports programming flash chips on the DLR Network Interface module or embedded design using the Ethernet Connector. The type of programming file used to support this is called a .load file. Innovasic supplies .load files for each software component in the DLR Network Interface. These components are identified as:

- Boot Loader
- Unified Interface
- Network
- Configuration Data

These .load file types are available on the DLR Network Interface Software page in the Developer Portal on the Innovasic website, and can be loaded as described in the "Boot Loader User Guide.pdf".

It is important to note that the BOOTLOADER_EN_N signal **must be** grounded when the DLR Network Interface powers-up in order to enter the programming mode. This is an important consideration if end use device requires field updates.

4.2 JTAG

Innovasic supports programming flash chips on the DLR Network Interface module or embedded design using the JTAG Connector. The type of programming file used to support this is called a .elf file. Innovasic supplies .elf files for each software component in the DLR Network Interface. These components are identified as:

- Boot Loader
- Unified Interface
- Network
- Configuration Data

These .elf file types are available on the DLR Network Interface Software page in the Developer Portal on the Innovasic website.

Using the JTAG method for configuring and programing the DLR Network Interface requires a PC, JTAG "wiggler" and programming software, and .elf programming files. The wiggler and programming software may be ordered from Innovasic using part number "RapID-PGMR VMCGR".

A connector compatible with the ribbon-cable side of the wiggler is already installed on the module as shown in Figure 9. This connector must be used in the embedded design. The ribbon cable on the wiggler connects to the module/embedded design connector. The other end of the

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wiggler connects to the USB port of the PC. Detailed instructions for loading and programming with the .elf files are provided with the JTAG programming software.

Note that it is possible to program blank flash using the JTAG method. This method is useful if a Flash Programmer is not available. Access to the JTAG connector is required; however, grounding BOOTLOADER_EN_N is not required.

4.3 Flash Programmer

Innovasic supports programming individual, blank flash chips using a flash programmer. The type of programming file used to support this is called a Motorola S record file (.srec). Innovasic supplies .srec files for each software component in the DLR Network Interface. These components are identified as:

- Boot Loader
- Unified Interface
- Network
- Configuration Data

These .srec file types are available in the Developer Portal on the Innovasic website, and can be sequentially loaded into the flash programmer. There is no need to be concerned the data will overlap. Once the files are loaded into the programmer the complete executable package can be programmed into the flash chip.

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5. For Additional Information

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6. Revision History

Table 5 – Document Revision History for IA211130109

Date	Revision	Description	Page(s)
January 9, 2013	00	Initial release	NA

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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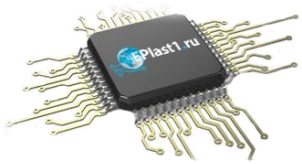
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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