10–810 MHz I²C Programmable XO/VCXO

Features

- I²C programmable output frequencies from 10 to 810 MHz
- 0.5 ps RMS phase jitter
- Superior power supply rejection: 0.3–0.4 ps additive jitter
- Available LVPECL, CMOS, LVDS, and CML outputs
- 1.8, 2.5, or 3.3 V supply
- Pin- and register-compatible with Si570/571
- Programmable with 28 parts per trillion frequency resolution
- Integrated crystal provides stability and low phase noise
- Frequency changes up to ±3500 ppm are glitchless
- –40 to 85 °C operation
- Industry-standard 5x7 mm package

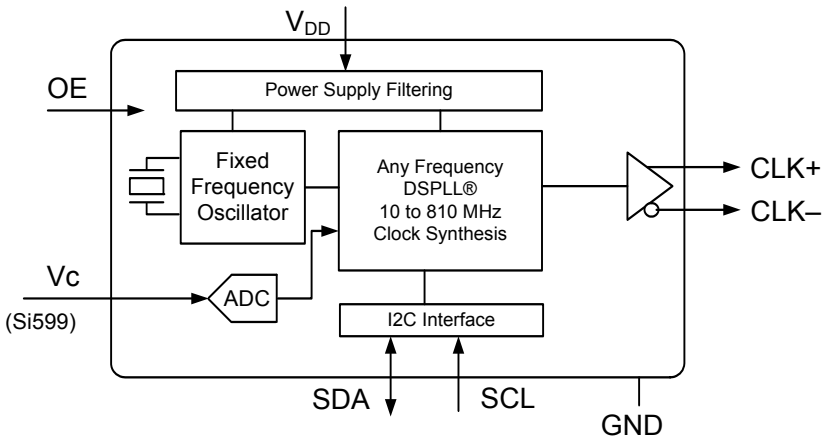
Applications

- SONET / SDH / xDSL
- Ethernet / Fibre Channel
- 3G SDI / HD SDI
- Multi-rate PLLs
- Multi-rate reference clocks
- Frequency margining
- Digital PLLs
- CPU / FPGA FIFO control
- Adaptive synchronization
- Agile RF local oscillators

Description

The Si598 XO/Si599 VCXO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low-jitter clock at any frequency. They are user-programmable to any output frequency from 10 to 810 MHz with 28 parts per trillion (PPT) resolution. The device is programmed via a 2-pin I²C compatible serial interface. The wide frequency range and ultra-fine programming resolution make these devices ideal for applications that require in-circuit dynamic frequency adjustments or multi-rate operation with non-integer related rates. Using an integrated crystal, these devices provide stable low jitter frequency synthesis and replace multiple XOs, clock generators, and DAC controlled VCXOs.

Functional Block Diagram



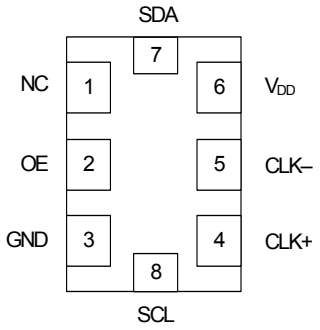
Ordering Information:

See page 21.

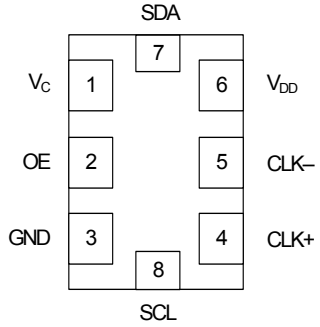
Pin Assignments:

See page 20.

(Top View)



Si598



Si599

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1. Detailed Block Diagrams

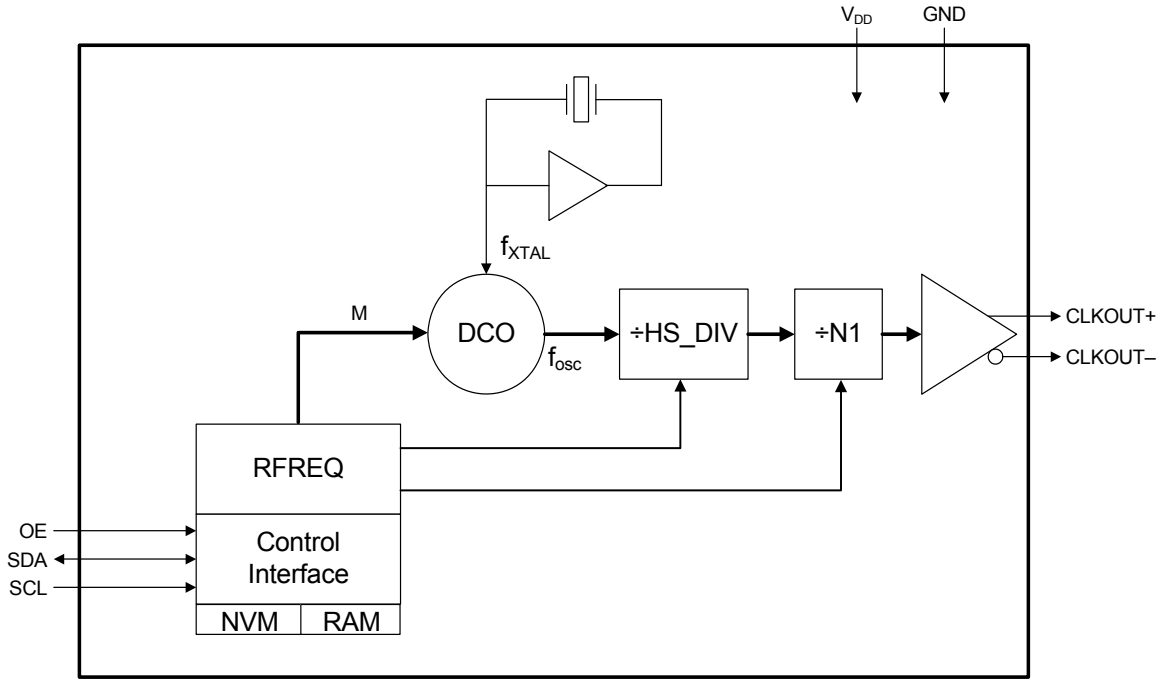


Figure 1. Si598 Detailed Block Diagram

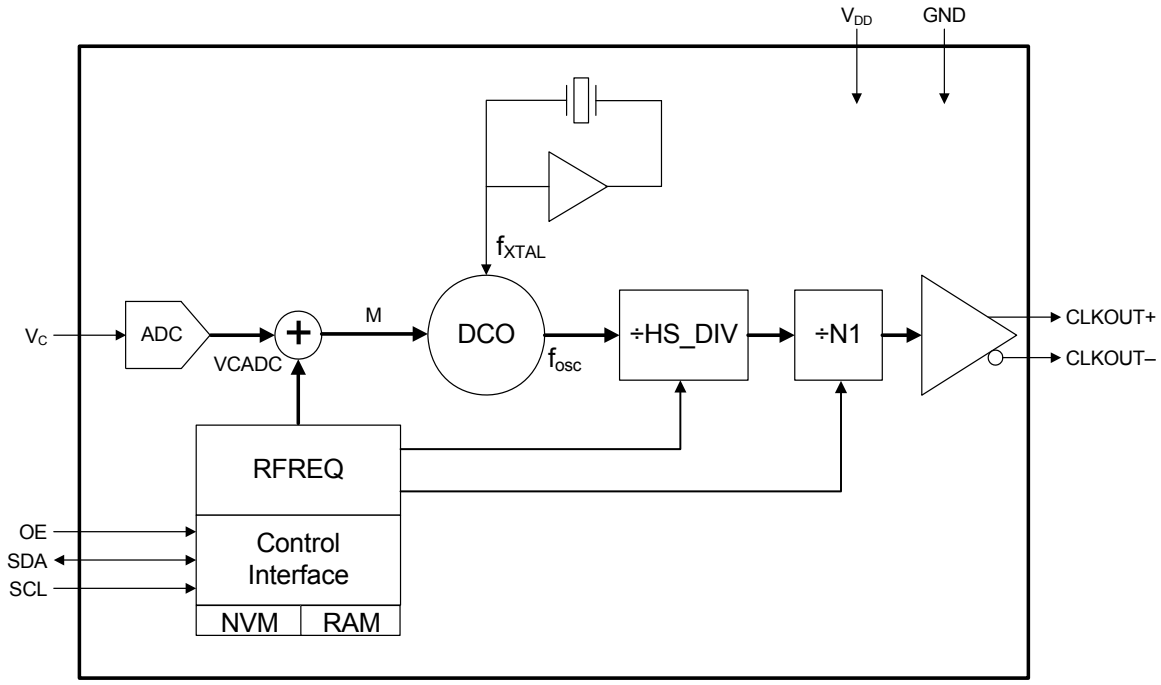


Figure 2. Si599 Detailed Block Diagram

2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	I_{DD}	Output enabled LVPECL CML LVDS CMOS	 — — — —	 120 108 99 90	 130 120 110 100	 mA mA mA mA
		Tristate mode	—	60	75	mA
Output Enable (OE)[2], Serial Data (SDA), Serial Clock (SCL)		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	V
Operating Temperature Range	T_A		–40	—	85	ºC

Notes:
1. Selectable parameter specified by part number. See Section 7. Ordering Information on page 21 for further details.
2. OE pin includes a 17 kΩ pullup resistor to V_{DD} for OE Active High Option. OE pin includes 17 kΩ pull down for OE Active Low. See Section “7.Ordering Information”.

Table 2. V_C Control Voltage Input (Si599)

(Typical values TA = 25 ºC, V_{DD} = 3.3 V, min/max limits VDD = 1.8 ±5%, 2.5 or 3.3 V ±10%, TA = –40 to 85 ºC unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope[1,2,3]	K_V	10 to 90% of V_{DD}	— — — — —	45 95 125 185 380	— — — — —	ppm/V ppm/V ppm/V ppm/V ppm/V
Control Voltage Linearity[4]	L_{VC}	BSL	–5	±1	+5	%
		Incremental	–10	±5	+10	%
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V_C Input Impedance	Z_{VC}		500	—	—	kΩ
V_C Input Capacitance	C_{VC}		—	50	—	pF
Nominal Control Voltage	V_{CNOM}	@ f_O	—	$V_{DD}/2$	—	V
Control Voltage Tuning Range	V_C		0	—	V_{DD}	V

Notes:
1. Positive slope; selectable option by part number. See 7. Ordering Information on page 21.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application’s minimum APR requirements. See “AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)” for more information.
3. K_V variation is ±10% of typical values.
4. BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope determined with V_C ranging from 10 to 90% of V_{DD}.

Table 3. CLK± Output Frequency Characteristics

(Typical values TA = 25 ºC, V_{DD}= 3.3 V, min/max limits VDD = 1.8 ±5%, 2.5 or 3.3 V ±10%, TA = –40 to 85 ºC unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Programmable Frequency Range[1,2,3]	f_O	LVPECL/LVDS/CML	10	—	810	MHz
		CMOS	10	—	160	MHz
Total Stability (Si598)[1,2,4,5]		Temp stability = ±20 ppm	—	—	±30	ppm
		Temp stability = ±25 ppm	—	—	±50	ppm
		Temp stability = ±50 ppm	—	—	±100	ppm
Temperature Stability (Si599)[1,5]		T_A = –40 to +85 ºC	–20 –50	— —	+20 +50	ppm
Absolute Pull Range[1,5] (Si599)	APR		±10	—	±370	ppm
Powerup Time[6]	t_{OSC}		—	—	10	ms

Notes:

1. See Section 7. Ordering Information on page 21 for further details.
2. Specified at time of order by part number. Three frequency grades are available:
   Grade A covers 10 to 810 MHz.
   Grade B covers 10 to 280 MHz.
   Grade C covers 10 to 160 MHz.
3. Nominal output frequency set by V_{CNOM} = 1/2 x V_{DD}.
4. Includes initial accuracy, temperature drift, shock, vibration, power supply and load drift. ±100 ppm and ±50 ppm options include 15 years aging at 70 °C. ±30 ppm option includes 10 years aging at 40 °C.
5. Selectable parameter specified by part number. See 7. Ordering Information on page 21.
6. Time from power up or tristate mode to f_O.

Table 4. CLK± Output Levels and Symmetry

(Typical values TA = 25 ºC, V_{DD} = 3.3 V, min/max limits VDD = 1.8 ±5%, 2.5 or 3.3 V ±10%, TA = –40 to 85 ºC unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option[2]	V_O	2.5/3.3 V option mid-level	—	V_{DD} – 1.30	—	V
		1.8 V option mid-level	—	V_{DD} – 0.36	—	V
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V_{PP}
		1.8 V option swing (diff)	0.35	0.425	0.50	V_{PP}
CMOS Output Option[3]	V_{OH}	I_{OH} = 32 mA	0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}	I_{OL} = 32 mA	—	—	0.4	V
Rise/Fall Time (20/80 %)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C_L = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V_{DD}/2	48	—	52	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF sinking or sourcing 12 mA for V_{DD} = 3.3 V, 6 mA for V_{DD} = 2.5 V, 3 mA for V_{DD} = 1.8 V.

Table 5. CLK± Output Phase Jitter (Si598)

(Typical values TA = 25 ºC, V_{DD} = 3.3 V, min/max limits VDD = 1.8 ±5%, 2.5 or 3.3 V ±10%, TA = –40 to 85 ºC unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS Random) 12 kHz to 20 MHz Integration Bandwidth	$\varphi_{J\text{-RANDOM}}$	LVPECL/LVDS/CML[1]	—	0.5	—	ps
		CMOS 3.3 V[2]	—	0.6	—	ps
Phase Jitter (RMS Random) 1.875 to 20 MHz Integration Bandwidth		LVPECL/LVDS/CML[1]	—	0.3	—	ps
		CMOS 3.3 V[2]	—	0.5	—	ps
Phase Jitter (RMS) 12 kHz to 20 MHz Integration Bandwidth	φ_J	LVPECL/LVDS/CML[1]	—	0.5	1	ps
		CMOS 3.3 V[2]	—	0.6	1	ps
Phase Jitter (RMS) 1.875 to 20 MHz Integration Bandwidth		LVPECL/LVDS/CML[1]	—	0.5	—	ps
		CMOS 3.3 V[2]	—	0.5	—	ps

Notes:
1. 50 to 810 MHz, 3.3 V/2.5 V only.
2. 50 to 160 MHz, single-ended CMOS output phase jitter measured using 33 Ω series termination into 50 Ω phase noise test equipment. 3.3 V supply voltage option only.

Table 6. CLK± Output Phase Jitter (Si599)

(Typical values TA = 25 ºC, V_{DD} = 3.3 V, min/max limits VDD = 1.8 ±5%, 2.5 or 3.3 V ±10%, TA = –40 to 85 ºC unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2] for F_{OUT} of 50 MHz ≤ F_{OUT} 810 MHz	ϕ_J	Kv = 45 ppm/V 12 kHz to 20 MHz	—	0.5	—	ps
		Kv = 95 ppm/V 12 kHz to 20 MHz	—	0.5	—	ps
		Kv = 125 ppm/V 12 kHz to 20 MHz	—	0.5	—	ps
		Kv = 185 ppm/V 12 kHz to 20 MHz	—	0.5	—	ps
		Kv = 380 ppm/V 12 kHz to 20 MHz	—	0.7	—	ps

Notes:
1. Differential Modes: LVPECL/LVDS/CML.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.

Table 7. CLK± Output Period Jitter

(Typical values TA = 25 ºC, V_{DD} = 3.3 V unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J_{PER}	RMS	—	3	—	ps
		Peak-to-Peak	—	35	—	ps
***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles.						

Table 8. CLK± Output Phase Noise (Typical, Si599)

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Offset Frequency	74.25 MHz 185 ppm/V LVPECL	148.5 MHz 185 ppm/V LVPECL	155.52 MHz 95 ppm/V LVPECL	Units
100 Hz	–77	–68	–77	dBc/Hz
1 kHz	–101	–95	–101	dBc/Hz
10 kHz	–121	–116	–119	dBc/Hz
100 kHz	–134	–128	–127	dBc/Hz
1 MHz	–149	–144	–144	dBc/Hz
10 MHz	–151	–147	–147	dBc/Hz
20 MHz	–150	–148	–148	dBc/Hz

Table 9. Power Supply Noise Rejection

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
RMS Additive Jitter due to Power Supply Noise*	φ_{PSRR}	100 kHz	—	0.32	—	ps
		300 kHz	—	0.36	—	ps
		700 kHz	—	0.36	—	ps
		1 MHz	—	0.32	—	ps
***Note:** Measured with 100 mVp-p sinusoid applied to power supply pin. VDD = 3.3 V, LVPECL.						

Table 10. Spurious Performance

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Spurious Free Dynamic Range	SFDR	LVPECL, LVDS, CML[1]	—	75	—	dB
		LVPECL, LVDS, CML[2]	—	64	—	dB
		CMOS[1]	—	77	—	dB

Notes:
1. 10 to 160 MHz.
2. 10 to 810 MHz.

Table 11. Environmental Compliance

The Si598/599 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross & Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	J-STD-020, MSL1
Contact Pads	Gold over Nickel

Table 12. Programming Constraints and Timing

(Typical values TA = 25 ºC, VDD = 3.3 V, min/max limits VDD = 1.8 ±5%, 2.5 or 3.3 V ±10%, TA = –40 to 85 ºC unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequency Range	CKO_F		10	—	810	MHz
Frequency Reprogramming Resolution	M_{RES}		—	28	—	ppt
Internal Oscillator Frequency	f_{OSC}		4850	—	5670	MHz
Internal Crystal Frequency Accuracy	f_{XTAL}	Maximum variation is ±2000 ppm	—	39.17	—	MHz
Delta Frequency for Continuous Output		From center frequency	–3500	—	+3500	ppm
Unfreeze to NewFreq Timeout*					10	ms
Settling Time for Small Frequency Change		<±3500 ppm from center frequency	—	—	100	µs
Settling Time for Large Frequency Change		>±3500 ppm from center frequency after setting NewFreq bit	—	—	10	ms

***Note:** Applies when using large frequency change procedure outlined in section “3.1.2.Reconfiguring the Output Clock for Large Changes in Output Frequency”.

Table 13. Thermal Characteristics

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	84.6	—	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	38.8	—	°C/W
Ambient Temperature	T_A		–40	—	85	°C
Junction Temperature	T_J		—	—	125	°C

Table 14. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage, 1.8 V Option	V_{DD}	–0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V_{DD}	–0.5 to +3.8	V
Input Voltage	V_I	–0.5 to V_{DD} + 0.3	V
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2000	V
Soldering Temperature (lead-free profile)	T_{PEAK}	260	ºC
Soldering Temperature Time @ T_{PEAK} (lead-free profile)	t_P	20–40	seconds

Notes:

1. Stresses beyond the absolute maximum ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at www.silabs.com/VCXO for further information, including soldering profiles.

3. Functional Description

The Si598 XO and the Si599 VCXO are low-jitter oscillators ideally suited for applications requiring programmable frequencies. The Si59x can be programmed to generate any output clock in the range of 10 to 810 MHz with frequency resolution of 30 parts per trillion. Output jitter performance exceeds the strict requirements of high-speed communication systems including OC-48/STM-16, 3G SDI, and Gigabit Ethernet.

The Si59x consists of a digitally-controlled oscillator (DCO) based on Silicon Laboratories' third-generation DSPLL technology, which is driven by an internal fixed-frequency crystal reference.

The device's default output frequency is set at the factory and can be reprogrammed through the two-wire I^2C serial port. Once the device is powered down, it will return to its factory-set default output frequency.

The Si599 has a pullable output frequency using the voltage control input pin. This makes the Si599 an ideal choice for high-performance, low-jitter, phase-locked loops. The Si598 is digitally pullable using the I^2C interface and is ideal for digital PLL applications.

3.1. Programming a New Output Frequency

The output frequency (f_{out}) is determined by programming the DCO frequency (f_{DCO}) and the device's output dividers (HS_DIV, N1). The output frequency is calculated using the following equation:

$$f_{out} = \frac{f_{DCO}}{\text{Output Dividers}} = \frac{f_{XTAL} \times RFREQ}{HSDIV \times N1}$$

The DCO frequency is adjustable in the range of 4.85 to 5.67 GHz by setting the high-resolution 38-bit fractional multiplier (RFREQ). The DCO frequency is the product of the internal fixed-frequency crystal (f_{XTAL}) and RFREQ.

The 38-bit resolution of RFREQ allows the DCO frequency to have a programmable frequency resolution of 28 ppt.

As shown in Figure 3, the device allows reprogramming of the DCO frequency up to ±3500 ppm from the center frequency configuration without interruption to the output clock. Changes greater than the ±3500 ppm window will cause the device to recalibrate its internal tuning circuitry, forcing the output clock to momentarily stop and start at any arbitrary point during a clock cycle. This re-calibration process establishes a new center frequency and can take up to 10 ms. Circuitry receiving a clock from the Si59x device that is sensitive to glitches or runt pulses may have to be reset once the recalibration process is complete.

3.1.1. Reconfiguring the Output Clock for a Small Change in Frequency

For output changes less than ±3500 ppm from the center frequency configuration, the DCO frequency is the only value that needs reprogramming. Since $f_{DCO} = f_{XTAL}$ x RFREQ, and that f_{XTAL} is fixed, changing the DCO frequency is as simple as reconfiguring the RFREQ value as outlined below:

1. Using the serial port, read the current RFREQ value (registers 0x08–0x12).
2. Calculate the new value of RFREQ given the change in frequency.

$$RFREQ_{new} = RFREQ_{current} \times \frac{f_{out\_new}}{f_{out\_current}}$$

3. Using the serial port, write the new RFREQ value (registers 0x08—0x12). Multi-byte changes to RFREQ can freeze the DCO to avoid unintended RFREQ values.

Example:

An Si598 generating a 148.35 MHz clock must be reconfigured "on-the-fly" to generate a 148.5 MHz clock. This represents a change of +1011.122 ppm, which is well within the ±3500 ppm window.

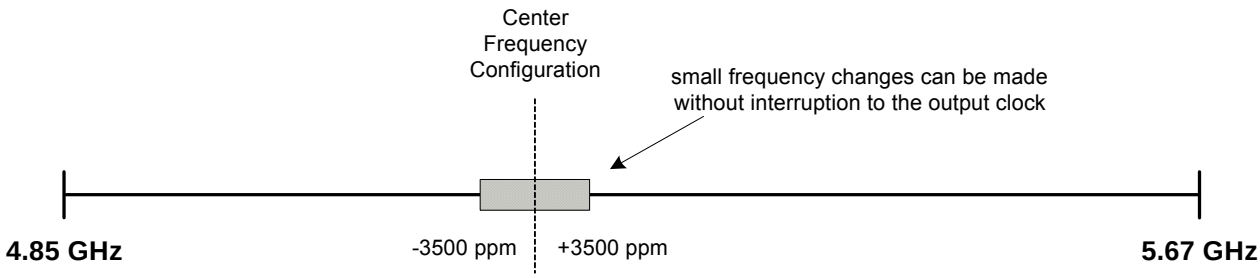


Figure 3. DCO Frequency Range

A typical frequency configuration for this example:

$RFREQ_{current}$ = 0x8858199E9

$F_{out\_current}$ = 148.35 MHz

F_{out_new} = 148.50 MHz

Calculate $RFREQ_{new}$ to change the output frequency from 148.35 to 148.5 MHz:

$$RFREQ_{new} = 0x8858199E9 \times \frac{148.50\ MHz}{148.35\ MHz}$$

$$= 0x887B6473C$$

Note that performing calculations with RFREQ requires a minimum of 38-bit arithmetic precision.

Relatively small changes in output frequency may require writing more than one RFREQ register. Such multi-register RFREQ writes can impact the output clock frequency on a register-by-register basis during updating.

Interim changes to the output clock during RFREQ writes can be prevented by using the following procedure:

1. Freeze the "M" value (Set Register 135 bit 5 = 1)
2. Write the new frequency configuration (RFREQ)
3. Unfreeze the "M" value (Set Register 135 bit 5 = 0)

3.1.2. Reconfiguring the Output Clock for Large Changes in Output Frequency

For output frequency changes outside of ±3500 ppm from the center frequency, it is likely that both the DCO frequency and the output dividers need to be reprogrammed. Note that changing the DCO frequency outside of the ±3500 ppm window will cause the output to momentarily stop and restart at any arbitrary point in a clock cycle. Devices sensitive to glitches or runt pulses may have to be reset once reconfiguration is complete.

The process for reconfiguring the output frequency outside of a ±3500 ppm window is shown below:

1. Using the serial port, read the current values for RFREQ, HSDIV, and N1.
2. Calculate f_{XTAL} for the device. Note that because of slight variations of the internal crystal frequency from one device to another, each device may have a different RFREQ value or possibly even different HSDIV or N1 values to maintain the same output frequency. It is necessary to calculate f_{XTAL} for each device.

$$f_{XTAL} = \frac{F_{out} \times HSDIV \times N1}{RFREQ}$$

Once f_{XTAL} has been determined, new values for RFREQ, HSDIV, and N1 are calculated to generate a new output frequency (f_{out_new}). New values can be calculated manually or with the Si59x-EVB software, which provides a user-friendly application to help find the optimum values.

The first step in manually calculating the frequency configuration is to determine new frequency divider values (HSDIV, N1). Given the desired output frequency (f_{out_new}), find the frequency divider values that will keep the DCO oscillation frequency in the range of 4.85 to 5.67 GHz.

$$f_{DCO\_new} = f_{out\_new} \times HSDIV_{new} \times N1_{new}$$

Valid values of HSDIV are 9 or 11. N1 can be selected as 1 or any even number up to 128 (i.e., 1, 2, 4, 6, 8, 10 … 128). To help minimize the device's power consumption, the divider values should be selected to keep the DCO's oscillation frequency as low as possible. The lowest value of N1 with the highest value of HS_DIV also results in the best power savings.

Once HS_DIV and N1 have been determined, the next step is to calculate the reference frequency multiplier (RFREQ).

$$RFREQ_{new} = \frac{f_{DCO\_new}}{f_{XTAL}}$$

RFREQ is programmable as a 38-bit binary fractional frequency multiplier with the first 10 most significant bits (MSBs) representing the integer portion of the multiplier and the 28 least significant bits (LSBs) representing the fractional portion.

Before entering a fractional number into the RFREQ register, it must be converted to a 38-bit integer using a bitwise left shift operation by 28 bits, which effectively multiplies RFREQ by 2^{28}.

Example:

RFREQ = 136.3441409d

Multiply RFREQ by 2^{28} = 36599601635.42d

Discard the fractional portion = 36599601635d

Convert to hexadecimal = 0x8858199E9

Once the new values for RFREQ, HSDIV, and N1 are determined, they can be written directly into the device from the serial port using the following procedure:

1. Freeze the DCO (bit 4 of Register 137)
2. Write the new frequency configuration (RFREQ, HS_DIV, N1)

3. Unfreeze the DCO and assert the NewFreq bit (bit 6 of Register 135) within the maximum Unfreeze to NewFreq Timeout in Table 12, “Programming Constraints and Timing,” on page 9.

The process of freezing and unfreezing the DCO will cause the output clock to momentarily stop and start at any arbitrary point during a clock cycle. This process can take up to 10 ms. Circuitry that is sensitive to glitches or runt pulses may have to be reset after the new frequency configuration is written.

Example:

An Si598 generating 156.25 MHz must be re-configured to generate a 161.1328125 MHz clock (156.25 MHz x 66/64). This frequency change is greater than ±3500 ppm.

f_{out} = 156.25 MHz

Read the current values for RFREQ, HS_DIV, N1:

$RFREQ_{current}$ = 0x7FA611E85 = 34265439877d, 34265439877d / 2^{28} = 127.64871074631810d

HS_DIV = 4

N1 = 8

Calculate f_{XTAL}, $f_{DCO\_current}$

$$f_{DCO\_current} = f_{out} \times HSDV \times N1 = 5.000000000\ GHz$$

$$f_{XTAL} = \frac{f_{DCO\_current}}{RFREQ_{current}} = 39.17\ MHz$$

Given f_{out_new} = 161.1328125 MHz, choose output dividers that will keep f_{DCO} within the range of 4.85 to 5.67 GHz. In this case, keeping the same output dividers will still keep f_{DCO} within its range limits:

$$f_{DCO\_new} = f_{out\_new} \times HSDV_{new} \times N1_{new}$$

$$= 161.1328125\ MHz \times 4 \times 8 = 5.156250000\ GHz$$

Calculate the new value of RFREQ given the new DCO frequency:

$$RFREQ_{new} = \frac{f_{DCO\_new}}{f_{XTAL}} = 131.637733d = 0x83A342779$$

3.2. I²C Interface

The control interface to the Si598 is an I²C-compatible 2-wire bus for bidirectional communication. The bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL). Both lines must be connected to the positive supply via an external pullup.Fast mode operation is supported for transfer rates up to 400 kbps as specified in the I²C-Bus Specification standard.

Figure 4 shows the command format for both read and write access. Data is always sent MSB. Data length is 1 byte. Read and write commands support 1 or more data bytes as illustrated. The master must send a Not Acknowledge and a Stop after the last read data byte to terminate the read command. The timing specifications and timing diagram for the I²C bus can be found in the I²C-Bus Specification standard (fast mode operation). The device I²C address is specified in the part number.

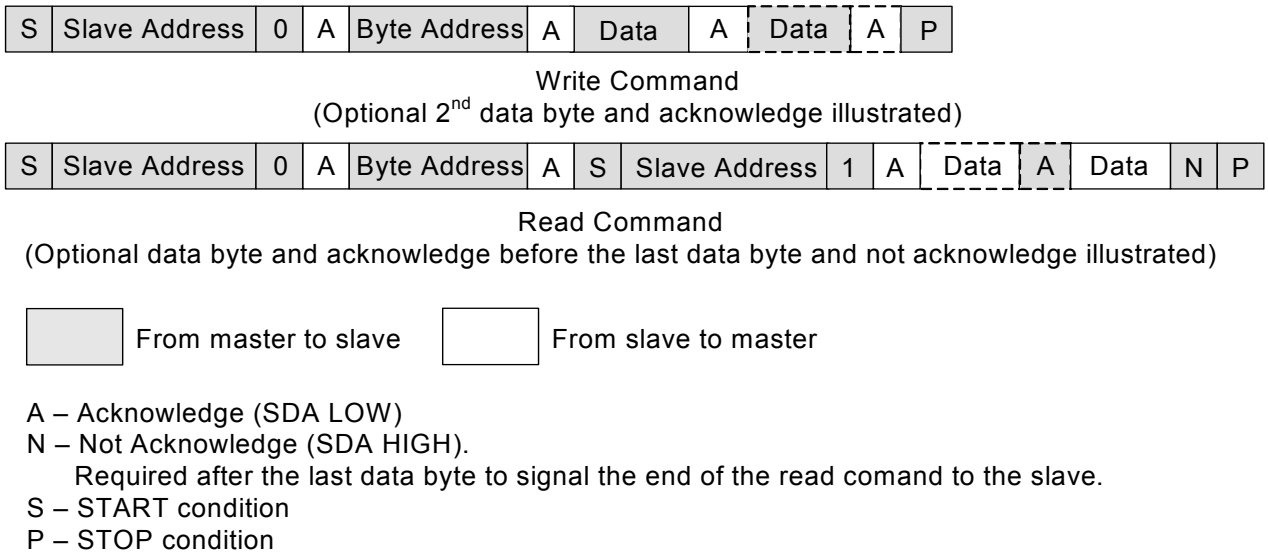


Figure 4. I²C Command Format

4. Serial Port Registers

Note: Registers not documented are reserved. Values within reserved registers and reserved bits must not be changed.

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7	High Speed/ N1 Dividers	HS_DIV[2:0]			N1[6:2]				
8	Reference Frequency	N1[1:0]		RFREQ[37:32]					
9	Reference Frequency	RFREQ[31:24]							
10	Reference Frequency	RFREQ[23:16]							
11	Reference Frequency	RFREQ[15:8]							
12	Reference Frequency	RFREQ[7:0]							
135	NewFreq/ Freeze/ Memory Control	Reserved	NewFreq	Freeze M	Freeze VCADC	Reserved			RECALL
137	Freeze DCO	Reserved			Freeze DCO	Reserved			

Register 7. High Speed/N1 Dividers

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HS_DIV[2:0]			N1[6:2]				
Type	R/W			R/W				

Bit	Name	Function
7:5	HS_DIV[2:0]	**DCO High Speed Divider.** Sets value for high speed divider that takes the DCO output f_{OSC} as its clock input. 000 = 4 001 = 5 010 = 6 011 = 7 100 = Not used. 101 = 9 110 = Not used. 111 = 11
4:0	N1[6:2]	**CLKOUT Output Divider.** Sets value for CLKOUT output divider. Allowed values are [1] and [2, 4, 6, ..., 2^7]. Illegal odd divider values will be rounded up to the nearest even value. The value for the N1 register can be calculated by taking the divider ratio minus one. For example, to divide by 10, write 0001001 (9 decimal) to the N1 registers. 0000000 = 1 1111111 = 2^7

Register 8. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1[1:0]		RFREQ[37:32]					
Type	R/W		R/W					

Bit	Name	Function
7:6	N1[1:0]	**CLKOUT Output Divider.** Sets value for CLKOUT output divider. Allowed values are [1] and [2, 4, 6, ..., 2^7]. Illegal odd divider values will be rounded up to the nearest even value. The value for the N1 register can be calculated by taking the divider ratio minus one. For example, to divide by 10, write 0001001 (9 decimal) to the N1 registers. 0000000 = 1 1111111 = 2^7
5:0	RFREQ[37:32]	**Reference Frequency.** Frequency control input to DCO.

Register 9. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[31:24]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[31:24]	**Reference Frequency.** Frequency control input to DCO.

Register 10. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[23:16]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[23:16]	**Reference Frequency.** Frequency control input to DCO.

Register 11. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[15:8]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[15:8]	**Reference Frequency.** Frequency control input to DCO.

Register 12. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[7:0]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[7:0]	**Reference Frequency.** Frequency control input to DCO.

Register 135. NewFreq/Freeze/Memory Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		NewFreq	Freeze M	Freeze VCADC				RECALL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00xxxx00

Bit	Name	Function
7	Reserved	This bit should read 0 in normal operation.
6	NewFreq	**New Frequency Applied.** Alerts the DSPLL that a new frequency configuration has been applied. This bit will clear itself when the new frequency is applied. Write 0x40 to this register to assert NewFreq.
5	Freeze M	**Freezes the M Control Word.** Prevents interim frequency changes when writing RFREQ registers.
4	Freeze VCADC	**Freezes the VCDADC Output Word.** May be used to hold the nominal output frequency of the Si599. Do not use with Si598.
3:1	Reserved	Always zero.
0	RECALL	**Recall NVM into RAM.** 0 = No operation. 1 = Write NVM bits into RAM. Bit is internally reset following completion of operation.

Register 137. Freeze DCO

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				Freeze DCO				
Type	R/W	R/W	R/W	R/W	R	R	R	R

Reset settings = Si598: 0000xxxx, Si599: 1000xxxx

Bit	Name	Function
7	Reserved	0: Si598 1: Si599
6:5	Reserved	This bits should read 0 in normal operation.
4	Freeze DCO	**Freeze DCO.** Freezes the DSPLL so the frequency configuration can be modified. Si598: Write 0x10 to this register to Freeze DCO. Si599: Write 0x90 to this register to Freeze DCO.
3:0	Reserved	Read only.

5. Si598 (XO) Pin Descriptions

(Top View)

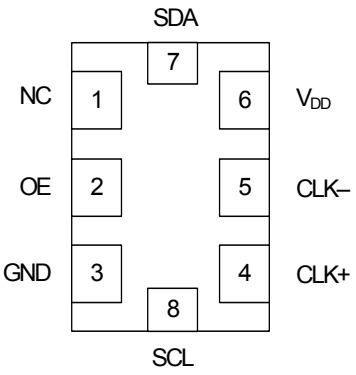


Table 15. Si598 Pin Descriptions

Pin	Name	Type	Function
1	NC	N/A	**No Connect.** Make no external connection to this pin.
2	OE	Input	**Output Enable.*** See 7. Ordering Information on page 21.
3	GND	Ground	**Electrical and Case Ground.**
4	CLK+	Output	**Oscillator Output.**
5	CLK– (NC for CMOS)	Output (N/A for CMOS)	**Complementary Output.** (NC for CMOS, do not make external connection).
6	V_{DD}	Power	**Power Supply Voltage.**
7	SDA	Bidirectional Open Drain	**I^2C Serial Data.**
8	SCL	Input	**I^2C Serial Clock.**
***Note:** OE pin includes a 17 kΩ resistor to V_{DD} for OE active high option or 17 kΩ to GND for OE active low option.			

6. Si599 (VCXO) Pin Descriptions

(Top View)

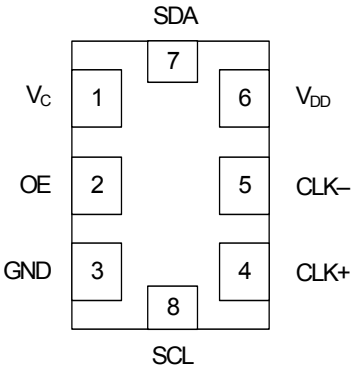


Table 16. Si599 Pin Descriptions

Pin	Name	Type	Function
1	V_C	Analog Input	**Control Voltage.**
2	OE	Input	**Output Enable.*** See 7. Ordering Information on page 21.
3	GND	Ground	**Electrical and Case Ground.**
4	CLK+	Output	**Oscillator Output.**
5	CLK– (NC for CMOS)	Output (N/A for CMOS)	**Complementary Output.** (NC for CMOS, do not make external connection).
6	V_{DD}	Power	**Power Supply Voltage.**
7	SDA	Bidirectional Open Drain	**I^2C Serial Data.**
8	SCL	Input	**I^2C Serial Clock.**
***Note:** OE pin includes a 17 kΩ resistor to V_{DD} for OE active high option or 17 kΩ to GND for OE active low option.			

7. Ordering Information

The Si598/Si599 supports a wide variety of options including frequency range, start-up frequency, temperature stability, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si598/Si599 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si598/Si599 XO/VCXO series is supplied in an industry-standard, RoHS compliant, 8-pad, 5x7 mm package. Tape and reel packaging is an ordering option.

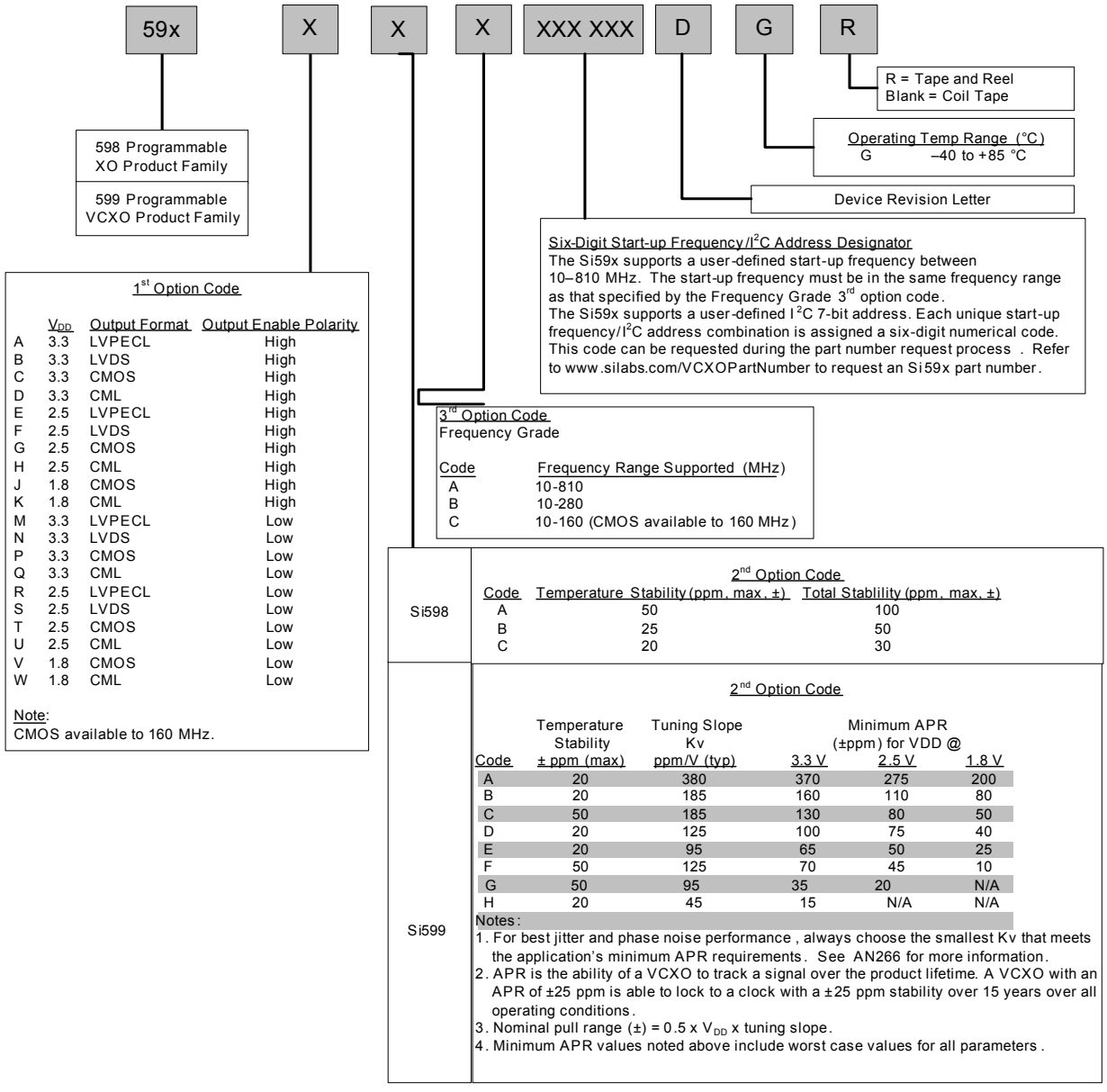


Figure 5. Part Number Convention

Table 17. Standard Si598 Part Numbers

Part Number	VDD	Output Format	Total Stability	Frequency Range	Startup Frequency	I^2C Address
598CCC000107DG	3.3V	CMOS	30 ppm	10–160 MHz	10 MHz	0x55
598BCA000107DG	3.3V	LVDS	30 ppm	10–810 MHz	10 MHz	0x55

8. Si59x Mark Specification

Figure 6 illustrates the mark specification for the Si59x. Table 18 lists the line information.

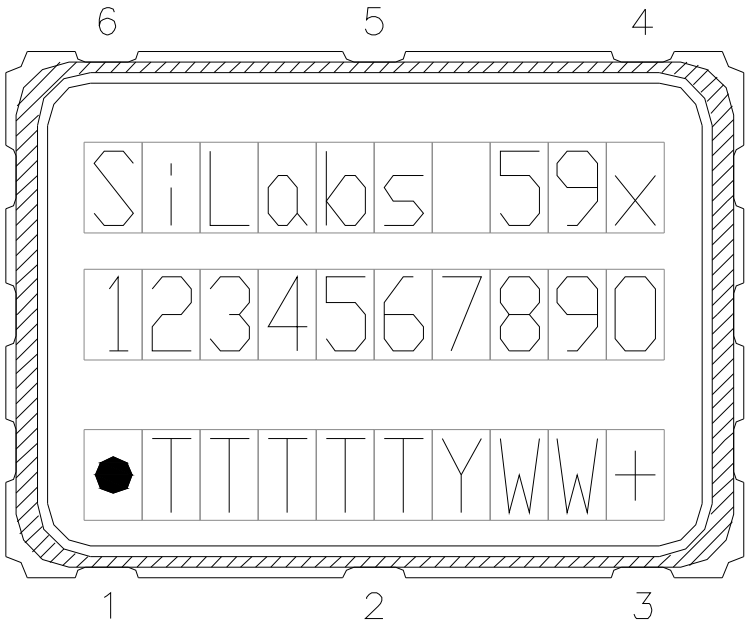


Figure 6. Mark Specification

Table 18. Si59x Top Mark Description

Line	Position	Description
1	1–10	“SiLabs"+ Part Family Number, 59x (first 3 characters in part number where x = 8 indicates a 598 device and x = 9 indicates a 599 device).
2	1–10	Option1 + Option2 + Option3 + ConfigNum(6) + Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2010 = 0)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

9. Outline Diagram and Suggested Pad Layout

Figure 7 illustrates the package details for the Si598/Si599. Table 19 lists the values for the dimensions shown in the illustration.

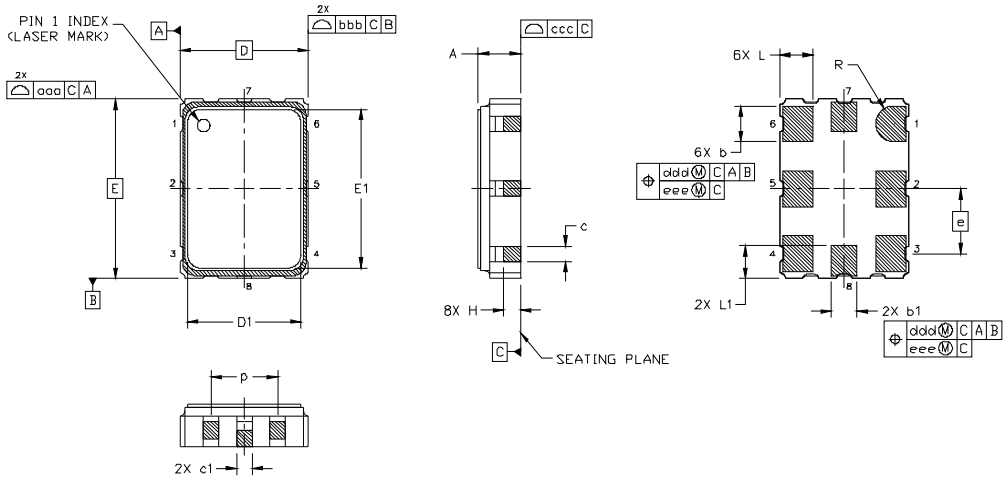


Figure 7. Si598/Si599 Outline Diagram

Table 19. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
b1	0.90	1.00	1.10
c	0.50	0.60	0.70
c1	0.30	—	0.60
D	5.00 BSC		
D1	4.30	4.40	4.50
e	2.54 BSC		
E	7.00 BSC		
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	1.07	1.17	1.27
p	1.80	—	2.60
R	0.70 REF		
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10
eee	—	—	0.05

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

10. 8-Pin PCB Land Pattern

Figure 8 illustrates the 8-pin PCB land pattern for the Si598/Si599. Table 20 lists the values for the dimensions shown in the illustration.

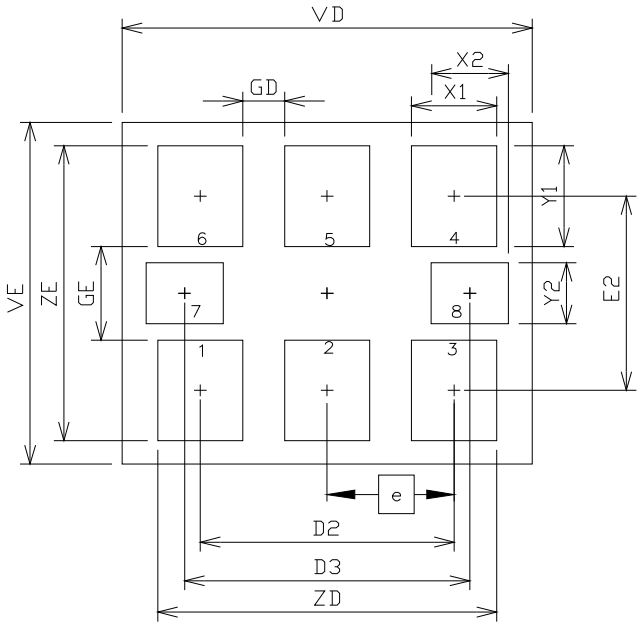


Figure 8. Si598/Si599 PCB Land Pattern

Table 20. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
D3	5.705 REF	
e	2.54 BSC	
E2	4.20 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X1	1.70 TYP	
X2	1.545 TYP	
Y1	2.15 REF	
Y2	1.3 REF	
ZD	—	6.78
ZE	—	6.30

Note:

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design follows IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

Revision History

Revision 1.1

June, 2018

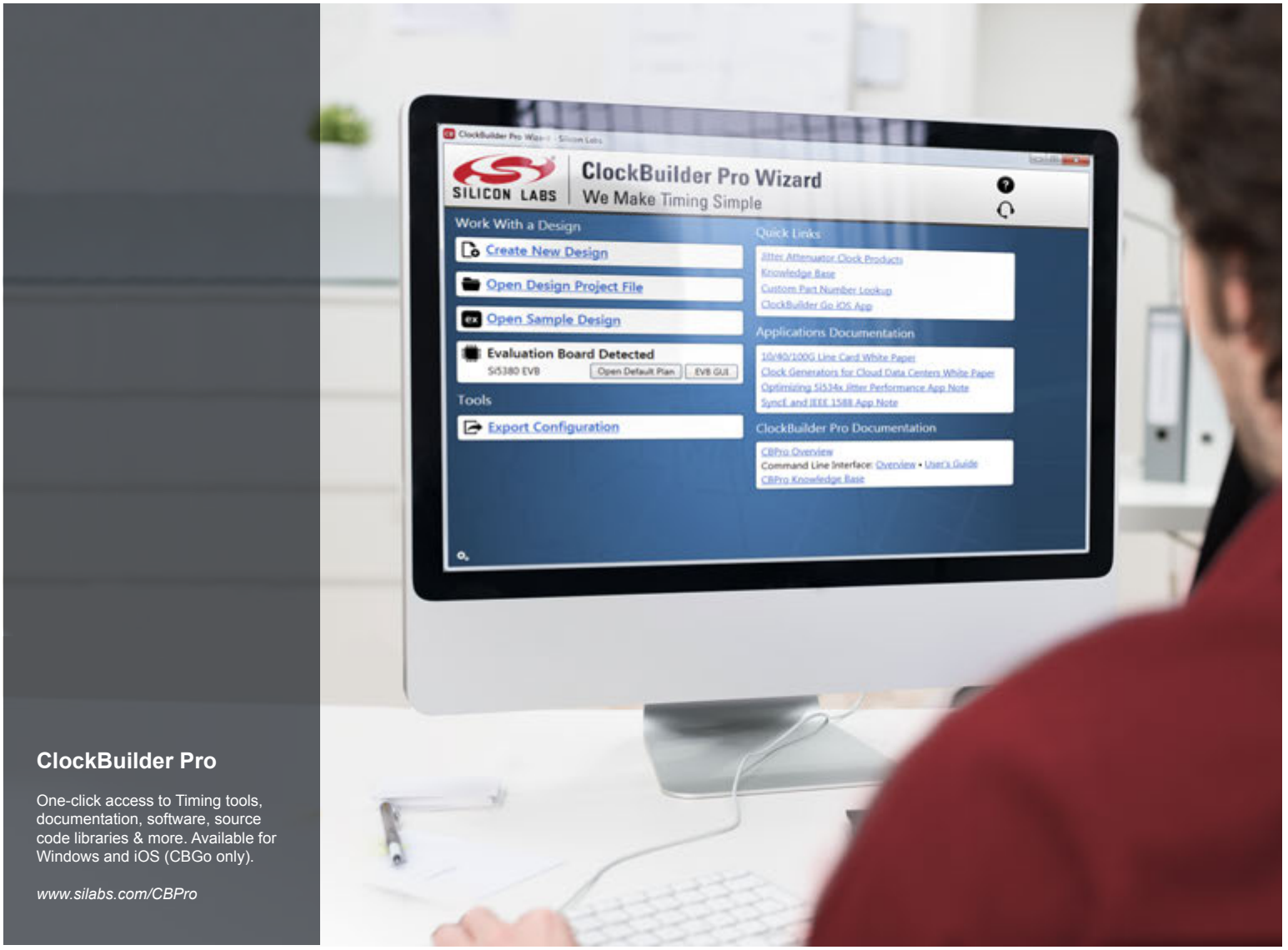
- Changed “Trays” to “Coil Tape” in 7. Ordering Information on page 21.

Revision 1.0

- Updated Register 135, “NewFreq/Freeze/Memory Control,” on page 17.
- Updated Register 137, “Freeze DCO,” on page 18.

Revision 0.9

- Updated Si598/599 devices to support frequencies up to 810 MHz for LVPECL, LVDS, and CML outputs.
- Added Table 13, “Thermal Characteristics,” on page 10.
- Updated ESD HBM sensitivity rating in Table 14 on page 10.
- Updated Table 11 on page 9 to include "Moisture Sensitivity Level" and "Contact Pads" rows.
- Updated Figure 6 and Table 18 on page 23 to reflect specific marking information.
- Corrected pin 7 and pin 8 designation in package diagram in Figure 7 on page 24.



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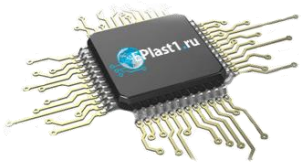

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