The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

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About Cypress

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MB9A110A/MB9A110 Series

32-bit ARM® Cortex®-M3 FM3 Microcontroller

The MB9A110A/MB9A110 Series are highly integrated 32-bit microcontrollers that target for high-performance and cost-sensitive embedded control applications.

The MB9A110A Series are based on the ARM® Cortex®-M3 Processor and on-chip Flash memory and SRAM, and peripheral functions, including Motor Control Timers, ADCs, Communication Interfaces (UART, CSIO, I²C, LIN).

The products which are described in this datasheet are placed into TYPE1 product categories in “FM3 Family Peripheral Manual”.

Features

32-bit ARM® Cortex®-M3 Core

- Processor version: r2p1
- Up to 40 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Up to 512 Kbyte
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This Series contain a total of up to 32 Kbyte on-chip SRAM. On-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 16 Kbytes
- SRAM1: Up to 16 Kbytes

Multi-function Serial Interface (Max 8 channels)

- 4 channels with 16 steps×9bit FIFO (ch.4-ch.7), 4 channels without FIFO (ch.0-ch3)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I²C

[UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)*
- Various error detection functions available (parity errors, framing errors, and overrun errors)

  *: MB9AF111LA, F112LA, F114LA, F112L and F114L do not support Hardware Flow control

[CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can be changed 13- 16bit length)
- LIN break delimiter generation (can be changed 1 - 4bit length)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

External Bus Interface*

- Supports SRAM, NOR Flash device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 Mbytes
- Supports Address/Data multiplex
- Supports external RDY function

*: MB9AF111LA, F112LA and F114LA do not support External Bus Interface

DMA Controller (8 channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 16 channels)

[12-bit A/D Converter]

- Successive Approximation type
- Built-in 3units*
- Conversion time: 1.0 µs@5 V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4steps)

*: MB9AF111LA, F112LA, F114LA built-in 2units

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

Multi-function Timer (Max 2 units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 3 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead timer function
- Input capture function
- A/D converter activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max 2 units)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each timer channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from Low-Power Consumption mode.

- Interval timer: up to 64 s(Max)@ Sub Clock: 32.768 kHz

Watch dog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

The "Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except STOP modes.

External Interrupt Controller Unit

- Up to 16 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 83 fast General Purpose I/O Ports@ 100 pin Package
- Some ports are 5V tolerant I/O (MB9AF115MA/NA, MB9AF116MA/NA only)
  Please see "Pin Description" to confirm the corresponding pins.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in High-speed CR Clock: 4 MHz
- Built-in Low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock Supervisor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- External clock failure (clock stop) is detected, reset is asserted.
- External frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Three Low-Power Consumption modes supported.

- SLEEP
- TIMER
- STOP

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM)*
  *: Mb9AF111LA/MA, F112LA/MA, F114LA/MA, F115MA and F116MA support only SWJ-DP.

Power Supply

- VCC = 2.7 V to 5.5 V: Correspond to the wide range voltage.

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1. Product Lineup

Memory Size

Product name	MB9AF111LA/MA/NA	MB9AF112LA/MA/NA MB9AF112L	MB9AF114LA/MA/NA MB9AF114L
On-chip Flash memory	64 Kbytes	128 Kbytes	256 Kbytes
On-chip SRAM	16 Kbytes	16 Kbytes	32 Kbytes

Product name	MB9AF115MA/NA	MB9AF116MA/NA
On-chip Flash memory	384 Kbytes	512 Kbytes
On-chip SRAM	32 Kbytes	32 Kbytes

Function

Product name			MB9AF111LA MB9AF112LA MB9AF114LA MB9AF112L MB9AF114L	MB9AF111MA MB9AF112MA MB9AF114MA MB9AF115MA MB9AF116MA	MB9AF111NA MB9AF112NA MB9AF114NA MB9AF115NA MB9AF116NA
Pin count			64	80	100
CPU			Cortex-M3		
	Freq.		40 MHz		
Power supply voltage range			2.7 V to 5.5 V		
DMAC			8 ch.		
External Bus Interface			-	Addr:21-bit (Max) Data:8-bit CS:4 (Max) Support: SRAM, NOR Flash	Addr:25-bit (Max) Data:8-/16-bit CS:8 (Max) Support: SRAM, NOR Flash
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8 ch. (Max) ch.4 to ch.7: FIFO (16 steps x 9-bit) ch.0 to ch.3: No FIFO		
Base Timer (PWC/Reload timer/PWM/PPG)			8 ch. (Max)		
MF-Timer	A/D activation compare	3 ch.	1 unit	2 units (Max)	
	Input capture	4 ch.			
	Free-run timer	3 ch.			
	Output compare	6 ch.			
	Waveform generator	3 ch.			
	PPG	3 ch.			
QPRC			2 ch. (Max)		
Dual Timer			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog timer			1 ch. (SW) + 1 ch. (HW)		
External Interrupts			8 pins (Max) + NMI × 1	11 pins (Max) + NMI × 1	16 pins (Max) + NMI × 1
I/O ports			51 pins (Max)	66 pins (Max)	83 pins (Max)
12-bit A/D converter			9 ch. (2 units)	12 ch. (3 units)	16 ch. (3 units)
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2 ch.		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SWJ-DP		SWJ-DP/ETM

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use. See "12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics" for accuracy of built-in CR.*

2. Packages

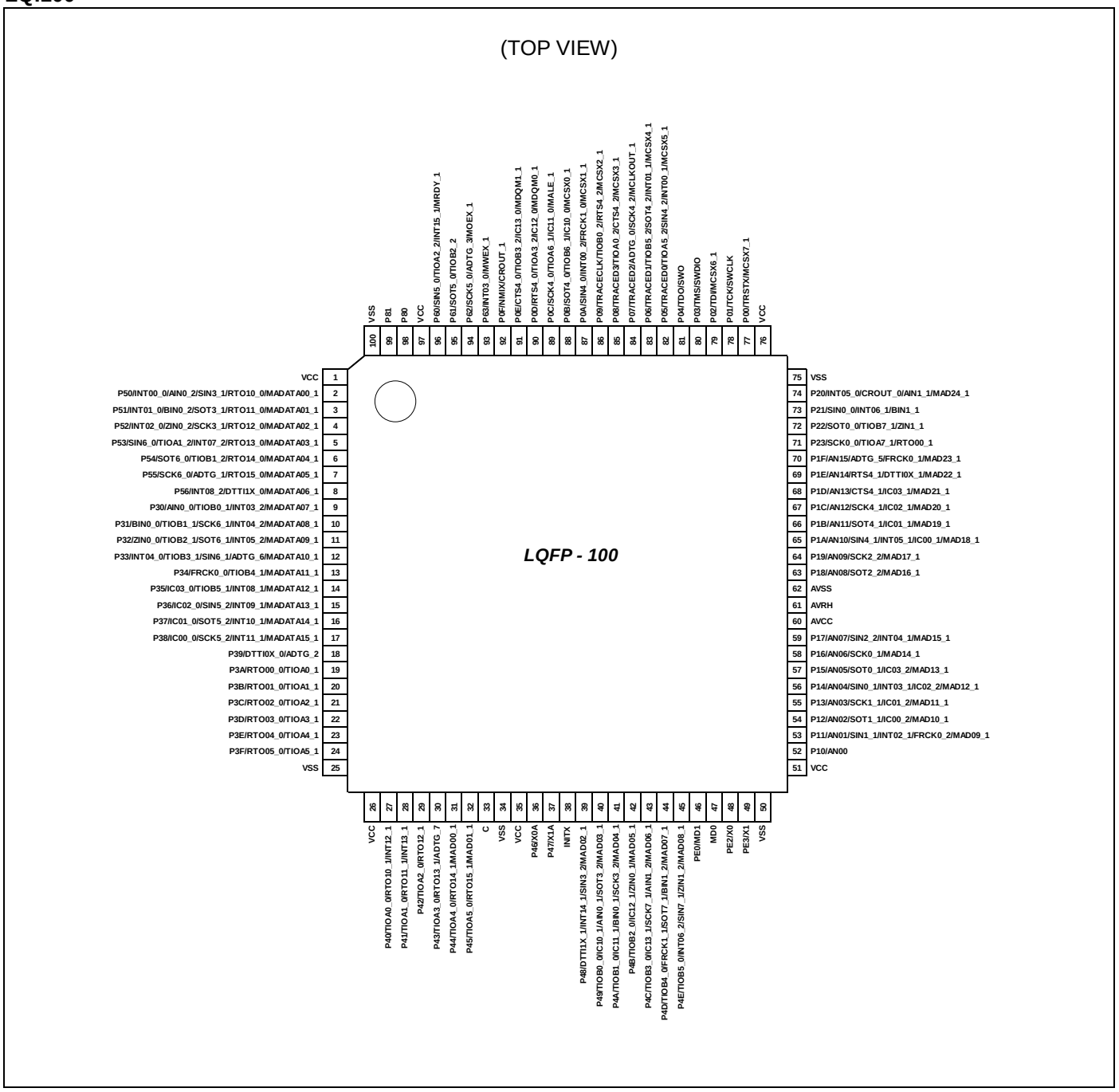
Package \ Product name	MB9AF111LA MB9AF112LA MB9AF114LA	MB9AF112L MB9AF114L	MB9AF111MA MB9AF112MA MB9AF114MA MB9AF115MA MB9AF116MA	MB9AF111NA MB9AF112NA MB9AF114NA MB9AF115NA MB9AF116NA
LQFP:LQD064 (0.5 mm pitch)	❍	-	-	-
LQFP:LQG064 (0.65 mm pitch)	❍	❍	-	-
QFN :VNC064 (0.5 mm pitch)	❍	-	-	-
LQFP:LQH080 (0.5 mm pitch)	-	-	❍	-
LQFP:LQI100 (0.65 mm pitch)	-	-	-	❍
QFP :PQH100 (0.65 mm pitch)	-	-	-	❍
BGA :LBC112 (0.8 mm pitch)	-	-	-	❍*

❍: Supported
*: MB9AF115NA, MB9AF116NA are planning

Note:
- *Refer to "14. Package Dimensions" for detailed information on each package.*

3. Pin Assignment

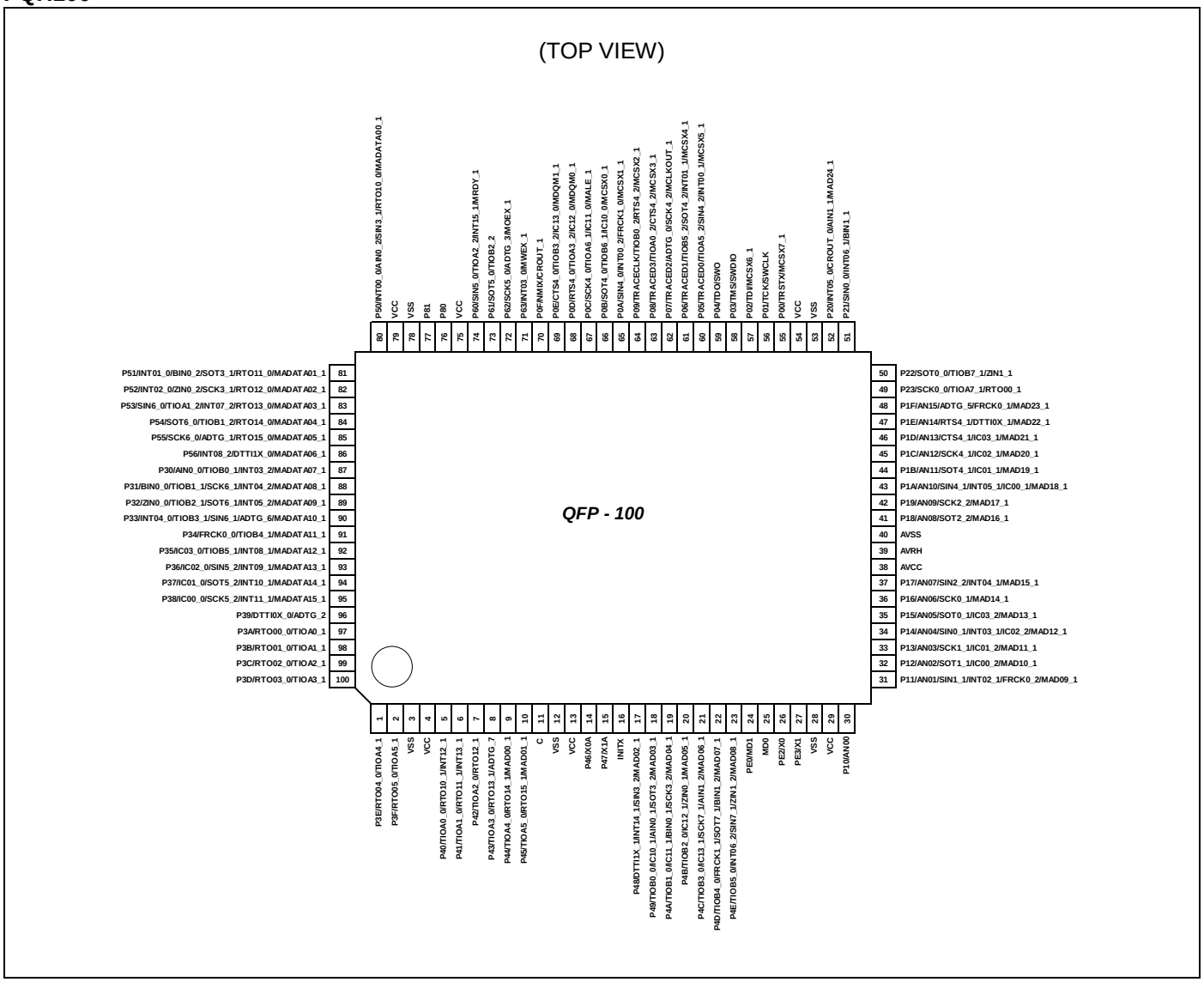
LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

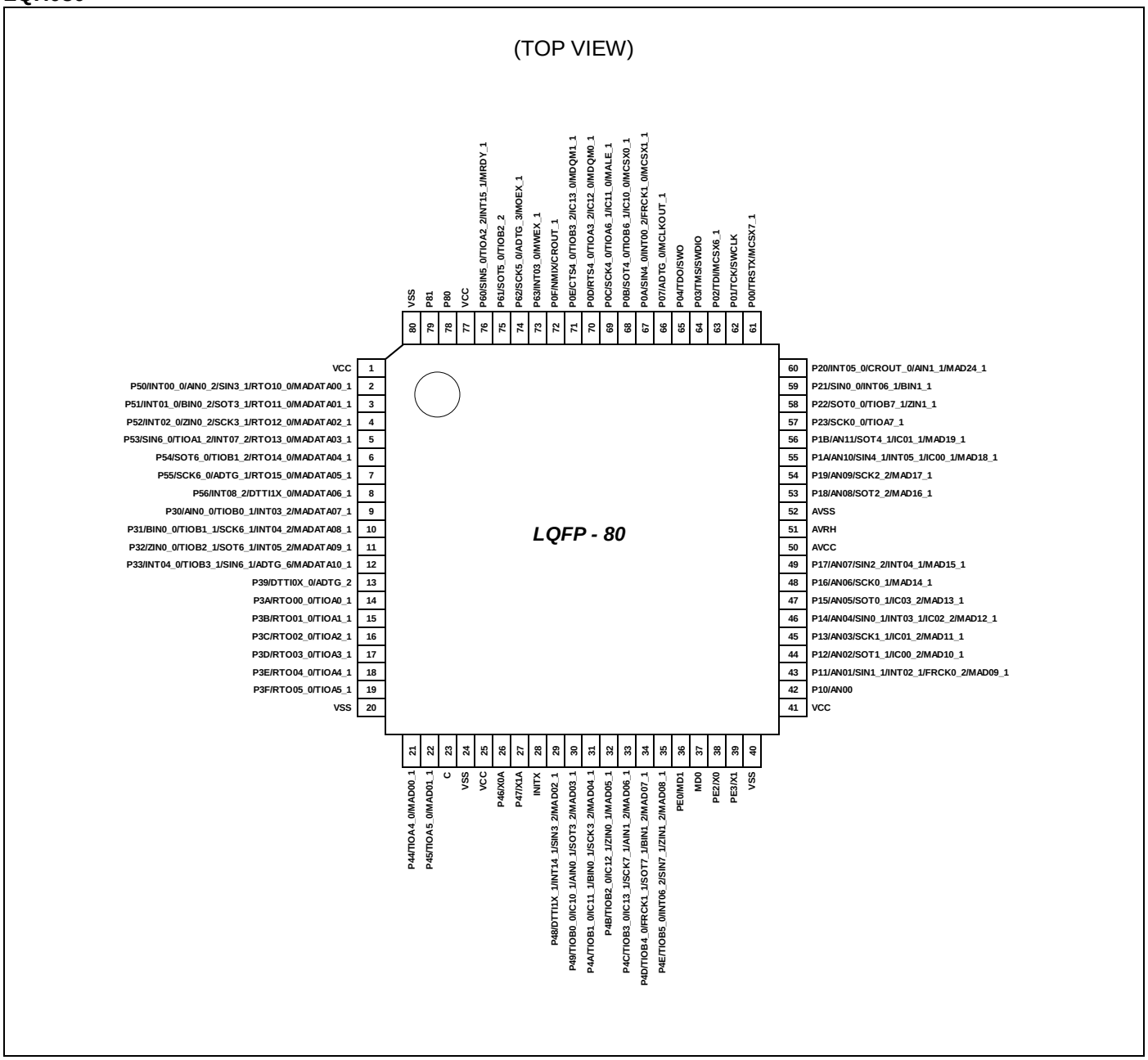
PQH100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

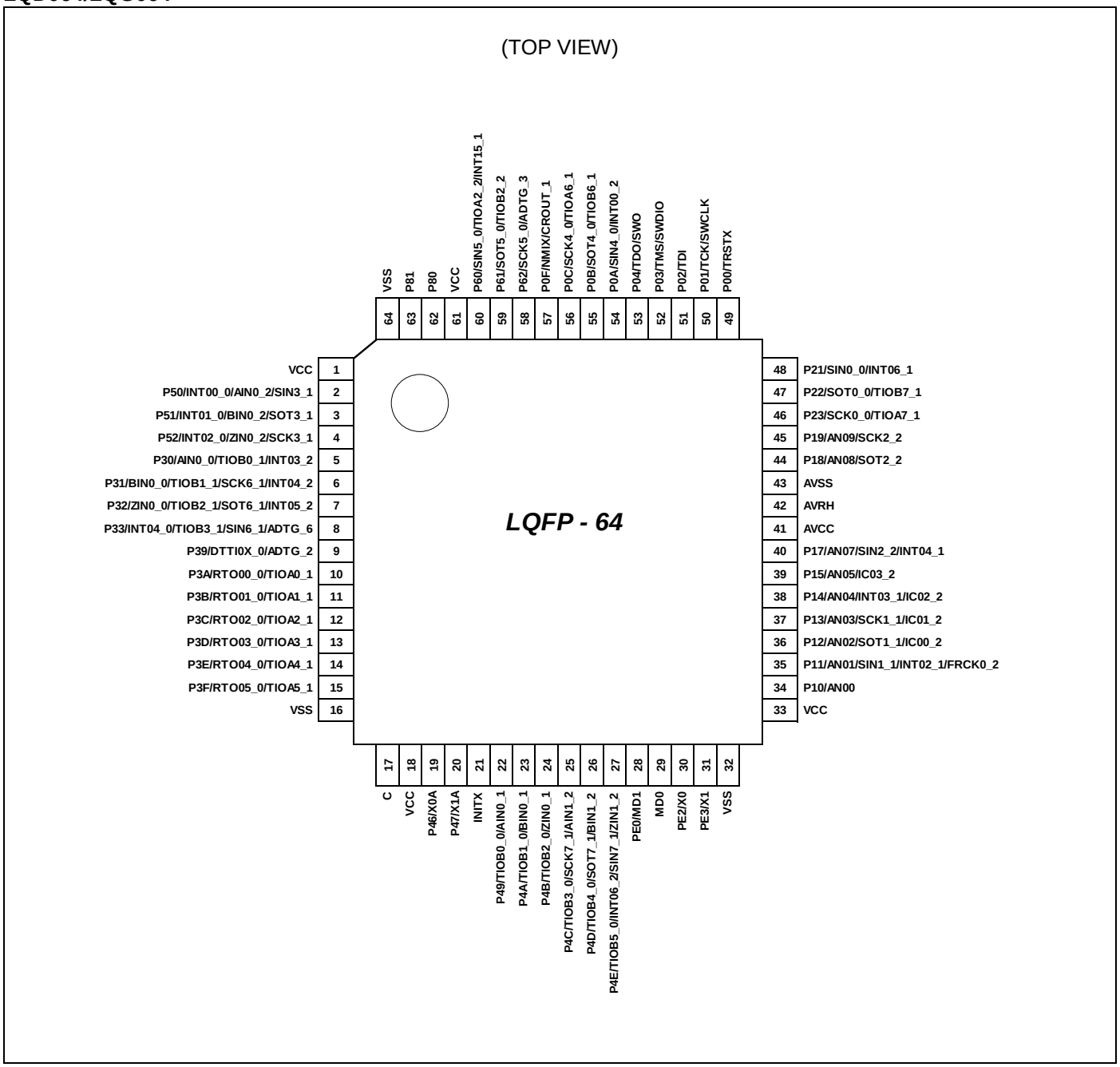
LQH080



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

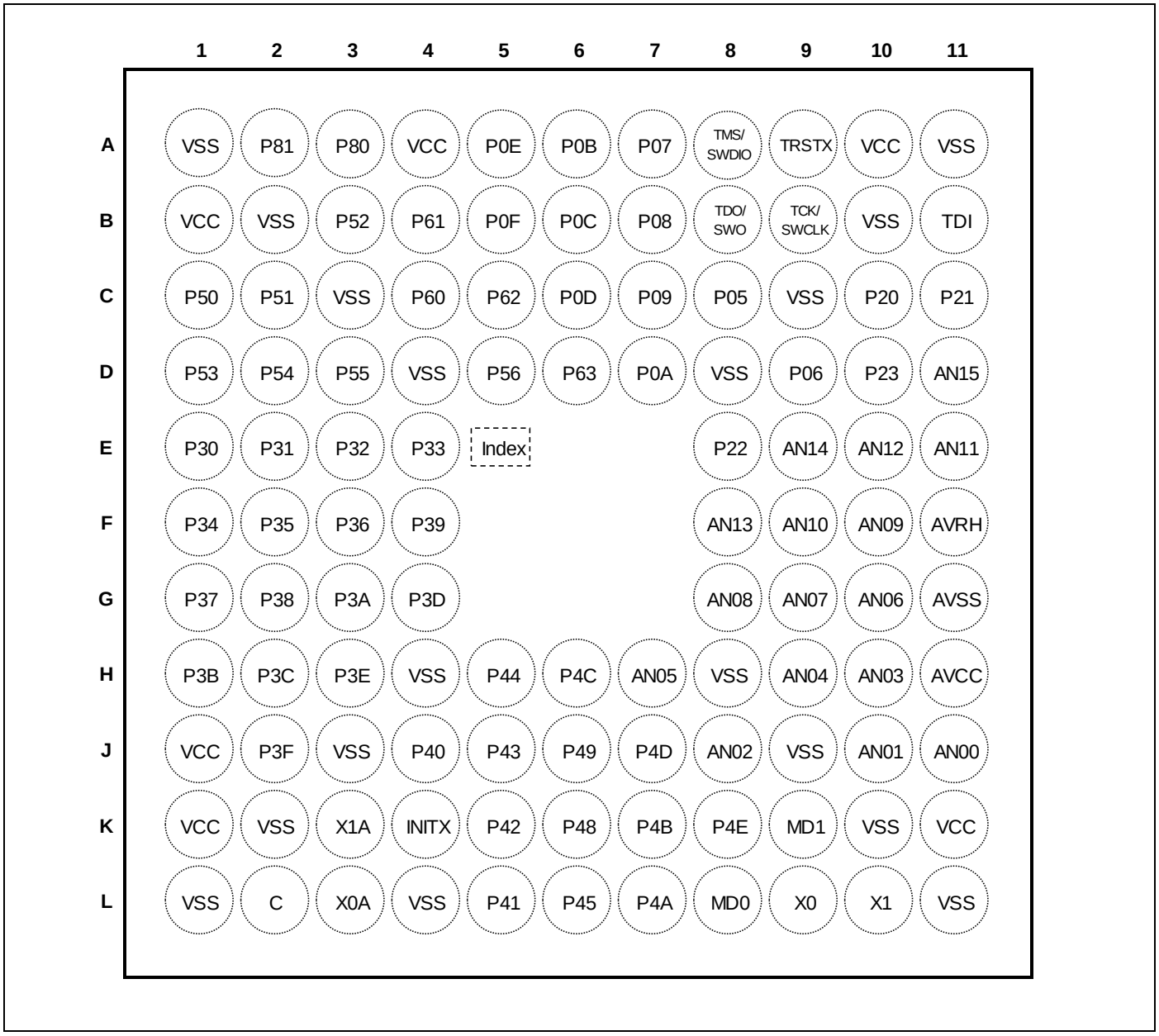
LQD064/LQG064



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

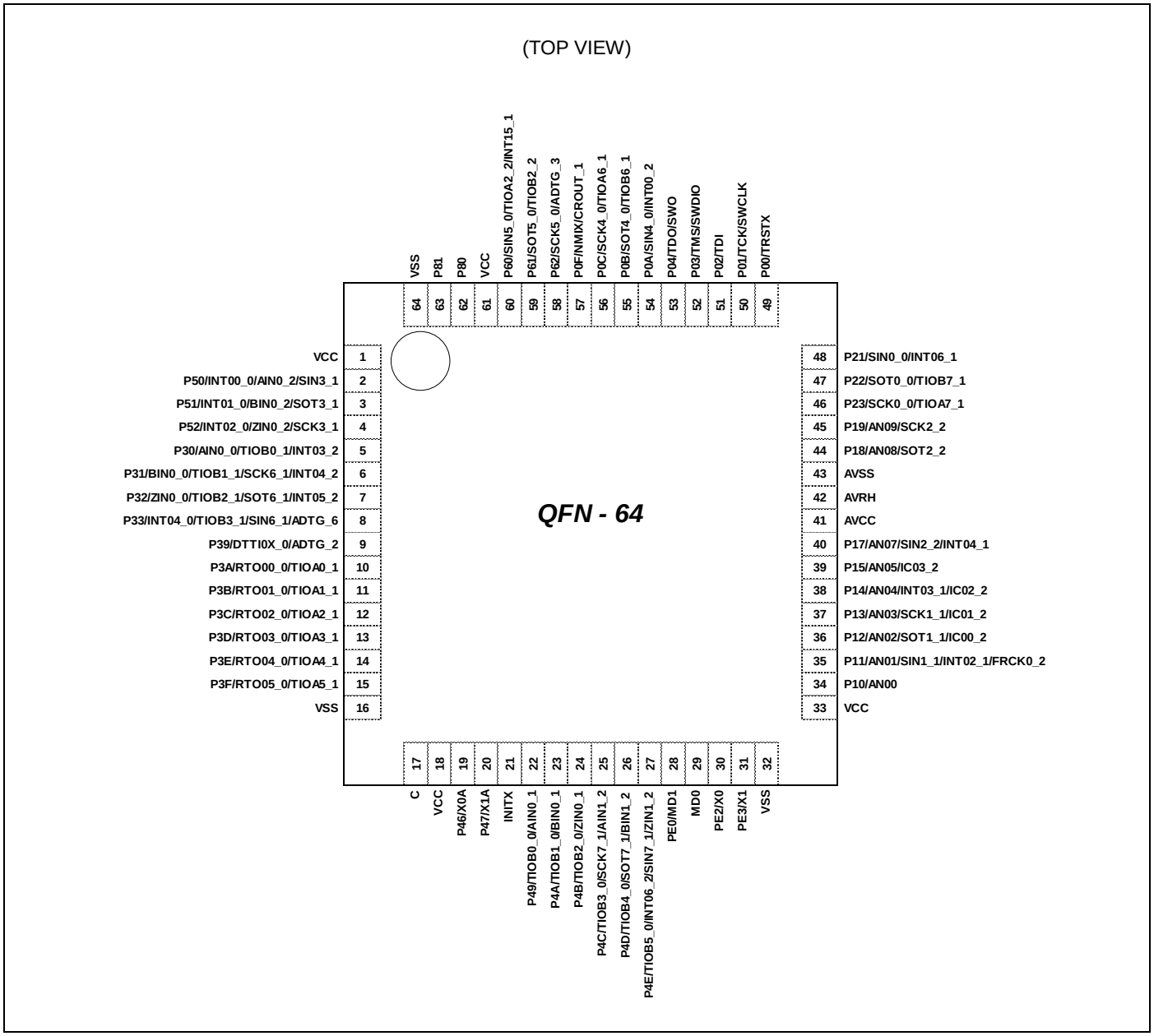
LBC112



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

VNC064



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
1	79	B1	1	1	VCC	-	
2	80	C1	2	2	P50 INT00_0 AIN0_2 SIN3_1	E	H
				-	RTO10_0 (PPG10_0) MADATA00_1		
3	81	C2	3	3	P51 INT01_0 BIN0_2 SOT3_1 (SDA3_1)	E	H
				-	RTO11_0 (PPG10_0) MADATA01_1		
4	82	B3	4	4	P52 INT02_0 ZIN0_2 SCK3_1 (SCL3_1)	E	H
				-	RTO12_0 (PPG12_0) MADATA02_1		
5	83	D1	5	-	P53 SIN6_0 TIOA1_2 INT07_2 RTO13_0 (PPG12_0) MADATA03_1	E	H
6	84	D2	6	-	P54 SOT6_0 (SDA6_0) TIOB1_2 RTO14_0 (PPG14_0) MADATA04_1	E	I

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
7	85	D3	7	-	P55	E	I
					SCK6_0 (SCL6_0)		
					ADTG_1		
					RTO15_0 (PPG14_0)		
					MADATA05_1		
8	86	D5	8	-	P56	E	H
					INT08_2		
					DTTI1X_0		
					MADATA06_1		
9	87	E1	9	5	P30	E	H
					AIN0_0		
					TIOB0_1		
					INT03_2		
				-	MADATA07_1		
10	88	E2	10	6	P31	E	H
					BIN0_0		
					TIOB1_1		
					SCK6_1 (SCL6_1)		
					INT04_2		
				-	MADATA08_1		
11	89	E3	11	7	P32	E	H
					ZIN0_0		
					TIOB2_1		
					SOT6_1 (SDA6_1)		
					INT05_2		
				-	MADATA09_1		
12	90	E4	12	8	P33	E	H
					INT04_0		
					TIOB3_1		
					SIN6_1		
					ADTG_6		
				-	MADATA10_1		
13	91	F1	-	-	P34	E	I
					FRCK0_0		
					TIOB4_1		
					MADATA11_1		

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
14	92	F2	-	-	P35 IC03_0 TIOB5_1 INT08_1 MADATA12_1	E	H
15	93	F3	-	-	P36 IC02_0 SIN5_2 INT09_1 MADATA13_1	E	H
16	94	G1	-	-	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MADATA14_1	E	H
17	95	G2	-	-	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1 MADATA15_1	E	H
18	96	F4	13	9	P39 DTTI0X_0 ADTG_2	E	I
19	97	G3	14	10	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
20	98	H1	15	11	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	99	H2	16	12	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	100	G4	17	13	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
-	-	B2	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
23	1	H3	18	14	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	2	J2	19	15	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	3	L1	20	16	VSS	-	
26	4	J1	-	-	VCC	-	
27	5	J4	-	-	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	H
28	6	L5	-	-	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1	G	H
29	7	K5	-	-	P42 TIOA2_0 RTO12_1 (PPG12_1)	G	I
30	8	J5	-	-	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7	G	I
31	9	H5	21 -	-	P44 TIOA4_0 MAD00_1 RTO14_1 (PPG14_1)	G	I
32	10	L6	22 -	-	P45 TIOA5_0 MAD01_1 RTO15_1 (PPG14_1)	G	I
-	-	K2	-	-	VSS	-	
-	-	J3	-	-	VSS	-	
-	-	H4	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
33	11	L2	23	17	C	-	
34	12	L4	24	-	VSS	-	
35	13	K1	25	18	VCC	-	
36	14	L3	26	19	P46	D	M
					X0A		
37	15	K3	27	20	P47	D	N
					X1A		
38	16	K4	28	21	INITX	B	C
39	17	K6	29	-	P48	E	H
					DTTI1X_1		
					INT14_1		
					SIN3_2		
					MAD02_1		
40	18	J6	30	22	P49	E	I
					TIOB0_0		
					AIN0_1		
				-	IC10_1		
					SOT3_2 (SDA3_2)		
					MAD03_1		
41	19	L7	31	23	P4A	E	I
					TIOB1_0		
					BIN0_1		
				-	IC11_1		
					SCK3_2 (SCL3_2)		
					MAD04_1		
42	20	K7	32	24	P4B	E	I
					TIOB2_0		
					ZIN0_1		
				-	IC12_1		
					MAD05_1		
43	21	H6	33	25	P4C	E / I*	I
					TIOB3_0		
					SCK7_1 (SCL7_1)		
					AIN1_2		
				-	IC13_1		
					MAD06_1		

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
44	22	J7	34	26	P4D	E / I*	I
					TIOB4_0		
					SOT7_1 (SDA7_1)		
					BIN1_2		
				-	FRCK1_1		
					MAD07_1		
45	23	K8	35	27	P4E	E / I*	I
					TIOB5_0		
					INT06_2		
					SIN7_1		
					ZIN1_2		
				-	MAD08_1		
46	24	K9	36	28	MD1	C	P
					PE0		
47	25	L8	37	29	MD0	J	D
48	26	L9	38	30	X0	A	A
					PE2		
49	27	L10	39	31	X1	A	B
					PE3		
50	28	L11	40	32	VSS	-	
51	29	K11	41	33	VCC	-	
52	30	J11	42	34	P10	F	K
					AN00		
53	31	J10	43	35	P11	F	L
					AN01		
					SIN1_1		
					INT02_1		
					FRCK0_2		
				-	MAD09_1		
54	32	J8	44	36	P12	F	K
					AN02		
					SOT1_1 (SDA1_1)		
					IC00_2		
				-	MAD10_1		
-	-	K10	-	-	VSS	-	
-	-	J9	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
55	33	H10	45	37	P13	F	K
					AN03		
					SCK1_1 (SCL1_1)		
					IC01_2		
				-	MAD11_1		
56	34	H9	46	38	P14	F	L
					AN04		
					INT03_1		
					IC02_2		
				-	SIN0_1		
					MAD12_1		
57	35	H7	47	39	P15	F	K
					AN05		
					IC03_2		
				-	SOT0_1 (SDA0_1)		
					MAD13_1		
58	36	G10	48	-	P16	F	K
					AN06		
					SCK0_1 (SCL0_1)		
					MAD14_1		
59	37	G9	49	40	P17	F	L
					AN07		
					SIN2_2		
					INT04_1		
				-	MAD15_1		
60	38	H11	50	41	AVCC	-	
61	39	F11	51	42	AVRH	-	
62	40	G11	52	43	AVSS	-	
63	41	G8	53	44	P18	F	K
					AN08		
					SOT2_2 (SDA2_2)		
				-	MAD16_1		
64	42	F10	54	45	P19	F	K
					AN09		
					SCK2_2 (SCL2_2)		
				-	MAD17_1		
-	-	H8	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
65	43	F9	55	-	P1A AN10 SIN4_1 INT05_1 IC00_1 MAD18_1	F	L
66	44	E11	56	-	P1B AN11 SOT4_1 (SDA4_1) IC01_1 MAD19_1	F	K
67	45	E10	-	-	P1C AN12 SCK4_1 (SCL4_1) IC02_1 MAD20_1	F	K
68	46	F8	-	-	P1D AN13 CTS4_1 IC03_1 MAD21_1	F	K
69	47	E9	-	-	P1E AN14 RTS4_1 DTTI0X_1 MAD22_1	F	K
70	48	D11	-	-	P1F AN15 ADTG_5 FRCK0_1 MAD23_1	F	K
-	-	B10	-	-	VSS	-	
-	-	C9	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
71	49	D10	57	46	P23	E	I
					SCK0_0 (SCL0_0)		
					TIOA7_1		
			-	-	RTO00_1 (PPG00_1)		
72	50	E8	58	47	P22	E	I
					SOT0_0 (SDA0_0)		
					TIOB7_1		
				-	ZIN1_1		
73	51	C11	59	48	P21	E	H
					SIN0_0		
					INT06_1		
				-	BIN1_1		
74	52	C10	60	-	P20	E	H
					INT05_0		
					CROUT_0		
					AIN1_1		
					MAD24_1		
75	53	A11	-	-	VSS	-	
76	54	A10	-	-	VCC	-	
77	55	A9	61	49	P00	E	E
					TRSTX		
				-	MCSX7_1		
78	56	B9	62	50	P01	E	E
					TCK		
					SWCLK		
79	57	B11	63	51	P02	E	E
					TDI		
				-	MCSX6_1		
80	58	A8	64	52	P03	E	E
					TMS		
					SWDIO		
81	59	B8	65	53	P04	E	E
					TDO		
					SWO		
82	60	C8	-	-	P05	E	F
					TRACED0		
					TIOA5_2		
					SIN4_2		
					INT00_1		
					MCSX5_1		
-	-	D8	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
83	61	D9	-	-	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 MCSX4_1	E	F
84	62	A7	66 -	-	P07 ADTG_0 MCLKOUT_1 TRACED2 SCK4_2 (SCL4_2)	E	G
85	63	B7	-	-	P08 TRACED3 TIOA0_2 CTS4_2 MCSX3_1	E	G
86	64	C7	-	-	P09 TRACECLK TIOB0_2 RTS4_2 MCSX2_1	E	G
87	65	D7	67	54 -	P0A SIN4_0 INT00_2 FRCK1_0 MCSX1_1	E / I*	H
88	66	A6	68	55 -	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 MCSX0_1	E / I*	I
89	67	B6	69	56 -	P0C SCK4_0 (SCL4_0) TIOA6_1 IC11_0 MALE_1	E / I*	I
-	-	D4	-	-	VSS	-	
-	-	C3	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
90	68	C6	70	-	P0D	E	I
					RTS4_0		
					TIOA3_2		
					IC12_0		
					MDQM0_1		
91	69	A5	71	-	P0E	E	I
					CTS4_0		
					TIOB3_2		
					IC13_0		
					MDQM1_1		
92	70	B5	72	57	P0F	E	J
					NMIX		
					CROUT_1		
93	71	D6	73	-	P63	E	H
					INT03_0		
					MWEX_1		
94	72	C5	74	58	P62	E	I
					SCK5_0 (SCL5_0)		
					ADTG_3		
				-	MOEX_1		
95	73	B4	75	59	P61	E	I
					SOT5_0 (SDA5_0)		
					TIOB2_2		
96	74	C4	76	60	P60	E / I*	H
					SIN5_0		
					TIOA2_2		
					INT15_1		
				-	MRDY_1		
97	75	A4	77	61	VCC	-	
98	76	A3	78	62	P80	H	O
99	77	A2	79	63	P81	H	O
100	78	A1	80	64	VSS	-	

*: 5V tolerant I/O on MB9AF115MA/NA and MB9AF116MA/NA

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
ADC	ADTG_0	A/D converter external trigger input pin	84	62	A7	66	-
	ADTG_1		7	85	D3	7	-
	ADTG_2		18	96	F4	13	9
	ADTG_3		94	72	C5	74	58
	ADTG_4		-	-	-	-	-
	ADTG_5		70	48	D11	-	-
	ADTG_6		12	90	E4	12	8
	ADTG_7		30	8	J5	-	-
	ADTG_8		-	-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	30	J11	42	34
	AN01		53	31	J10	43	35
	AN02		54	32	J8	44	36
	AN03		55	33	H10	45	37
	AN04		56	34	H9	46	38
	AN05		57	35	H7	47	39
	AN06		58	36	G10	48	-
	AN07		59	37	G9	49	40
	AN08		63	41	G8	53	44
	AN09		64	42	F10	54	45
	AN10		65	43	F9	55	-
	AN11		66	44	E11	56	-
	AN12		67	45	E10	-	-
	AN13		68	46	F8	-	-
	AN14		69	47	E9	-	-
	AN15		70	48	D11	-	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	27	5	J4	-	-
	TIOA0_1		19	97	G3	14	10
	TIOA0_2		85	63	B7	-	-
	TIOB0_0	Base timer ch.0 TIOB pin	40	18	J6	30	22
	TIOB0_1		9	87	E1	9	5
	TIOB0_2		86	64	C7	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	28	6	L5	-	-
	TIOA1_1		20	98	H1	15	11
	TIOA1_2		5	83	D1	5	-
	TIOB1_0	Base timer ch.1 TIOB pin	41	19	L7	31	23
	TIOB1_1		10	88	E2	10	6
	TIOB1_2		6	84	D2	6	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	29	7	K5	-	-
	TIOA2_1		21	99	H2	16	12
	TIOA2_2		96	74	C4	76	60
	TIOB2_0	Base timer ch.2 TIOB pin	42	20	K7	32	24
	TIOB2_1		11	89	E3	11	7
	TIOB2_2		95	73	B4	75	59
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	30	8	J5	-	-
	TIOA3_1		22	100	G4	17	13
	TIOA3_2		90	68	C6	70	-
	TIOB3_0	Base timer ch.3 TIOB pin	43	21	H6	33	25
	TIOB3_1		12	90	E4	12	8
	TIOB3_2		91	69	A5	71	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	31	9	H5	21	-
	TIOA4_1		23	1	H3	18	14
	TIOA4_2		-	-	-	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	44	22	J7	34	26
	TIOB4_1		13	91	F1	-	-
	TIOB4_2		-	-	-	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	32	10	L6	22	-
	TIOA5_1		24	2	J2	19	15
	TIOA5_2		82	60	C8	-	-
	TIOB5_0	Base timer ch.5 TIOB pin	45	23	K8	35	27
	TIOB5_1		14	92	F2	-	-
	TIOB5_2		83	61	D9	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	89	67	B6	69	56
	TIOB6_1	Base timer ch.6 TIOB pin	88	66	A6	68	55
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-	-	-	-
	TIOA7_1		71	49	D10	57	46
	TIOA7_2		-	-	-	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-	-	-	-
	TIOB7_1		72	50	E8	58	47
	TIOB7_2		-	-	-	-	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Debugger	SWCLK	Serial wire debug interface clock input	78	56	B9	62	50
	SWDIO	Serial wire debug interface data input / output	80	58	A8	64	52
	SWO	Serial wire viewer output	81	59	B8	65	53
	TCK	JTAG test clock input	78	56	B9	62	50
	TDI	JTAG test data input	79	57	B11	63	51
	TDO	JTAG debug data output	81	59	B8	65	53
	TMS	JTAG test mode state input/output	80	58	A8	64	52
	TRACECLK	Trace CLK output of ETM	86	64	C7	-	-
	TRACED0	Trace data output of ETM	82	60	C8	-	-
	TRACED1		83	61	D9	-	-
	TRACED2		84	62	A7	-	-
	TRACED3		85	63	B7	-	-
	TRSTX	JTAG test reset input	77	55	A9	61	49
External Bus	MAD00_1	External bus interface address bus	31	9	H5	21	-
	MAD01_1		32	10	L6	22	-
	MAD02_1		39	17	K6	29	-
	MAD03_1		40	18	J6	30	-
	MAD04_1		41	19	L7	31	-
	MAD05_1		42	20	K7	32	-
	MAD06_1		43	21	H6	33	-
	MAD07_1		44	22	J7	34	-
	MAD08_1		45	23	K8	35	-
	MAD09_1		53	31	J10	43	-
	MAD10_1		54	32	J8	44	-
	MAD11_1		55	33	H10	45	-
	MAD12_1		56	34	H9	46	-
	MAD13_1		57	35	H7	47	-
	MAD14_1		58	36	G10	48	-
	MAD15_1		59	37	G9	49	-
	MAD16_1		63	41	G8	53	-
	MAD17_1		64	42	F10	54	-
	MAD18_1		65	43	F9	55	-
	MAD19_1		66	44	E11	56	-
	MAD20_1		67	45	E10	-	-
	MAD21_1		68	46	F8	-	-
	MAD22_1		69	47	E9	-	-
	MAD23_1		70	48	D11	-	-
	MAD24_1		74	52	C10	60	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
External Bus	MCSX0_1	External bus interface chip select output pin	88	66	A6	68	-
	MCSX1_1		87	65	D7	67	-
	MCSX2_1		86	64	C7	-	-
	MCSX3_1		85	63	B7	-	-
	MCSX4_1		83	61	D9	-	-
	MCSX5_1		82	60	C8	-	-
	MCSX6_1		79	57	B11	63	-
	MCSX7_1		77	55	A9	61	-
	MDQM0_1	External bus interface byte mask signal output	90	68	C6	70	-
	MDQM1_1		91	69	A5	71	-
	MOEX_1	External bus interface read enable signal for SRAM	94	72	C5	74	-
	MWEX_1	External bus interface write enable signal for SRAM	93	71	D6	73	-
	MADATA00_1	External bus interface data bus	2	80	C1	2	-
	MADATA01_1		3	81	C2	3	-
	MADATA02_1		4	82	B3	4	-
	MADATA03_1		5	83	D1	5	-
	MADATA04_1		6	84	D2	6	-
	MADATA05_1		7	85	D3	7	-
	MADATA06_1		8	86	D5	8	-
	MADATA07_1		9	87	E1	9	-
	MADATA08_1		10	88	E2	10	-
	MADATA09_1		11	89	E3	11	-
	MADATA10_1		12	90	E4	12	-
	MADATA11_1		13	91	F1	-	-
	MADATA12_1		14	92	F2	-	-
	MADATA13_1		15	93	F3	-	-
	MADATA14_1		16	94	G1	-	-
	MADATA15_1		17	95	G2	-	-
	MALE_1	Address Latch enable signal for multiplex	89	67	B6	69	-
	MRDY_1	External RDY input signal	96	74	C4	76	-
	MCLKOUT_1	External bus clock output	84	62	A7	66	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
External Interrupt	INT00_0	External interrupt request 00 input pin	2	80	C1	2	2
	INT00_1		82	60	C8	-	-
	INT00_2		87	65	D7	67	54
	INT01_0	External interrupt request 01 input pin	3	81	C2	3	3
	INT01_1		83	61	D9	-	-
	INT02_0	External interrupt request 02 input pin	4	82	B3	4	4
	INT02_1		53	31	J10	43	35
	INT03_0	External interrupt request 03 input pin	93	71	D6	73	-
	INT03_1		56	34	H9	46	38
	INT03_2		9	87	E1	9	5
	INT04_0	External interrupt request 04 input pin	12	90	E4	12	8
	INT04_1		59	37	G9	49	40
	INT04_2		10	88	E2	10	6
	INT05_0	External interrupt request 05 input pin	74	52	C10	60	-
	INT05_1		65	43	F9	55	-
	INT05_2		11	89	E3	11	7
	INT06_1	External interrupt request 06 input pin	73	51	C11	59	48
	INT06_2		45	23	K8	35	27
	INT07_2	External interrupt request 07 input pin	5	83	D1	5	-
	INT08_1	External interrupt request 08 input pin	14	92	F2	-	-
	INT08_2		8	86	D5	8	-
	INT09_1	External interrupt request 09 input pin	15	93	F3	-	-
	INT10_1	External interrupt request 10 input pin	16	94	G1	-	-
	INT11_1	External interrupt request 11 input pin	17	95	G2	-	-
	INT12_1	External interrupt request 12 input pin	27	5	J4	-	-
	INT13_1	External interrupt request 13 input pin	28	6	L5	-	-
	INT14_1	External interrupt request 14 input pin	39	17	K6	29	-
	INT15_1	External interrupt request 15 input pin	96	74	C4	76	60
	NMIX	Non-Maskable Interrupt input	92	70	B5	72	57

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
GPIO	P00	General-purpose I/O port 0	77	55	A9	61	49
	P01		78	56	B9	62	50
	P02		79	57	B11	63	51
	P03		80	58	A8	64	52
	P04		81	59	B8	65	53
	P05		82	60	C8	-	-
	P06		83	61	D9	-	-
	P07		84	62	A7	66	-
	P08		85	63	B7	-	-
	P09		86	64	C7	-	-
	P0A		87	65	D7	67	54
	P0B		88	66	A6	68	55
	P0C		89	67	B6	69	56
	P0D		90	68	C6	70	-
	P0E		91	69	A5	71	-
	P0F		92	70	B5	72	57
	P10	General-purpose I/O port 1	52	30	J11	42	34
	P11		53	31	J10	43	35
	P12		54	32	J8	44	36
	P13		55	33	H10	45	37
	P14		56	34	H9	46	38
	P15		57	35	H7	47	39
	P16		58	36	G10	48	-
	P17		59	37	G9	49	40
	P18		63	41	G8	53	44
	P19		64	42	F10	54	45
	P1A		65	43	F9	55	-
	P1B		66	44	E11	56	-
	P1C		67	45	E10	-	-
	P1D		68	46	F8	-	-
	P1E		69	47	E9	-	-
	P1F		70	48	D11	-	-
	P20	General-purpose I/O port 2	74	52	C10	60	-
	P21		73	51	C11	59	48
	P22		72	50	E8	58	47
	P23		71	49	D10	57	46

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
GPIO	P30	General-purpose I/O port 3	9	87	E1	9	5
	P31		10	88	E2	10	6
	P32		11	89	E3	11	7
	P33		12	90	E4	12	8
	P34		13	91	F1	-	-
	P35		14	92	F2	-	-
	P36		15	93	F3	-	-
	P37		16	94	G1	-	-
	P38		17	95	G2	-	-
	P39		18	96	F4	13	9
	P3A		19	97	G3	14	10
	P3B		20	98	H1	15	11
	P3C		21	99	H2	16	12
	P3D		22	100	G4	17	13
	P3E		23	1	H3	18	14
	P3F		24	2	J2	19	15
	P40	General-purpose I/O port 4	27	5	J4	-	-
	P41		28	6	L5	-	-
	P42		29	7	K5	-	-
	P43		30	8	J5	-	-
	P44		31	9	H5	21	-
	P45		32	10	L6	22	-
	P46		36	14	L3	26	19
	P47		37	15	K3	27	20
	P48		39	17	K6	29	-
	P49		40	18	J6	30	22
	P4A		41	19	L7	31	23
	P4B		42	20	K7	32	24
	P4C		43	21	H6	33	25
	P4D		44	22	J7	34	26
	P4E		45	23	K8	35	27
	P50	General-purpose I/O port 5	2	80	C1	2	2
	P51		3	81	C2	3	3
	P52		4	82	B3	4	4
	P53		5	83	D1	5	-
	P54		6	84	D2	6	-
	P55		7	85	D3	7	-
	P56		8	86	D5	8	-
	P60	General-purpose I/O port 6	96	74	C4	76	60
	P61		95	73	B4	75	59
	P62		94	72	C5	74	58
	P63		93	71	D6	73	-
	P80	General-purpose I/O port 8	98	76	A3	78	62
	P81		99	77	A2	79	63
	PE0	General-purpose I/O port E	46	24	K9	36	28
	PE2		48	26	L9	38	30
	PE3		49	27	L10	39	31

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 0	SIN0_0	Multifunction serial interface ch.0 input pin	73	51	C11	59	48
	SIN0_1		56	34	H9	46	-
	SOT0_0 (SDA0_0)	Multifunction serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	72	50	E8	58	47
	SOT0_1 (SDA0_1)		57	35	H7	47	-
	SCK0_0 (SCL0_0)	Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4).	71	49	D10	57	46
	SCK0_1 (SCL0_1)		58	36	G10	48	-
Multi Function Serial 1	SIN1_1	Multifunction serial interface ch.1 input pin	53	31	J10	43	35
	SOT1_1 (SDA1_1)	Multifunction serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	54	32	J8	44	36
	SCK1_1 (SCL1_1)	Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I^2C (operation mode 4).	55	33	H10	45	37
Multi Function Serial 2	SIN2_2	Multifunction serial interface ch.2 input pin	59	37	G9	49	40
	SOT2_2 (SDA2_2)	Multifunction serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	63	41	G8	53	44
	SCK2_2 (SCL2_2)	Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I^2C (operation mode 4).	64	42	F10	54	45
Multi Function Serial 3	SIN3_1	Multifunction serial interface ch.3 input pin	2	80	C1	2	2
	SIN3_2		39	17	K6	29	-
	SOT3_1 (SDA3_1)	Multifunction serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	3	81	C2	3	3
	SOT3_2 (SDA3_2)		40	18	J6	30	-
	SCK3_1 (SCL3_1)	Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation mode 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	82	B3	4	4
	SCK3_2 (SCL3_2)		41	19	L7	31	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin	87	65	D7	67	54
	SIN4_1		65	43	F9	55	-
	SIN4_2		82	60	C8	-	-
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	66	A6	68	55
	SOT4_1 (SDA4_1)		66	44	E11	56	-
	SOT4_2 (SDA4_2)		83	61	D9	-	-
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	67	B6	69	56
	SCK4_1 (SCL4_1)		67	45	E10	-	-
	SCK4_2 (SCL4_2)		84	62	A7	-	-
	RTS4_0	Multifunction serial interface ch.4 RTS output pin	90	68	C6	70	-
	RTS4_1		69	47	E9	-	-
	RTS4_2		86	64	C7	-	-
	CTS4_0	Multifunction serial interface ch.4 CTS input pin	91	69	A5	71	-
	CTS4_1		68	46	F8	-	-
	CTS4_2		85	63	B7	-	-
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin	96	74	C4	76	60
	SIN5_2		15	93	F3	-	-
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	73	B4	75	59
	SOT5_2 (SDA5_2)		16	94	G1	-	-
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	72	C5	74	58
	SCK5_2 (SCL5_2)		17	95	G2	-	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin	5	83	D1	5	-
	SIN6_1		12	90	E4	12	8
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	6	84	D2	6	-
	SOT6_1 (SDA6_1)		11	89	E3	11	7
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	85	D3	7	-
	SCK6_1 (SCL6_1)		10	88	E2	10	6
Multi Function Serial 7	SIN7_1	Multifunction serial interface ch.7 input pin	45	23	K8	35	27
	SOT7_1 (SDA7_1)	Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	44	22	J7	34	26
	SCK7_1 (SCL7_1)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	43	21	H6	33	25

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of multi-function timer 0	18	96	F4	13	9
	DTTI0X_1		69	47	E9	-	-
	FRCK0_0	16-bit free-run timer external clock input pin	13	91	F1	-	-
	FRCK0_1		70	48	D11	-	-
	FRCK0_2		53	31	J10	43	35
	IC00_0	16-bit input capture input pin of multi-function timer 0. ICxx describes channel number.	17	95	G2	-	-
	IC00_1		65	43	F9	55	-
	IC00_2		54	32	J8	44	36
	IC01_0		16	94	G1	-	-
	IC01_1		66	44	E11	56	-
	IC01_2		55	33	H10	45	37
	IC02_0		15	93	F3	-	-
	IC02_1		67	45	E10	-	-
	IC02_2		56	34	H9	46	38
	IC03_0		14	92	F2	-	-
	IC03_1		68	46	F8	-	-
	IC03_2		57	35	H7	47	39
	RTO00_0 (PPG00_0)	Waveform generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG 0 output mode.	19	97	G3	14	10
	RTO00_1 (PPG00_1)		71	49	D10	-	-
	RTO01_0 (PPG00_0)	Waveform generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG 0 output mode.	20	98	H1	15	11
	RTO02_0 (PPG02_0)	Waveform generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output mode.	21	99	H2	16	12
	RTO03_0 (PPG02_0)	Waveform generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output mode.	22	100	G4	17	13
	RTO04_0 (PPG04_0)	Waveform generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output mode.	23	1	H3	18	14
	RTO05_0 (PPG04_0)	Waveform generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output mode.	24	2	J2	19	15

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 1	DTTI1X_0	Input signal of waveform generator to control outputs RTO10 to RTO15 of multi-function timer 1	8	86	D5	8	-
	DTTI1X_1		39	17	K6	29	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	87	65	D7	67	-
	FRCK1_1		44	22	J7	34	-
	IC10_0	16-bit input capture input pin of multi-function timer 1. ICxx describes channel number.	88	66	A6	68	-
	IC10_1		40	18	J6	30	-
	IC11_0		89	67	B6	69	-
	IC11_1		41	19	L7	31	-
	IC12_0		90	68	C6	70	-
	IC12_1		42	20	K7	32	-
	IC13_0		91	69	A5	71	-
	IC13_1		43	21	H6	33	-
	RTO10_0 (PPG10_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output mode.	2	80	C1	2	-
	RTO10_1 (PPG10_1)		27	5	J4	-	-
	RTO11_0 (PPG10_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output mode.	3	81	C2	3	-
	RTO11_1 (PPG10_1)		28	6	L5	-	-
	RTO12_0 (PPG12_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output mode.	4	82	B3	4	-
	RTO12_1 (PPG12_1)		29	7	K5	-	-
	RTO13_0 (PPG12_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output mode.	5	83	D1	5	-
	RTO13_1 (PPG12_1)		30	8	J5	-	-
	RTO14_0 (PPG14_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output mode.	6	84	D2	6	-
	RTO14_1 (PPG14_1)		31	9	H5	21	-
	RTO15_0 (PPG14_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output mode.	7	85	D3	7	-
	RTO15_1 (PPG14_1)		32	10	L6	22	-

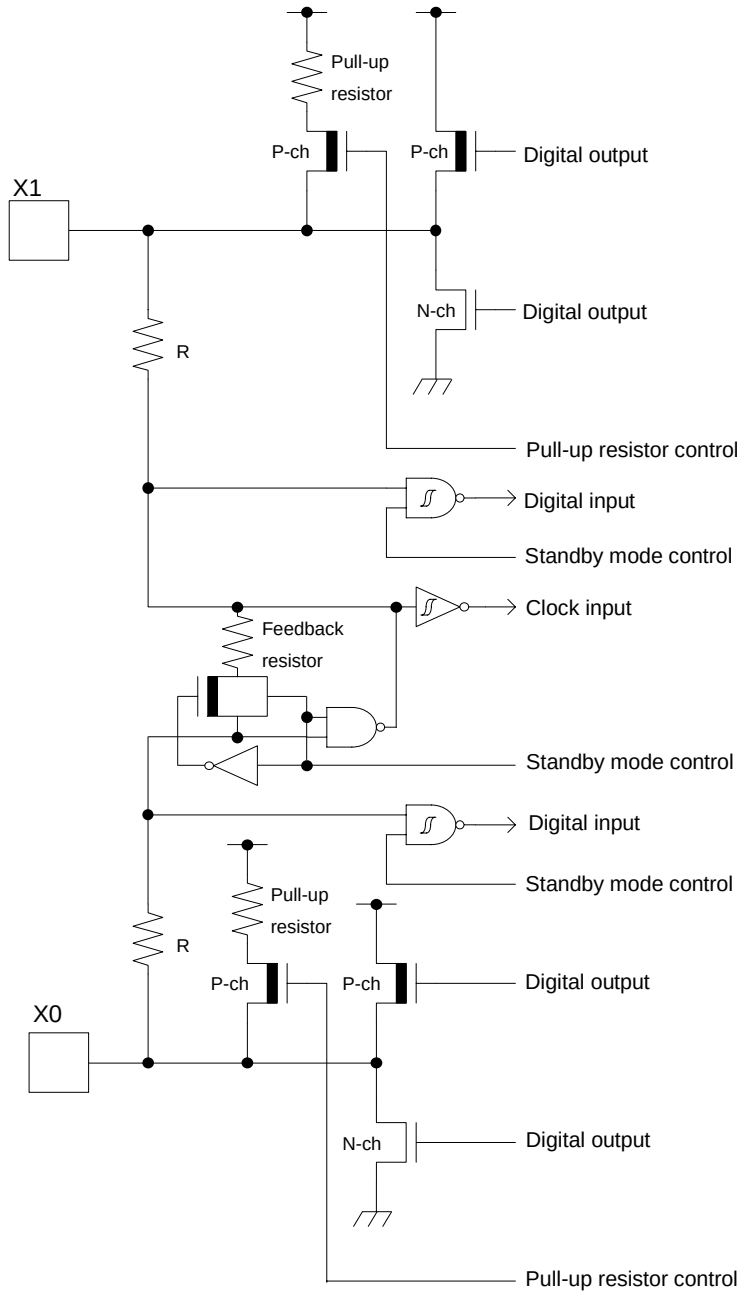
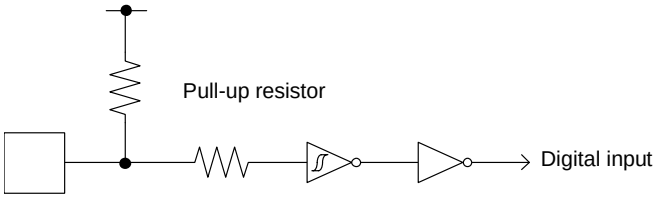
Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	9	87	E1	9	5
	AIN0_1		40	18	J6	30	22
	AIN0_2		2	80	C1	2	2
	BIN0_0	QPRC ch.0 BIN input pin	10	88	E2	10	6
	BIN0_1		41	19	L7	31	23
	BIN0_2		3	81	C2	3	3
	ZIN0_0	QPRC ch.0 ZIN input pin	11	89	E3	11	7
	ZIN0_1		42	20	K7	32	24
	ZIN0_2		4	82	B3	4	4
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin	74	52	C10	60	-
	AIN1_2		43	21	H6	33	25
	BIN1_1	QPRC ch.1 BIN input pin	73	51	C11	59	-
	BIN1_2		44	22	J7	34	26
	ZIN1_1	QPRC ch.1 ZIN input pin	72	50	E8	58	-
	ZIN1_2		45	23	K8	35	27

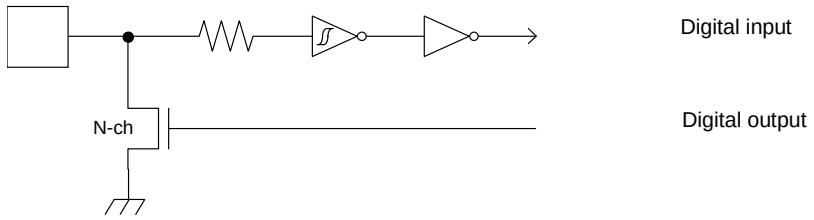
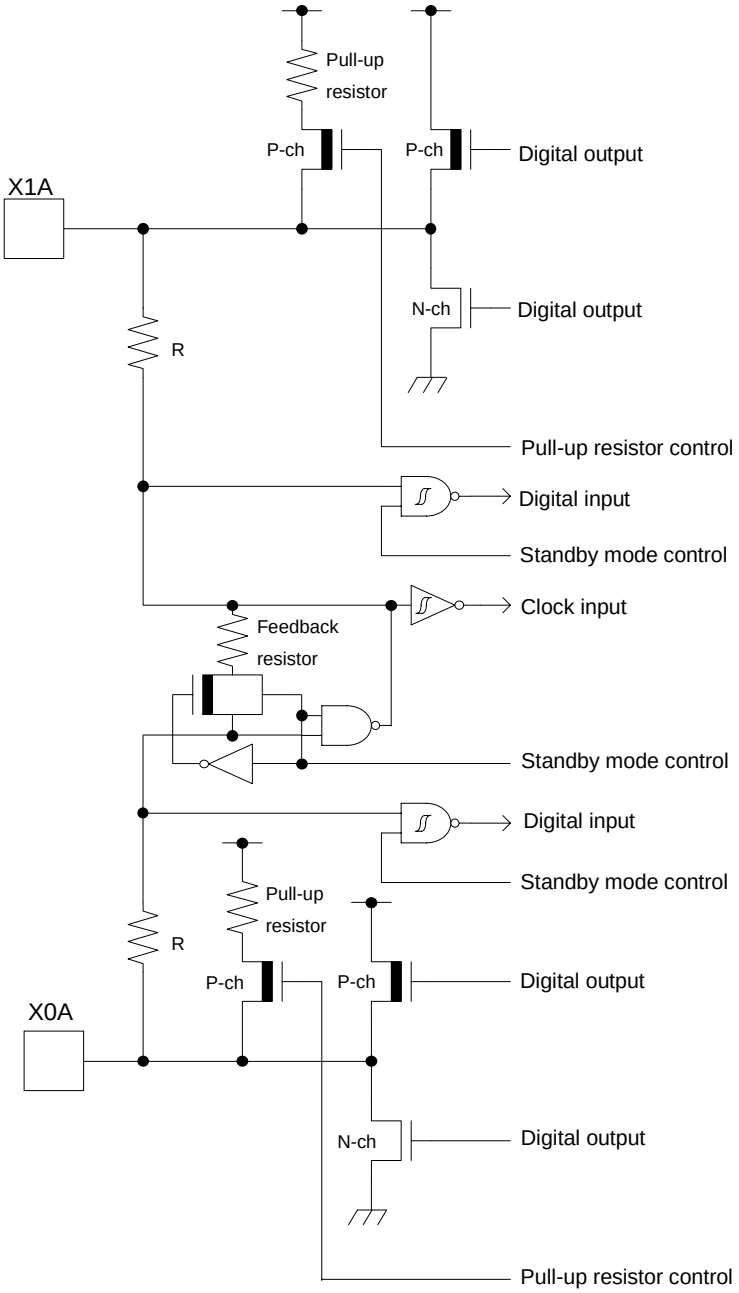
Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Reset	INITX	External Reset Input. A reset is valid when INITX="L"	38	16	K4	28	21
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to flash memory, MD0="H" must be input.	47	25	L8	37	29
	MD1	Mode 1 pin. During serial programming to flash memory, MD1="L" must be input.	46	24	K9	36	28
Power	VCC	Power supply pin	1	79	B1	1	1
	VCC	Power supply pin	26	4	J1	-	-
	VCC	Power supply pin	35	13	K1	25	18
	VCC	Power supply pin	51	29	K11	41	33
	VCC	Power supply pin	76	54	A10	-	-
	VCC	Power supply pin	97	75	A4	77	61
GND	VSS	GND pin	-	-	B2	-	-
	VSS	GND pin	25	3	L1	20	16
	VSS	GND pin	-	-	K2	-	-
	VSS	GND pin	-	-	J3	-	-
	VSS	GND pin	-	-	H4	-	-
	VSS	GND pin	34	12	L4	24	-
	VSS	GND pin	50	28	L11	40	32
	VSS	GND pin	-	-	K10	-	-
	VSS	GND pin	-	-	J9	-	-
	VSS	GND pin	-	-	H8	-	-
	VSS	GND pin	-	-	B10	-	-
	VSS	GND pin	-	-	C9	-	-
	VSS	GND pin	75	53	A11	-	-
	VSS	GND pin	-	-	D8	-	-
	VSS	GND pin	-	-	D4	-	-
	VSS	GND pin	-	-	C3	-	-
	VSS	GND pin	100	78	A1	80	64
Clock	X0	Main clock (oscillation) input pin	48	26	L9	38	30
	X0A	Sub clock (oscillation) input pin	36	14	L3	26	19
	X1	Main clock (oscillation) I/O pin	49	27	L10	39	31
	X1A	Sub clock (oscillation) I/O pin	37	15	K3	27	20
	CROUT_0	Built-in high-speed CR-osc clock output port	74	52	C10	60	-
	CROUT_1		92	70	B5	72	57
Analog Power	AVCC	A/D converter analog power supply pin	60	38	H11	50	41
	AVRH	A/D converter analog reference voltage input pin	61	39	F11	51	42
Analog GND	AVSS	A/D converter GND pin	62	40	G11	52	43
C pin	C	Power supply stabilization capacity pin	33	11	L2	23	17

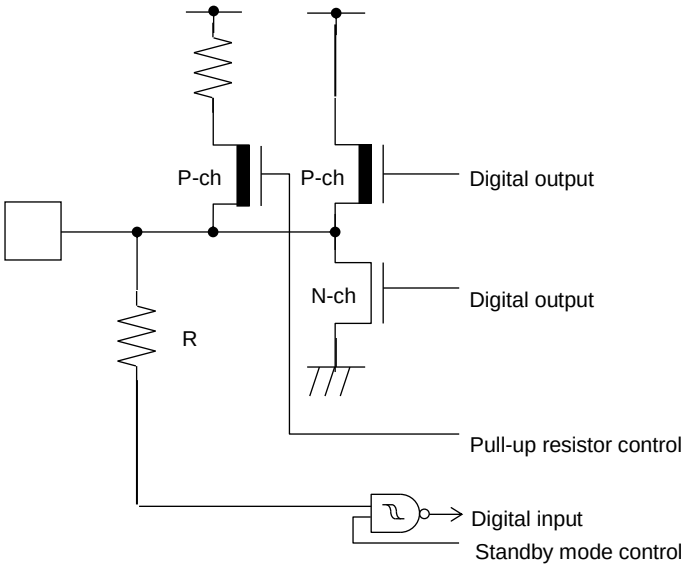
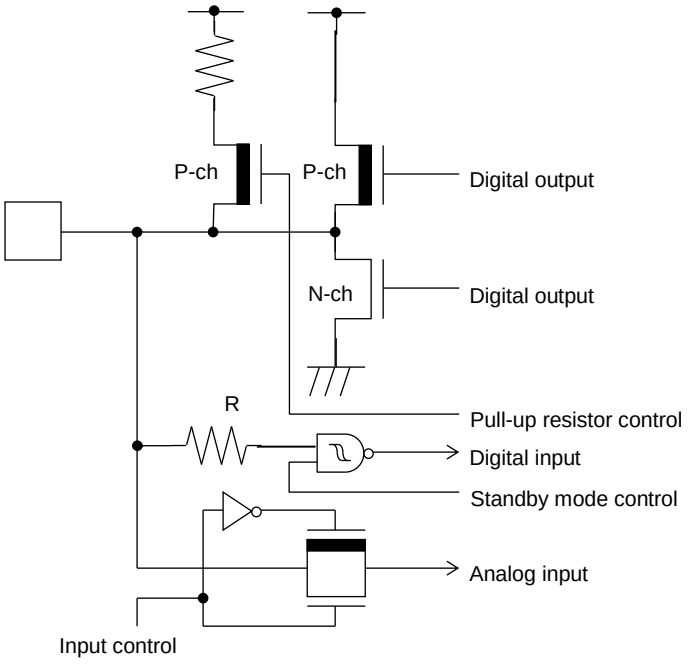
Note:

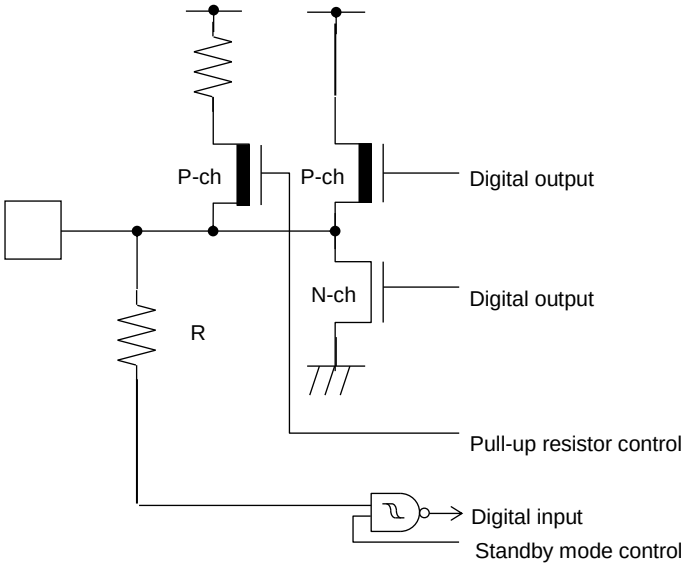
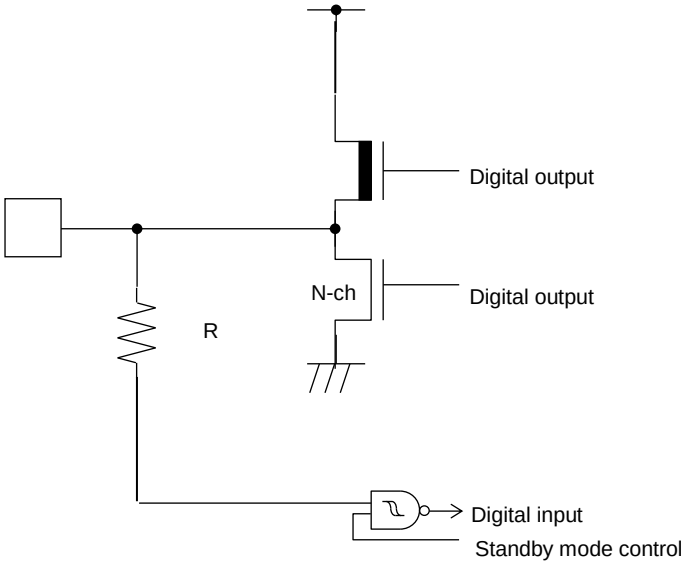
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

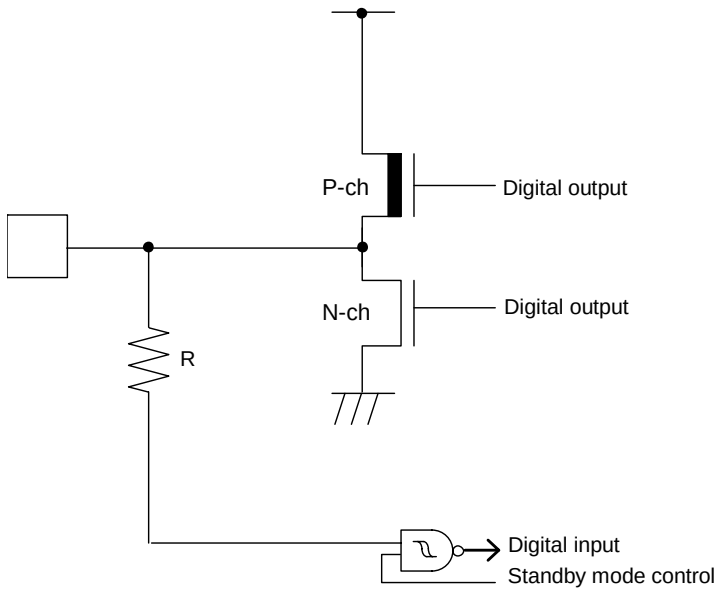
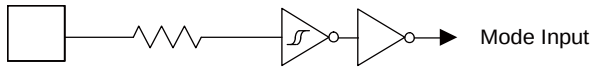
5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}=-4 mA, I_{OL}=4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}=-4 mA, I_{OL}=4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}=-12 mA, I_{OL}= 12 mA • +B input is available
H		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With standby mode control • I_{OH}=-4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

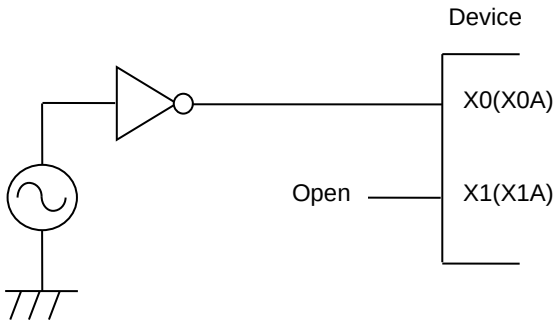
It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Using an external clock

When using an external clock, the clock signal should be driven to the X0, X0A pin only and the X1,X1A pin should be kept open.

- **Example of Using an External Clock**

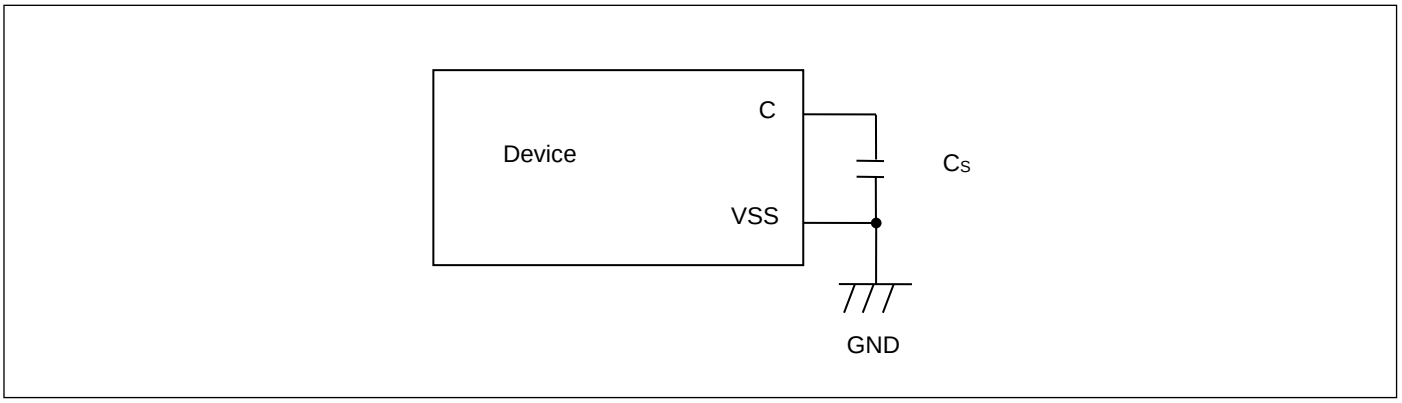


Handling when using Multi-function serial pin as I²C pin

If it is using the multi function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistor stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

Serial Communication

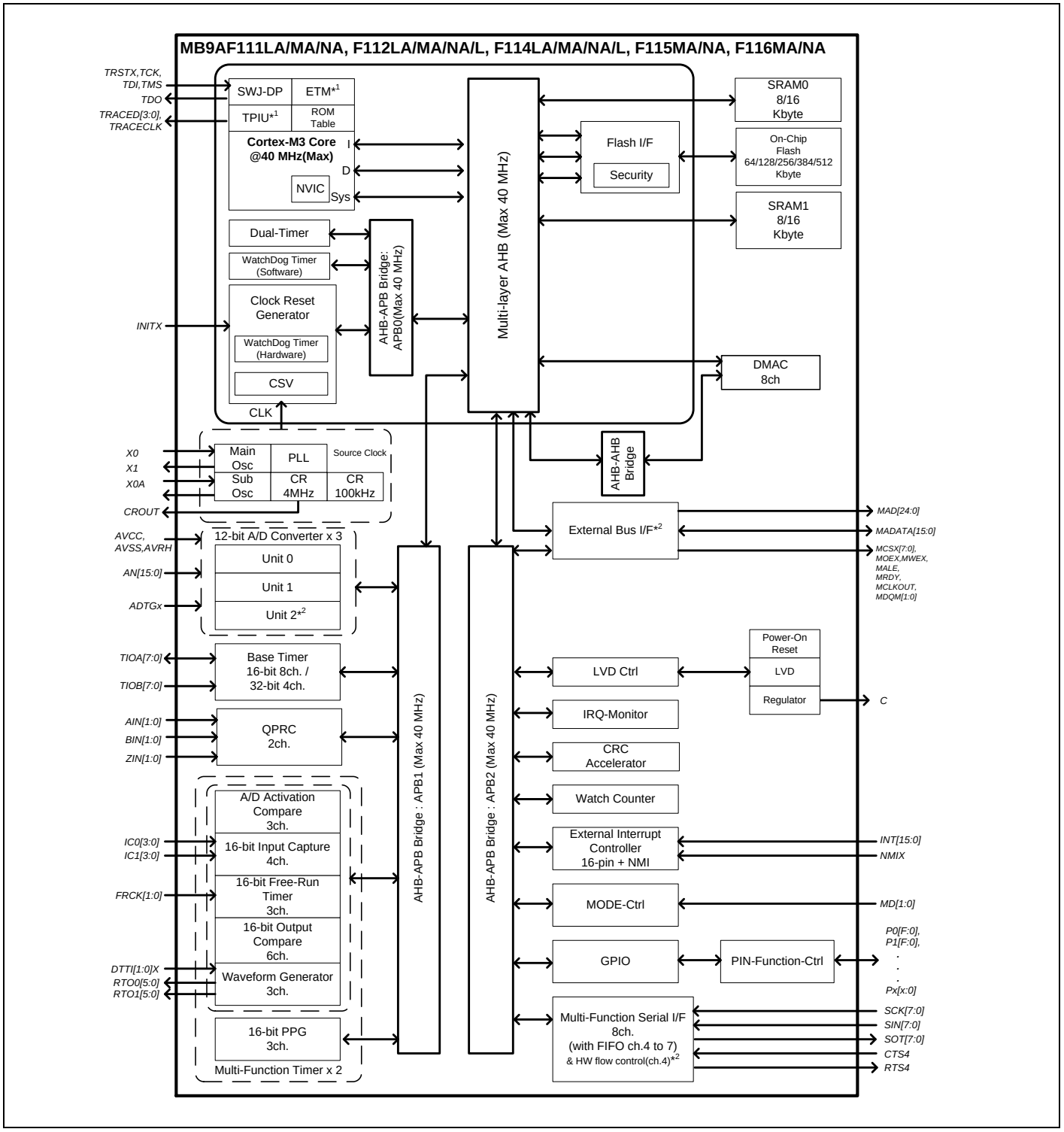
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

8. Block Diagram



*1: For the MB9AF111LA/MA, F112LA/MA, MB9AF114LA/MA, MB9AF115MA and MB9AF116MA, ETM is not available.

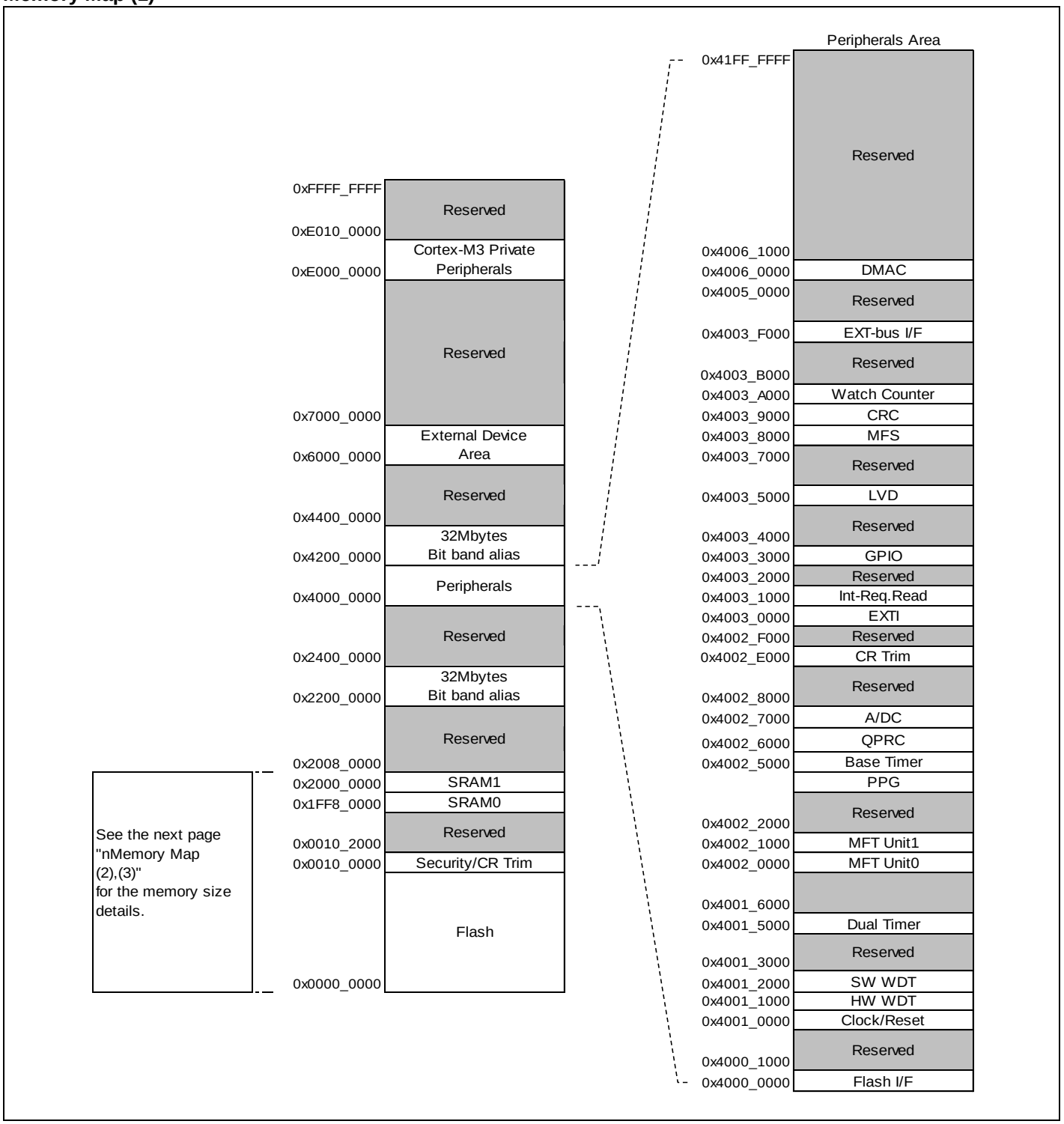
*2: For the MB9AF111LA, F112LA and MB9AF114LA, the External Bus Interface and 12-bit A/D Converter (unit 2) are not available. And the Multi-function Serial Interface does not support hardware flow control in these products.

9. Memory Size

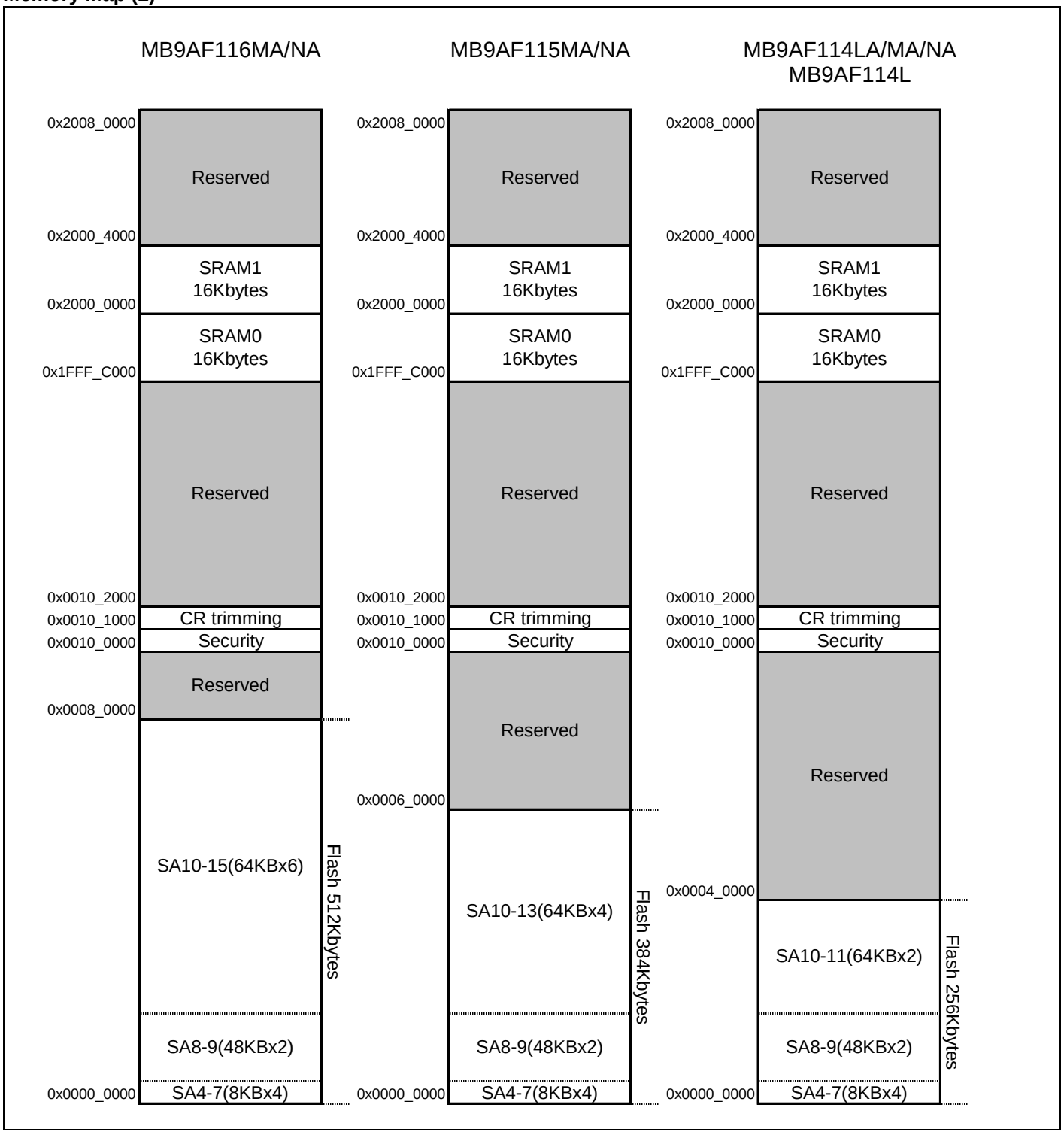
See “Memory Size” in “1. Product Lineup” to confirm the memory size.

10. Memory Map

Memory Map (1)

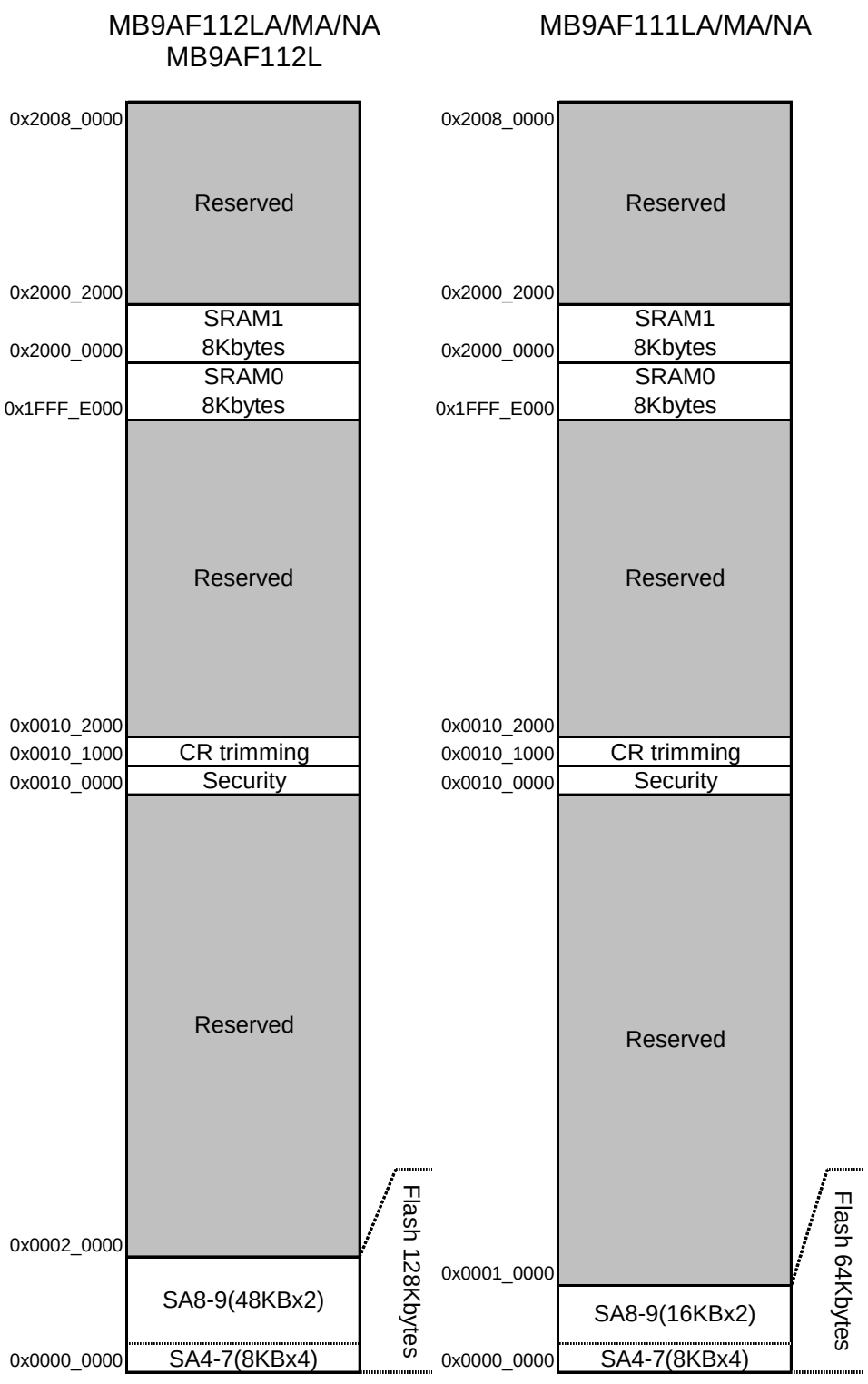


Memory Map (2)



See "MB9A310A/110A Series Flash programming Manual" for sector structure of Flash.

Memory Map (3)



See "MB9A310A/110A Series Flash programming Manual" for sector structure of Flash.

Peripheral Address Map

Start address	End address	Bus	Peripherals
$0x4000_0000_H$	$0x4000_0FFF_H$	AHB	Flash Memory I/F register
$0x4000_1000_H$	$0x4000_FFFF_H$		Reserved
$0x4001_0000_H$	$0x4001_0FFF_H$	APB0	Clock/Reset Control
$0x4001_1000_H$	$0x4001_1FFF_H$		Hardware Watchdog timer
$0x4001_2000_H$	$0x4001_2FFF_H$		Software Watchdog timer
$0x4001_3000_H$	$0x4001_4FFF_H$		Reserved
$0x4001_5000_H$	$0x4001_5FFF_H$		Dual-Timer
$0x4001_6000_H$	$0x4001_FFFF_H$		Reserved
$0x4002_0000_H$	$0x4002_0FFF_H$	APB1	Multi-function timer unit0
$0x4002_1000_H$	$0x4002_1FFF_H$		Multi-function timer unit1
$0x4002_2000_H$	$0x4002_3FFF_H$		Reserved
$0x4002_4000_H$	$0x4002_4FFF_H$		PPG
$0x4002_5000_H$	$0x4002_5FFF_H$		Base Timer
$0x4002_6000_H$	$0x4002_6FFF_H$		Quadrature Position/Revolution Counter(QPRC)
$0x4002_7000_H$	$0x4002_7FFF_H$		A/D Converter
$0x4002_8000_H$	$0x4002_DFFF_H$		Reserved
$0x4002_E000_H$	$0x4002_EFFF_H$		Built-in CR trimming
$0x4002_F000_H$	$0x4002_FFFF_H$		Reserved
$0x4003_0000_H$	$0x4003_0FFF_H$	APB2	External Interrupt
$0x4003_1000_H$	$0x4003_1FFF_H$		Interrupt Source Check Register
$0x4003_2000_H$	$0x4003_2FFF_H$		Reserved
$0x4003_3000_H$	$0x4003_3FFF_H$		GPIO
$0x4003_4000_H$	$0x4003_4FFF_H$		Reserved
$0x4003_5000_H$	$0x4003_5FFF_H$		Low-Voltage Detector
$0x4003_6000_H$	$0x4003_6FFF_H$		Reserved
$0x4003_7000_H$	$0x4003_7FFF_H$		Reserved
$0x4003_8000_H$	$0x4003_8FFF_H$		Multi-function serial Interface
$0x4003_9000_H$	$0x4003_9FFF_H$		CRC
$0x4003_A000_H$	$0x4003_AFFF_H$		Watch Counter
$0x4003_B000_H$	$0x4003_EFFF_H$		Reserved
$0x4003_F000_H$	$0x4003_FFFF_H$		External Bus interface
$0x4004_0000_H$	$0x4004_FFFF_H$	AHB	Reserved
$0x4005_0000_H$	$0x4005_FFFF_H$		Reserved
$0x4006_0000_H$	$0x4006_0FFF_H$		DMAC register
$0x4006_1000_H$	$0x4006_1FFF_H$		Reserved
$0x4006_2000_H$	$0x4006_2FFF_H$		Reserved
$0x4006_3000_H$	$0x4006_3FFF_H$		Reserved
$0x4006_4000_H$	$0x41FF_FFFF_H$		Reserved

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the "L" level.

- INITX=1

  This is the period when the INITX pin is the "H" level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at "0"

  This is the status that the input function cannot be used. Internal input is fixed at "L".

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enable	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enabled	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"
O	GPIO pin	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/Input enabled

*1: Oscillation is stopped at sub timer mode, low-speed CR timer mode, and stop mode.

*2: Oscillation is stopped at stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	$\Sigma [I_{CLAMP}]$		+20	mA	*7
"L" level maximum output current*4	I_{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80, P81
"L" level average output current*5	I_{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			18.5	mA	P80, P81
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*4	I_{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80, P81
"H" level average output current*5	I_{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 20.5	mA	P80, P81
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Be careful not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

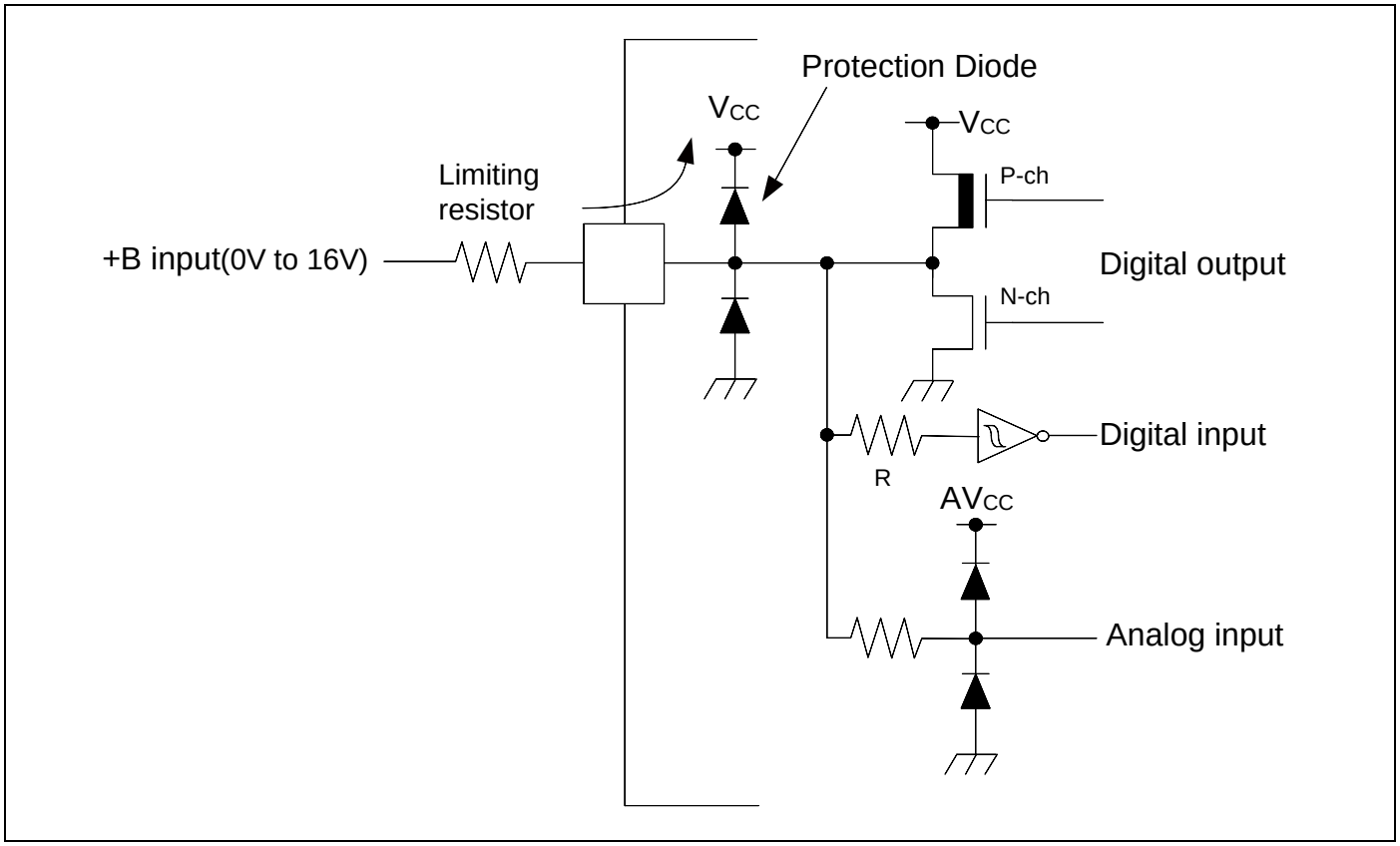
*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

*7:

- See “4. List of Pin Functions” and “5. I/O Circuit Type” about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

- *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7*2	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage		AVRH	-	2.7	AV_{CC}	V	
Smoothing capacitor		C_S	-	1	10	µF	For built-in regulator*1
Operating temperature	LQI100 LQH080 LQD064 LQG064 VNC064 LBC112	T_A	-	- 40	+ 105	°C	
	PQH100	T_A	When mounted on four-layer PCB	- 40	+ 105	°C	
			When mounted on double-sided single-layer PCB	- 40	+ 105	°C	I_{CC} ≤ 35 mA
				- 40	+ 85	°C	I_{CC} > 35 mA

*1: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
  Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3 DC Characteristics

12.3.1 Current rating

(V_{CC} = AV_{CC}= 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*3	Max*4		
RUN mode current	I_{CC}	VCC	PLL RUN mode	CPU: 40 MHz, Peripheral: 40 MHz, Flash 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *5	32	41	mA	*1
				CPU: 40 MHz, Peripheral: 40 MHz, Flash 3 Wait FRWTR.RWT = 00 FSYNDN.SD = 011 *5	21	28	mA	*1
			High-speed CR RUN mode	CPU/ Peripheral: 4 MHz *2 Flash 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	3.9	7.7	mA	*1
			Sub RUN mode	CPU/ Peripheral: 32 kHz Flash 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *6	0.15	3.2	mA	*1
			Low-speed CR RUN mode	CPU/ Peripheral: 100 kHz Flash 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.2	3.3	mA	*1
SLEEP mode current	I_{CCS}		PLL SLEEP mode	Peripheral: 40 MHz *5	10	15	mA	*1
			High-speed CR SLEEP mode	Peripheral: 4 MHz *2	1.2	4.4	mA	*1
			Sub SLEEP mode	Peripheral: 32 kHz *6	0.1	3.1	mA	*1
			Low-speed CR SLEEP mode	Peripheral: 100 kHz	0.1	3.1	mA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A =+25°C, V_{CC}=5.5 V

*4: T_A =+105°C, V_{CC}=5.5 V

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
TIMER mode current	I_{CCT}	VCC	Main TIMER mode	T_A = + 25°C, When LVD is off *3	2.5	3	mA	*1
				T_A = + 105°C, When LVD is off *3	-	6	mA	*1
			Sub TIMER mode	T_A = + 25°C, When LVD is off *4	60	230	µA	*1
				T_A = + 105°C, When LVD is off *4	-	3.1	mA	*1
STOP mode current	I_{CCH}		STOP mode	T_A = + 25°C, When LVD is off	35	200	µA	*1
				Ta = + 105°C, When LVD is off	-	3	mA	*1

*1: When all ports are fixed.

*2: V_{CC}=5.5 V

*3: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt Vcc = 5.5 V	4	7	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	11.4	13.1	mA	

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.57	0.72	mA	
			At stop	0.06	20	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.96	mA	
			At stop	0.06	4	µA	

12.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0,1	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5V tolerant I/O pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0,1	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
"H" level output voltage	V_{OH}	4mA type	Vcc ≥ 4.5 V I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			Vcc < 4.5 V I_{OH} = - 2 mA					
		12mA type	Vcc ≥ 4.5 V I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			Vcc < 4.5 V I_{OH} = - 8 mA					
		P80, P81	Vcc ≥ 4.5 V I_{OH} = - 20.5 mA	V_{CC} - 0.4	-	V_{CC}	V	
			Vcc < 4.5 V I_{OH} = - 13.0 mA					
"L" level output voltage	V_{OL}	4mA type	Vcc ≥ 4.5 V I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 2 mA					
		12mA type	Vcc ≥ 4.5 V I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 8 mA					
		P80, P81	Vcc ≥ 4.5 V I_{OL} = 18.5 mA	V_{SS}	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 10.5 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	Vcc≥ 4.5 V	25	50	100	kΩ	
			V_{CC}<4.5 V	30	80	200		
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

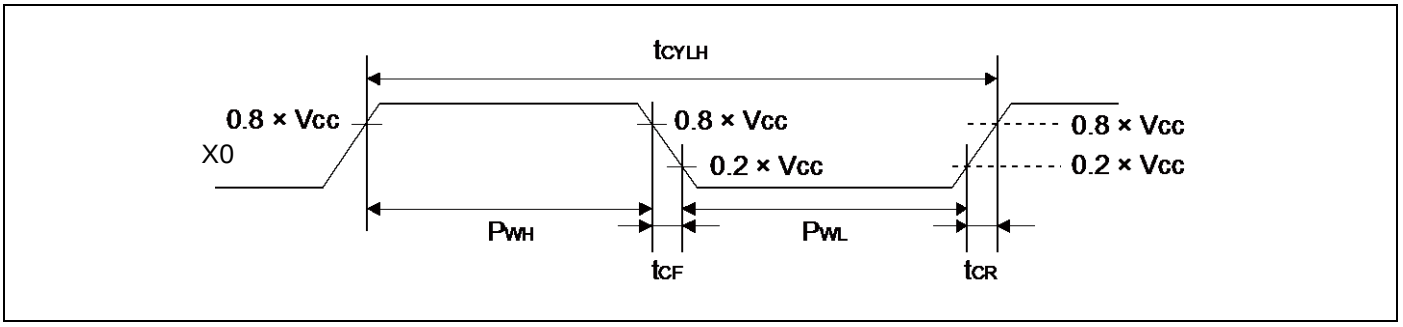
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0 X1	V_{CC}≥ 4.5 V	4	48	MHz	When crystal oscillator is connected
			V_{CC}<4.5 V	4	20		
			V_{CC}≥ 4.5 V	4	48	MHz	When using external clock
			V_{CC}<4.5 V	4	20		
Input clock cycle	t_{CYLH}		V_{CC}≥ 4.5 V	20.83	250	ns	When using external clock
			V_{CC}<4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF} t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	40	MHz	Master clock
	F_{CC}	-	-	-	40	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	25	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

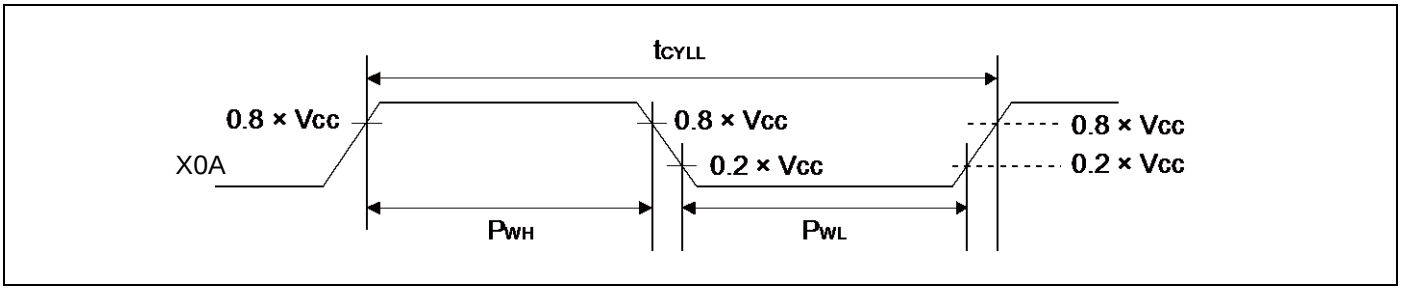
*2: For about each APB bus which each peripheral is connected to, see "8. Block Diagram" in this datasheet.



12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL} P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(Vcc = 2.7V to 5.5V, Vss = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	T_A = + 25°C	3.96	4	4.04	MHz	When trimming *1
		T_A = 0°C to + 70°C	3.84	4	4.16		
		T_A = - 40°C to + 105°C	3.8	4	4.2		
		T_A = - 40°C to + 105°C	3	4	5		When not trimming
Frequency stability time	t_{CRWT}	-	-	-	90	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: Frequency stable time is time to stable of the frequency of the High-speed CR.
clock after the trim value is set. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time) *1	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	300	MHz	
Main PLL clock frequency *2	F_{CLKPLL}	-	-	40	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

12.4.5 Operating Conditions of Main PLL (In the case of using the built-in high speed CR for the input clock of the main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

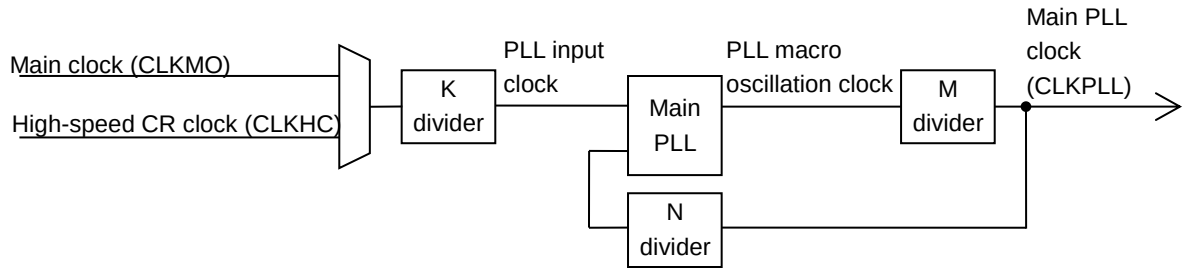
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time) *1	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	50	-	71	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	300	MHz	
Main PLL clock frequency *2	F_{CLKPLL}	-	-	40	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection



12.4.6 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{SS} = 0V, T_A = - 40°C to + 105°C)

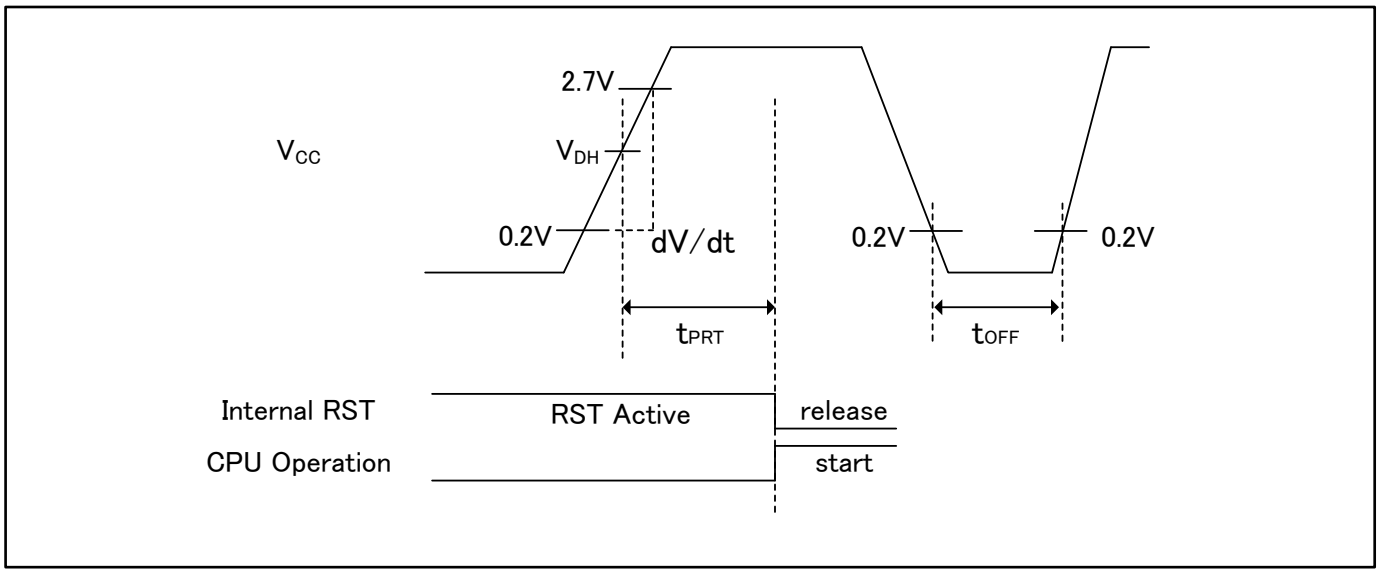
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	50	-	-	ms	*1
Power ramp rate	dV/dt		Vcc:0.2 V to 2.70 V	0.9	-	1000	mV/us	*2
Time until releasing Power-on reset	t_{PRT}		-	0.446	-	0.744	ms	

*1: V_{CC} must be held below 0.2 V for minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>50 ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 6.*



Glossary

VDH: detection voltage of Low Voltage detection reset. See "12.6. Low-voltage detection characteristics"

12.4.8 External Bus Timing

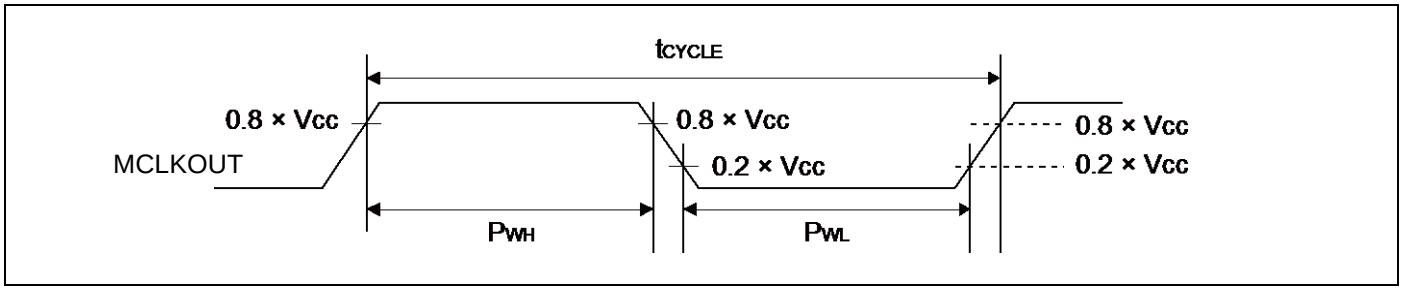
External bus clock output characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT	$V_{CC} \geq 4.5$ V	-	40	MHz
			$V_{CC} < 4.5$ V	-	32	MHz
Minimum clock cycle time	-		$V_{CC} \geq 4.5$ V	25	-	ns
			$V_{CC} < 4.5$ V	31.25	-	ns

Note:

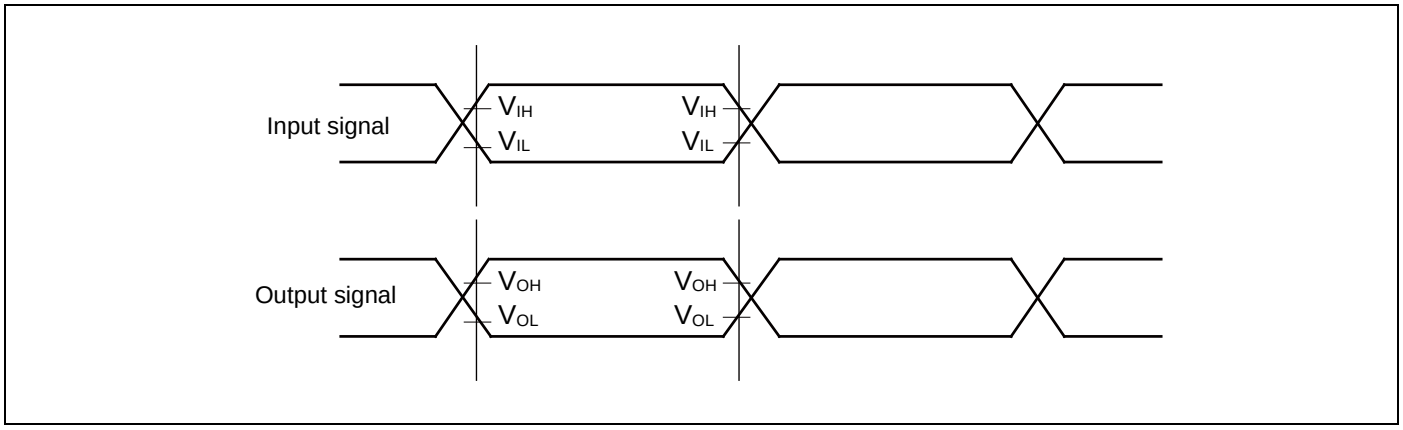
- *The external bus clock output is a divided clock of HCLK. For more information about setting of clock divider, see "Chapter 12: External Bus Interface" in "FM3 Family Peripheral Manual"*
  When external bus clock is not output, this characteristic does not give any effect on external bus operation.



External bus signal input/output characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



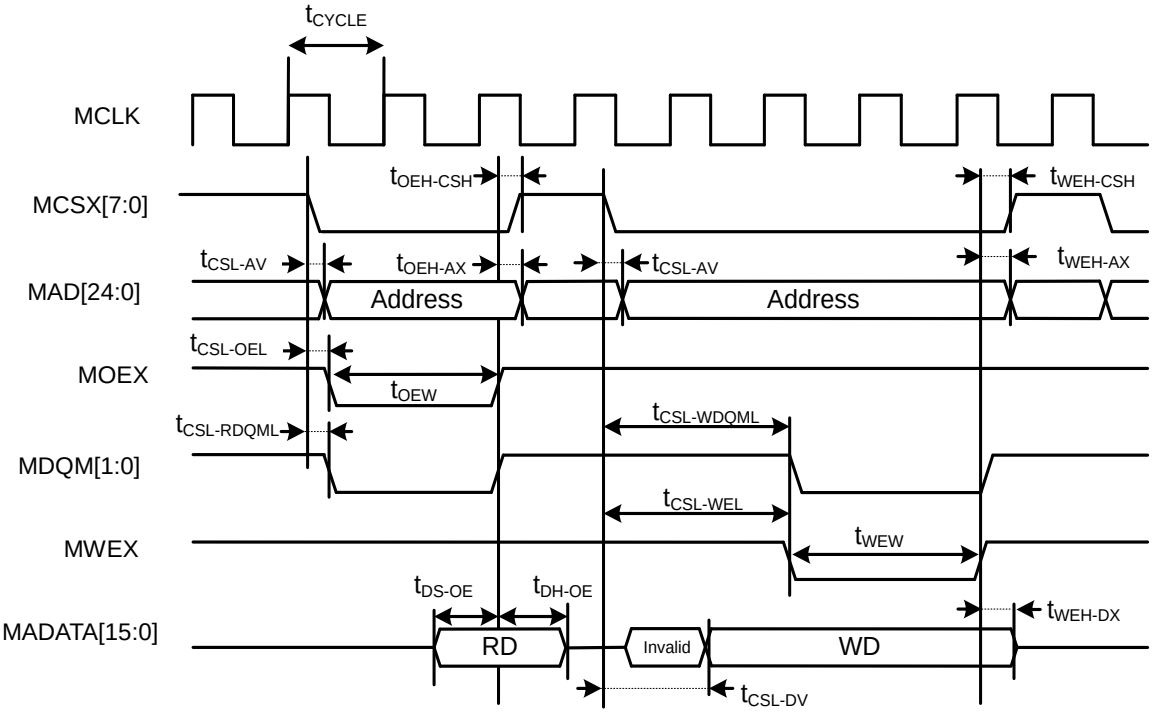
Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MCSX ↓→Address output delay time	t_{CSL-AV}	MCSX[7:0] MAD[24:0]	$V_{CC} \geq 4.5$ V	-9	+ 9	ns
			$V_{CC} < 4.5$ V	-12	+ 12	
MOEX ↑→ Address hold time	t_{OEH-AX}	MOEX MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓→ MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MOEX ↑→ MCSX ↑ time	$t_{OEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓→ MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	t_{DS-OE}	MOEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MOEX ↑→ Data hold time	t_{DH-OE}	MOEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX Min pulse width	t_{WEW}	MWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MWEX ↑→ Address output delay time	t_{WEH-AX}	MWEX MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓→ MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MWEX ↑→ MCSX ↑ delay time	$t_{WEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MCSX ↓ → Data output time	t_{CSL-DV}	MCSX MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK-9	MCLK+9	ns
			$V_{CC} < 4.5$ V	MCLK-12	MCLK+12	
MWEX ↑→ Data hold time	t_{WEH-DX}	MWEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).*


tCYCLE
MCLK
MCSX[7:0]
tOEH-CSH
tWEH-CSH
MAD[24:0]
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
MOEX
tCSL-OEL
tOEW
MDQM[1:0]
tCSL-RDQML
tCSL-WDQML
MWEX
tCSL-WEL
tWEW
MADATA[15:0]
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DV

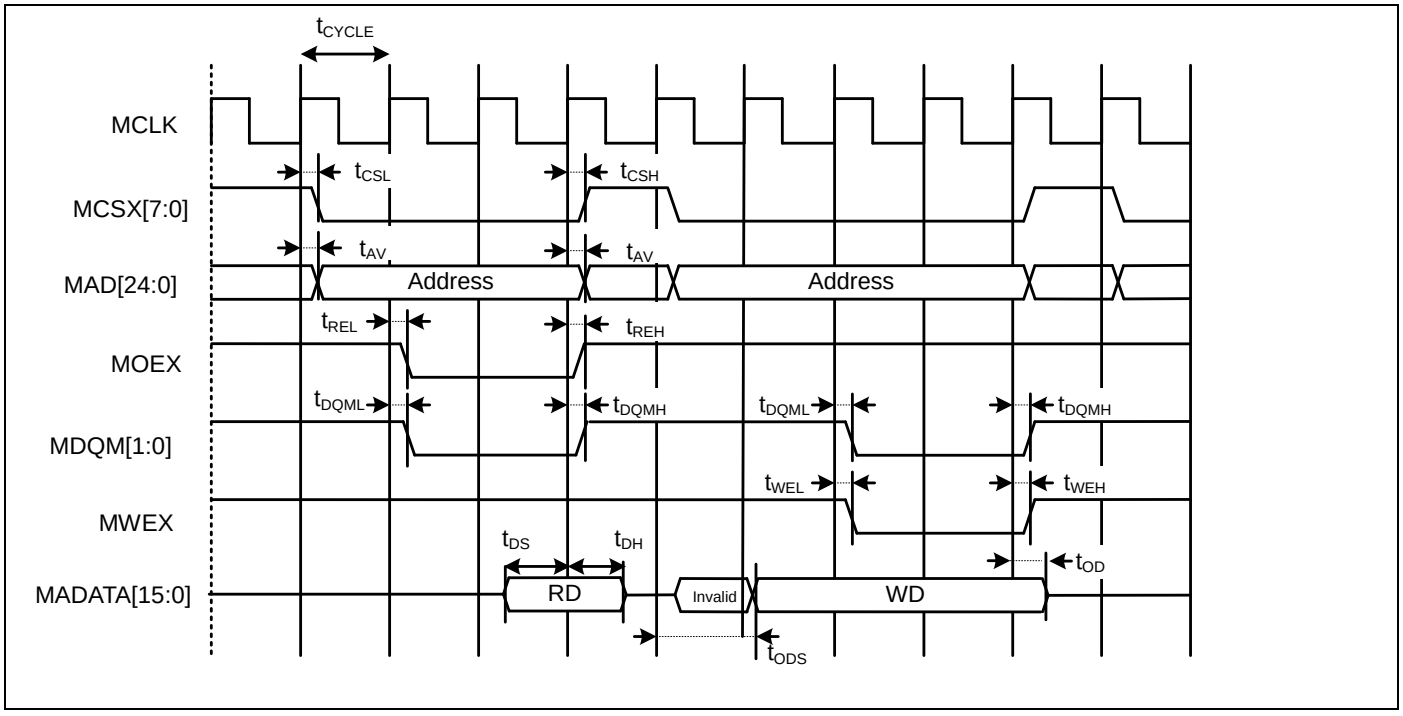
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK MAD[24:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MCSX delay time	t_{CSL}	MCLK MCSX[7:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{CSH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MOEX delay time	t_{REL}	MCLK MOEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{REH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
Data set up→ MCLK ↑time	t_{DS}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	19	-	ns
			$V_{CC} < 4.5$ V	37		
MCLK ↑→ Data hold time	t_{DH}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX delay time	t_{WEL}	MCLK MWEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{WEH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK MDQM[1:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{DQMH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MCLK ↑→ Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK+1	MCLK+18	ns
			$V_{CC} < 4.5$ V		MCLK+24	
MCLK ↑→ Data output time	t_{OD}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	18	ns
			$V_{CC} < 4.5$ V	1	24	

Note:

- *When the external load capacitance C_L = 30 pF.*



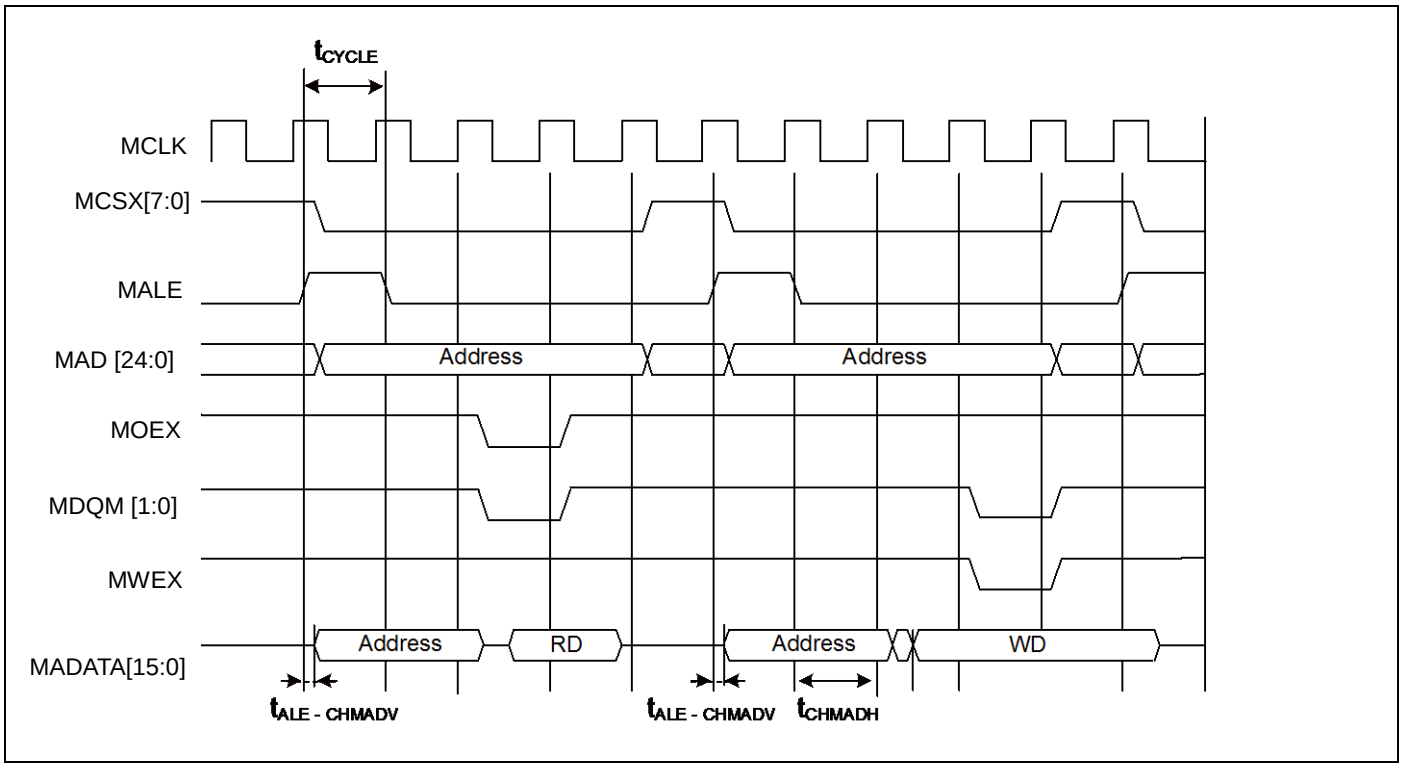
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed Address delay time	$t_{ALE-CHMADV}$	MALE MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	10	ns
			$V_{CC} < 4.5$ V		20	
Multiplexed Address hold time	t_{CHMADH}		$V_{CC} \geq 4.5$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 4.5$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).*



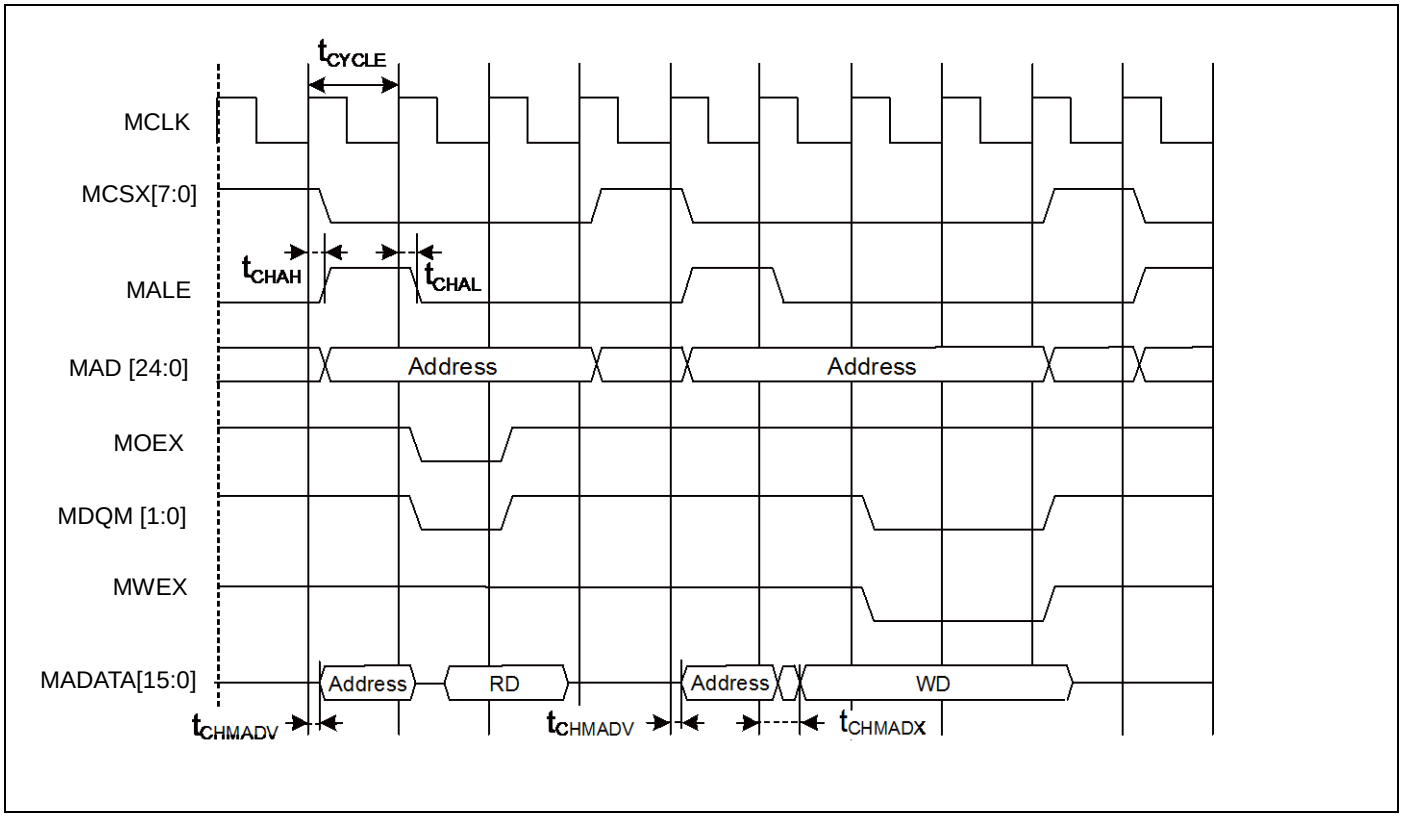
Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK ALE	$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
	t_{CHAH}		$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
MCLK ↑→ Multiplexed Address delay time	t_{CHMADV}	MCLK MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				
MCLK ↑→ Multiplexed Data output time	t_{CHMADX}		$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				

Note:

- *When the external load capacitance C_L = 30 pF.*

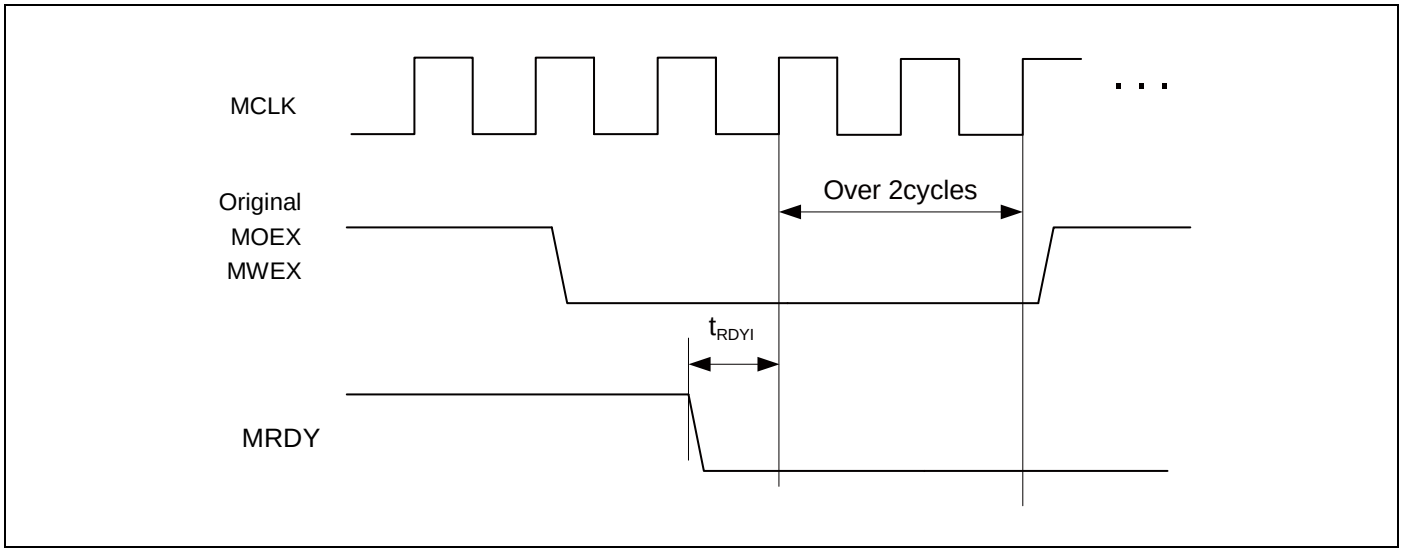


External Ready Input Timing

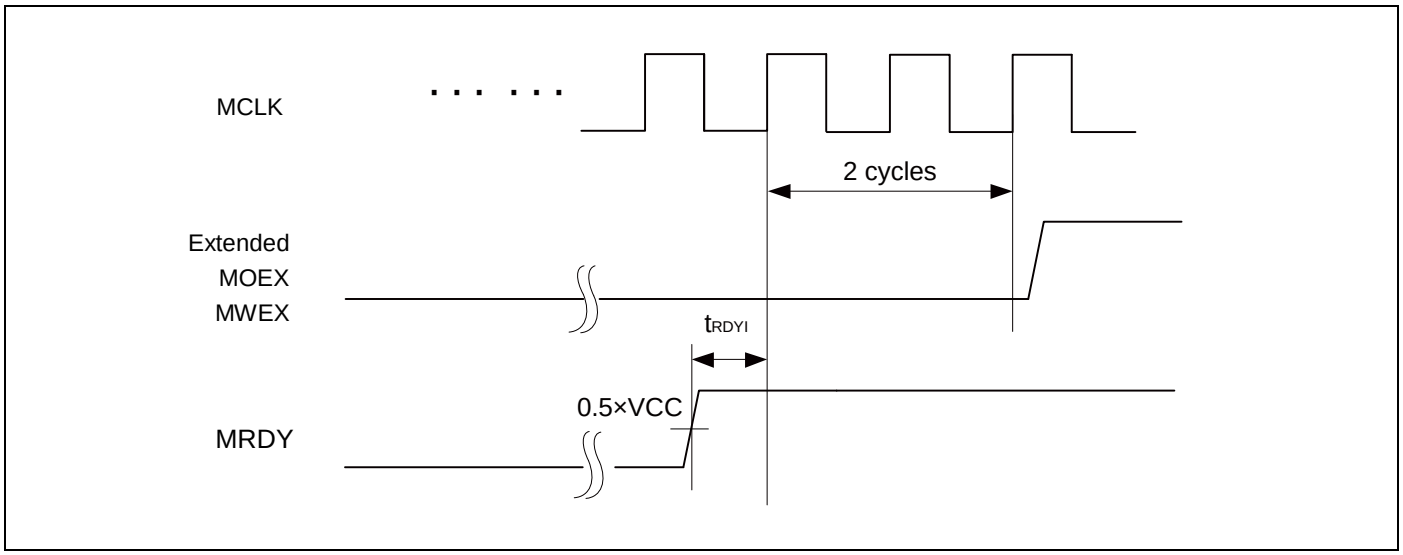
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK ↑ MRDY input setup time	t_{RDYI}	MCLK MRDY	V_{CC} ≥ 4.5 V	19	-	ns	
			V_{CC} < 4.5 V	37			

When RDY is input



When RDY is released

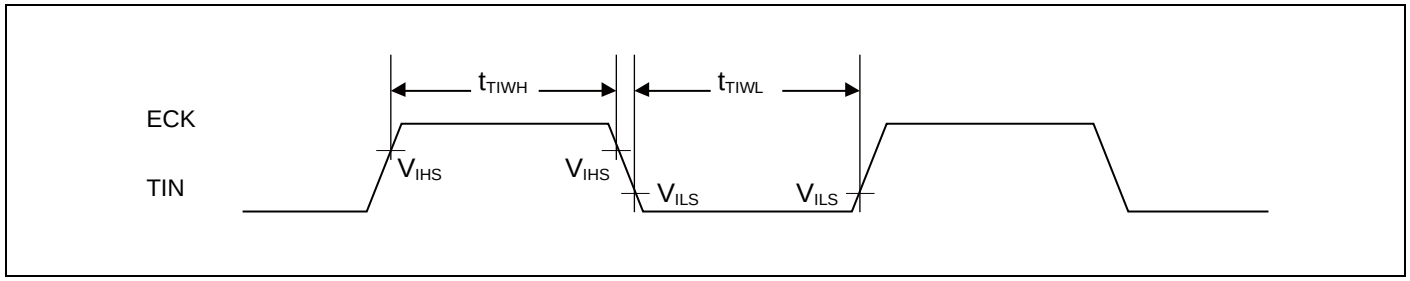


12.4.9 Base Timer Input Timing

Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

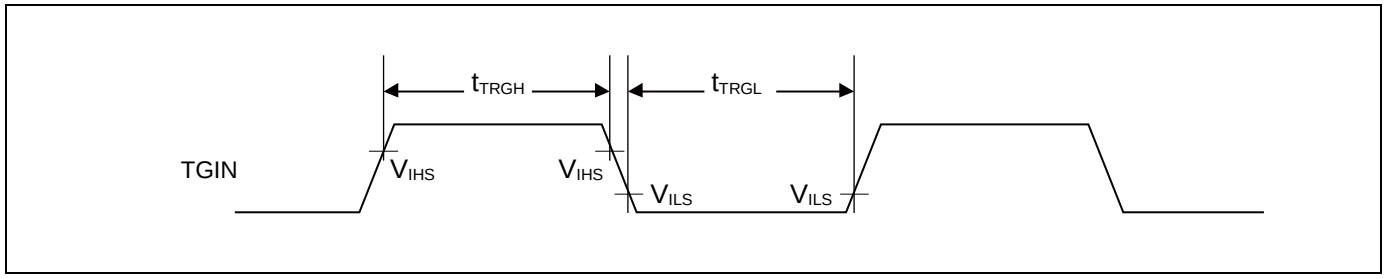
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (when using as ECK,TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see "8. Block Diagram" in this datasheet.

12.4.10 CSIO/UART Timing

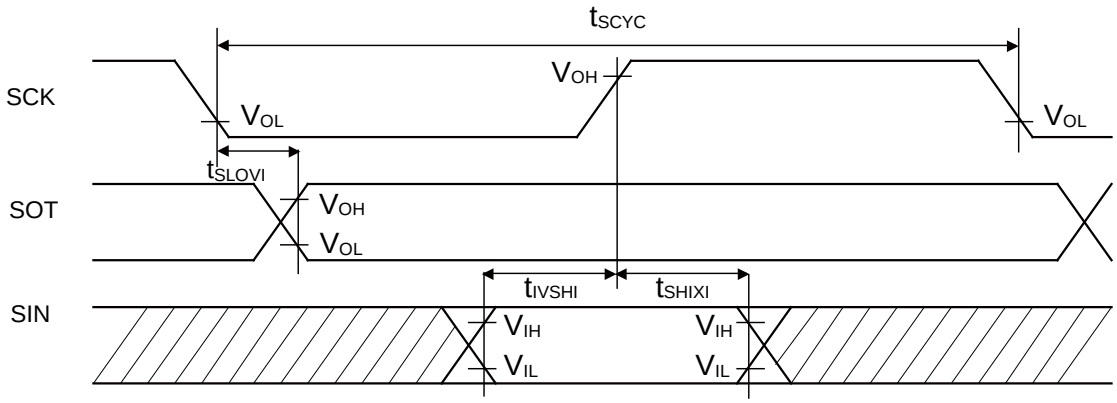
CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

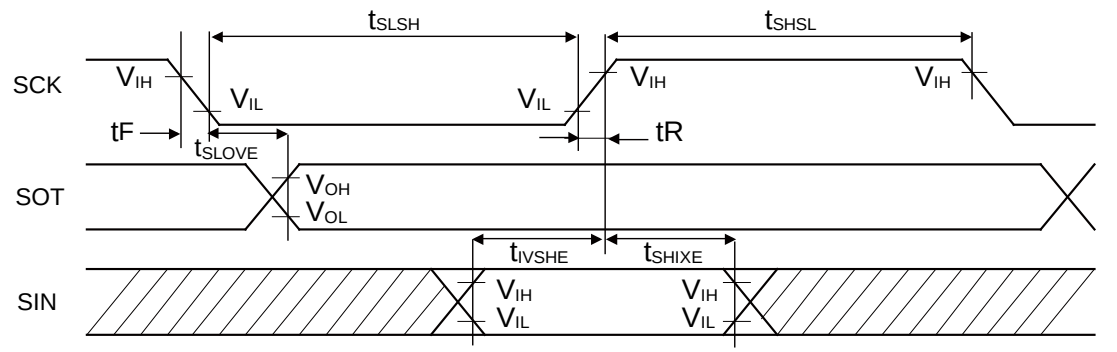
Parameter	Symbol	Pin name	Conditions	V_{CC}<4.5 V		V_{CC}≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑→ SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L= 30 pF.*



Master mode



Slave mode

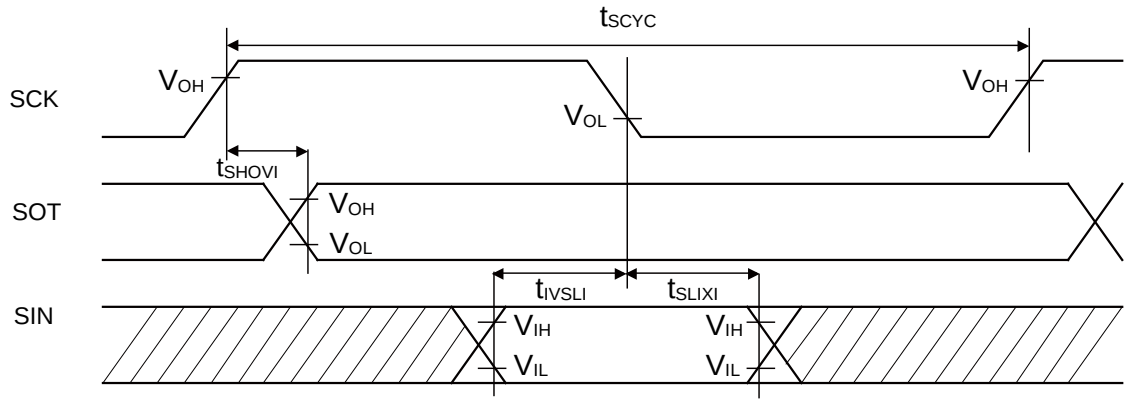
CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

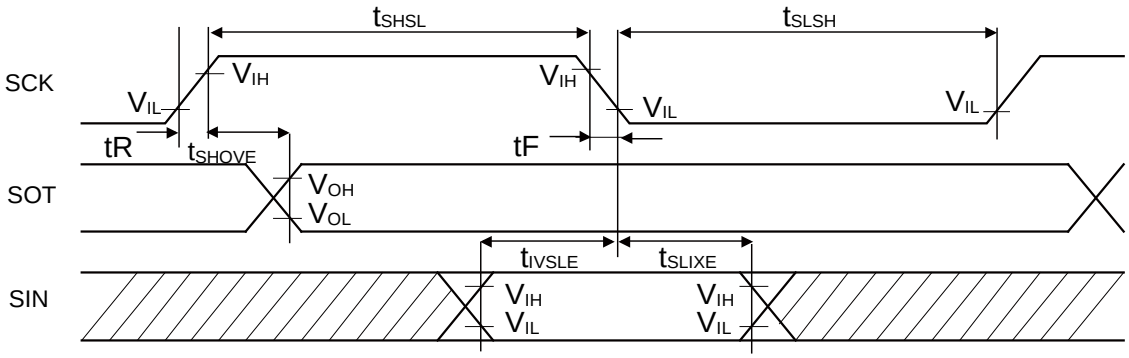
Parameter	Symbol	Pin name	Conditions	V_{CC}<4.5 V		V_{CC}≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCKx SOTx		- 30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑→ SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L= 30 pF.*



Master mode



Slave mode

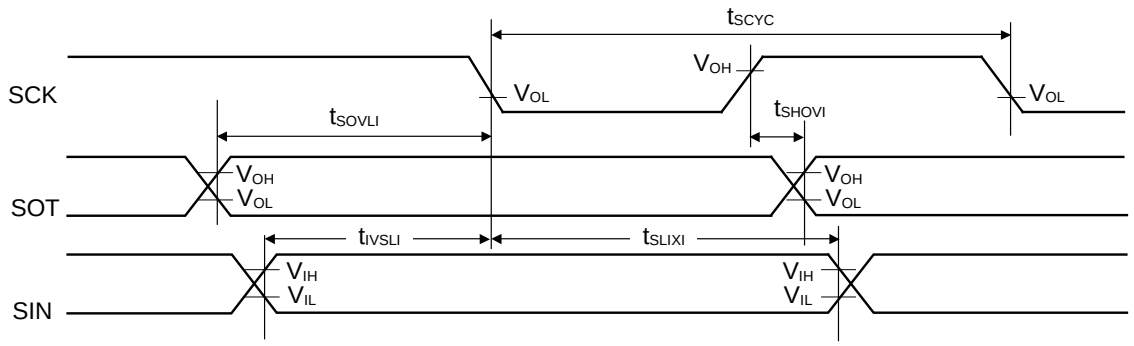
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

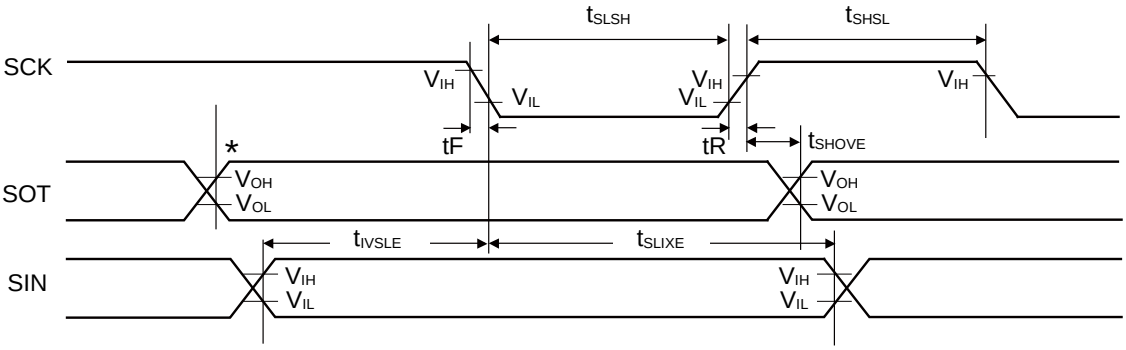
Parameter	Symbol	Pin name	Conditions	V_{CC}<4.5 V		V_{CC}≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L= 30 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

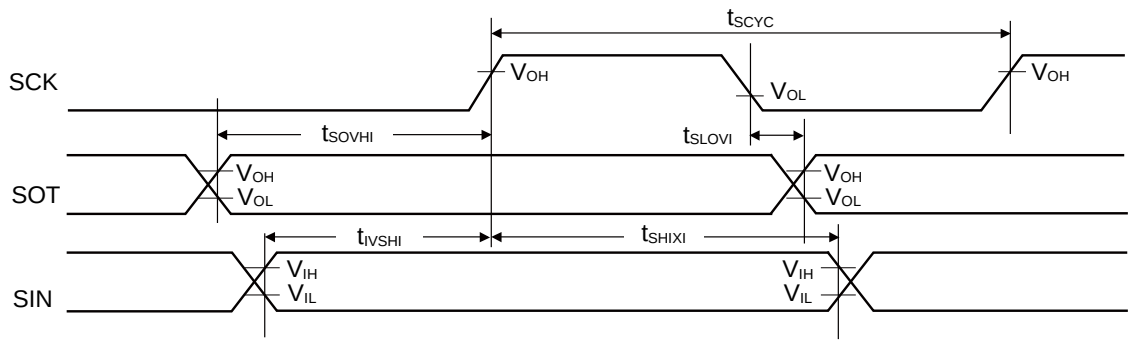
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

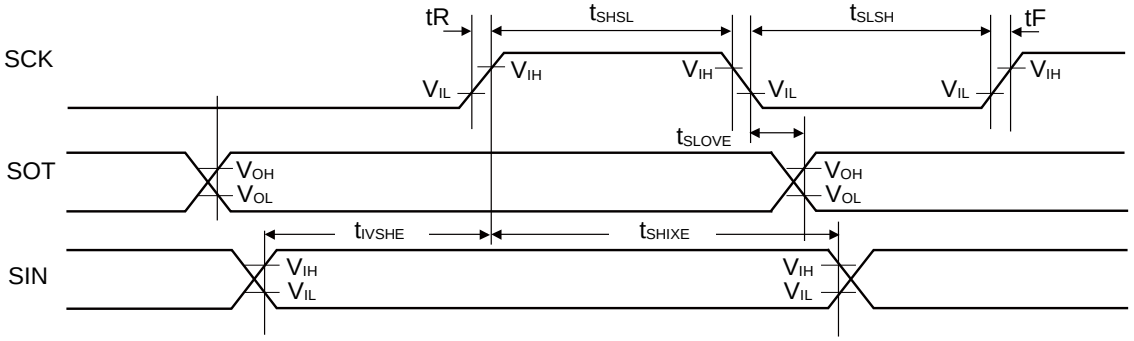
Parameter	Symbol	Pin name	Conditions	V_{CC}<4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓⟶ SOT delay time	t_{SLOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN ⟶ SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑⟶SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
SOT ⟶ SCK ↑ delay time	t_{SOVHI}	SCKx SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ ⟶ SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN ⟶ SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑⟶ SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L= 30 pF.*



Master mode

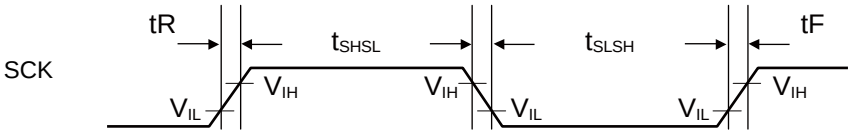


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock "L" pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	

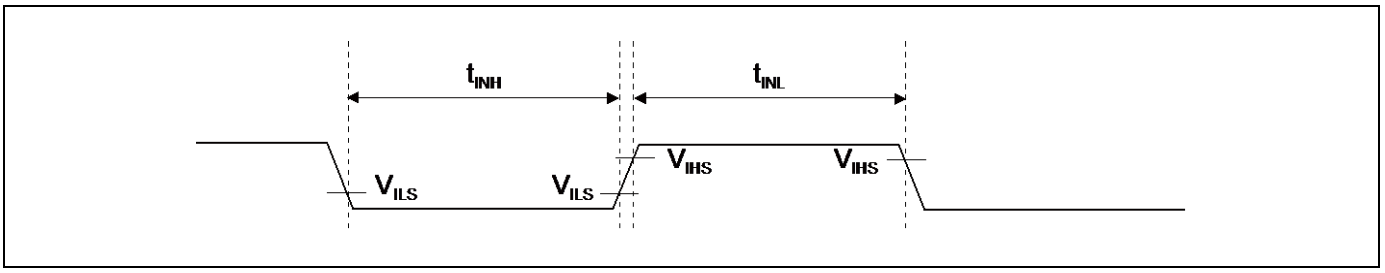


12.4.11 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH} t_{INL}	ADTG	-	$2t_{CYCP}$*	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*	-	ns	Wave form generator
		INTxx, NMIX	Except Timer mode, Stop mode	$2t_{CYCP}$ + 100*	-	ns	External interrupt NMI
			Timer mode, Stop mode	500	-	ns	

*1: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see “8. Block Diagram” in this datasheet.

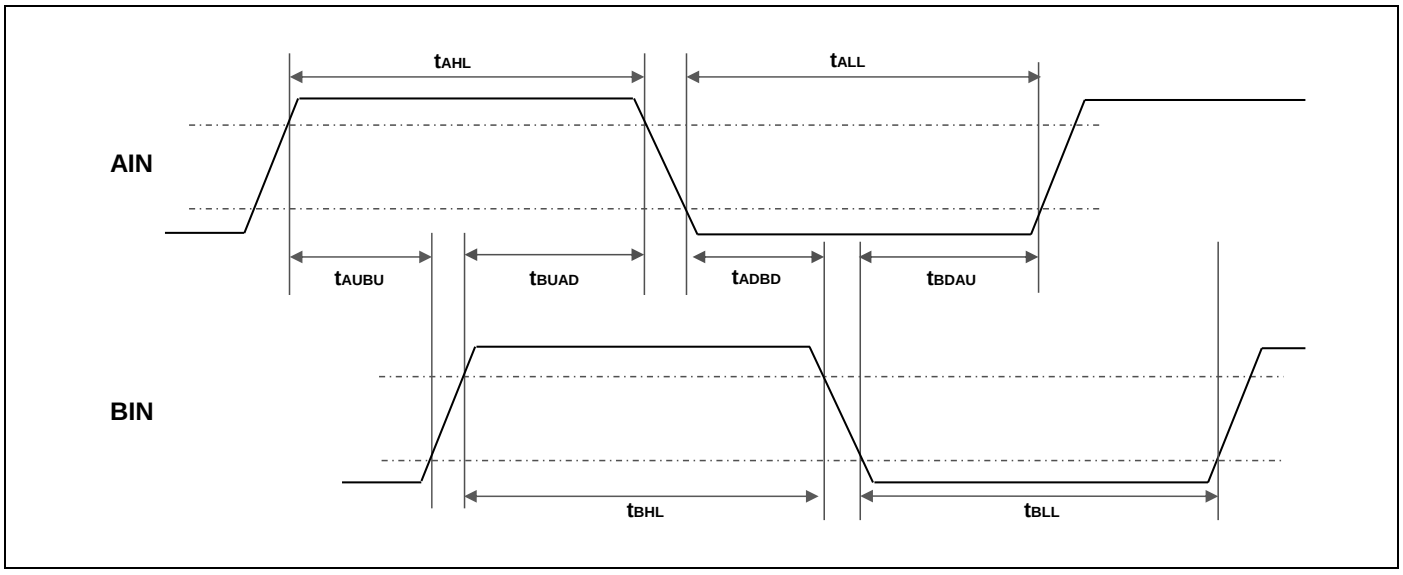


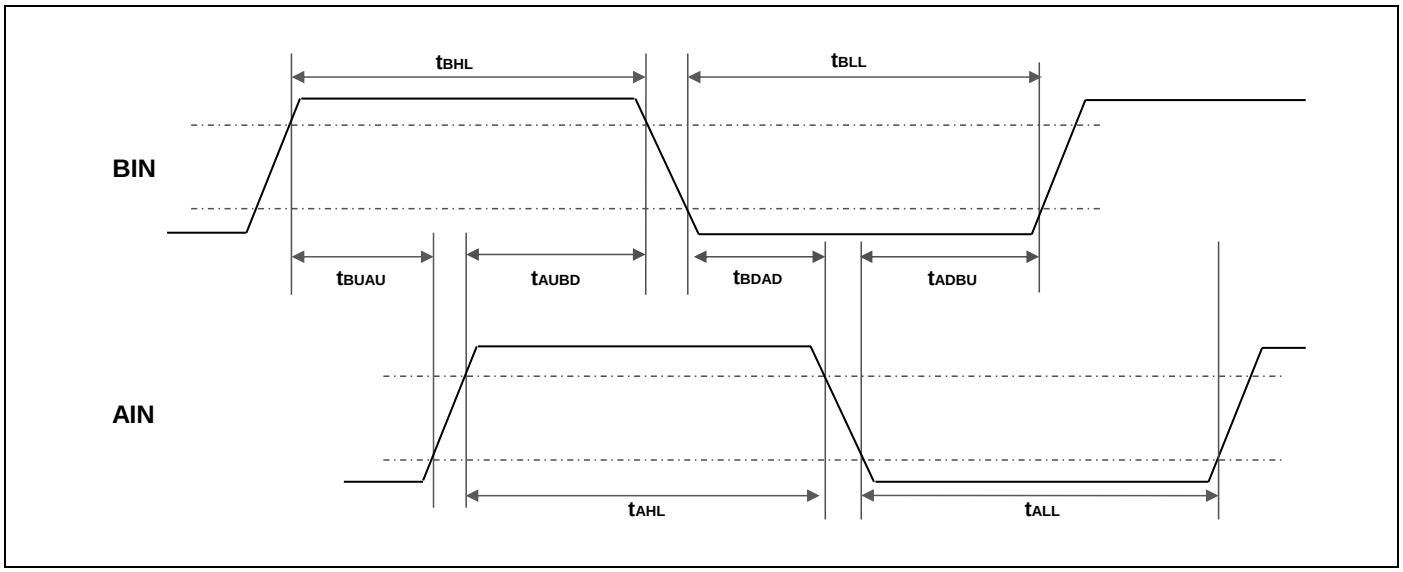
12.4.12 Quadrature Position/Revolution Counter timing

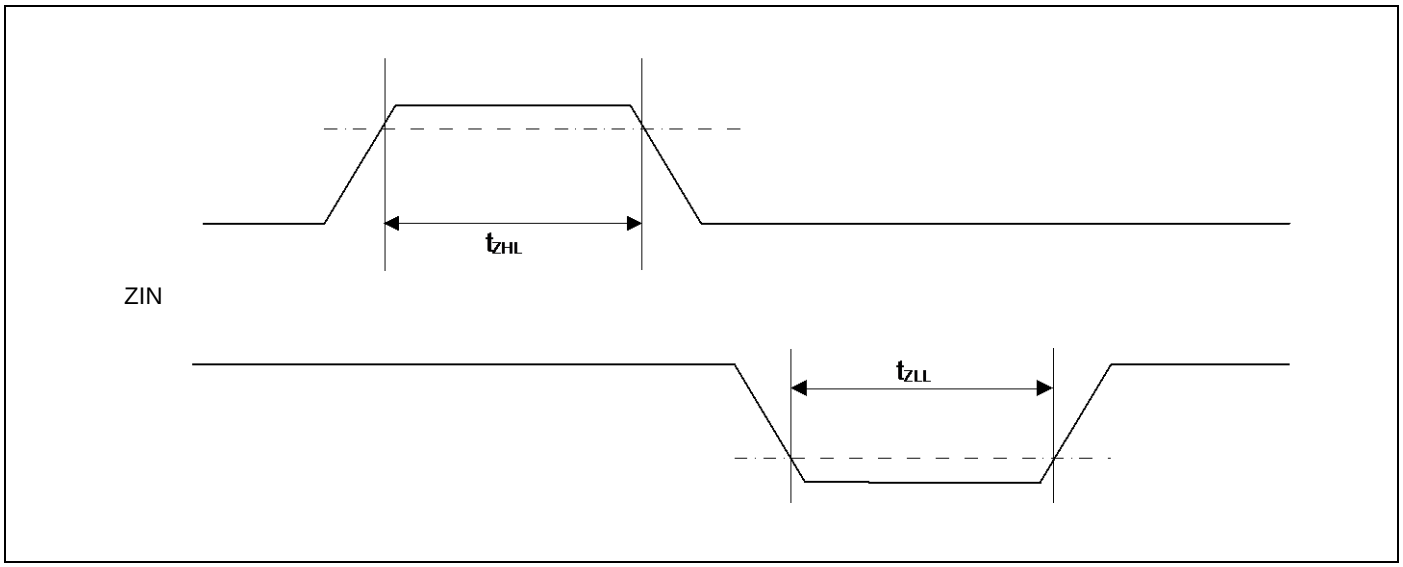
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

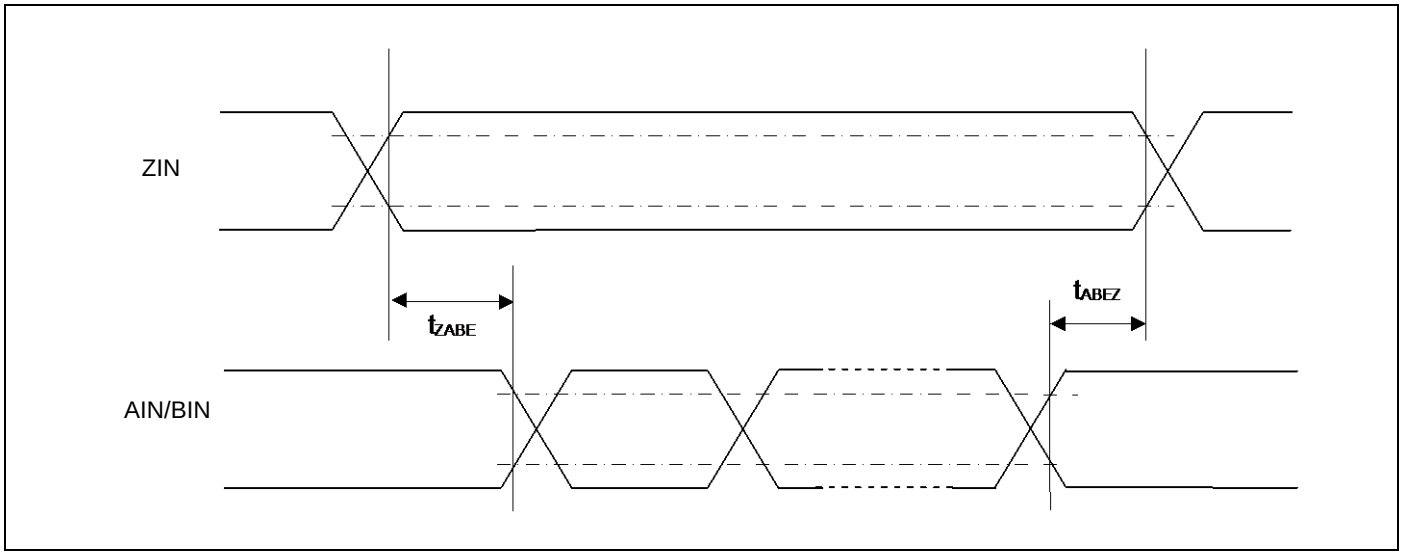
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	$2t_{CYCP}$ *	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rise time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC = "0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC = "0"			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC = "1"			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC = "1"			

*: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8. Block Diagram" in this datasheet.




BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL


ZIN
tZHL
tZLL


ZIN
AIN/BIN
tZABE
tABEZ

12.4.13 I²C Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

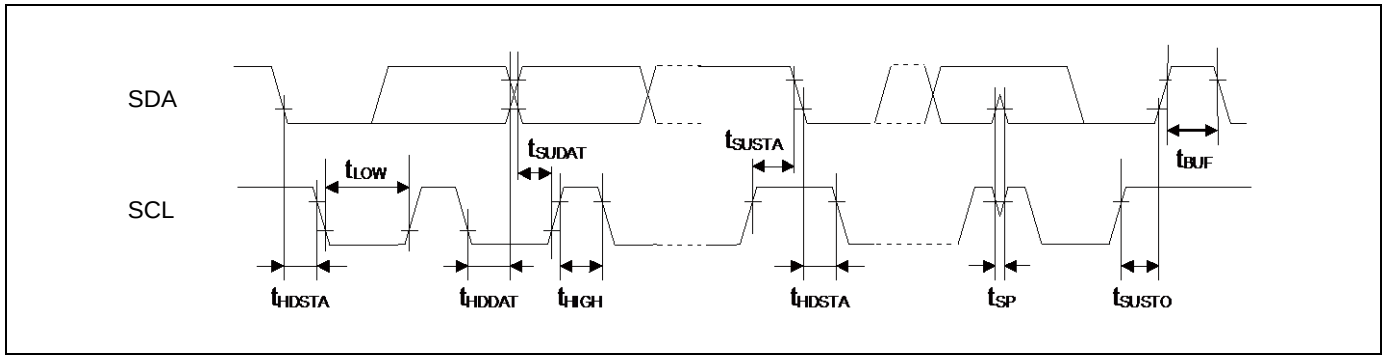
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL}) *1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓→ SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑→ SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓→ SDA ↓↑	t_{HDDAT}		0	3.45 *2	0	0.9 *3	µs	
Data setup time SDA ↓↑→ SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑→ SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: Fast-mode I²C bus device can be used on Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I2C is connected to, see "8. Block Diagram" in this datasheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



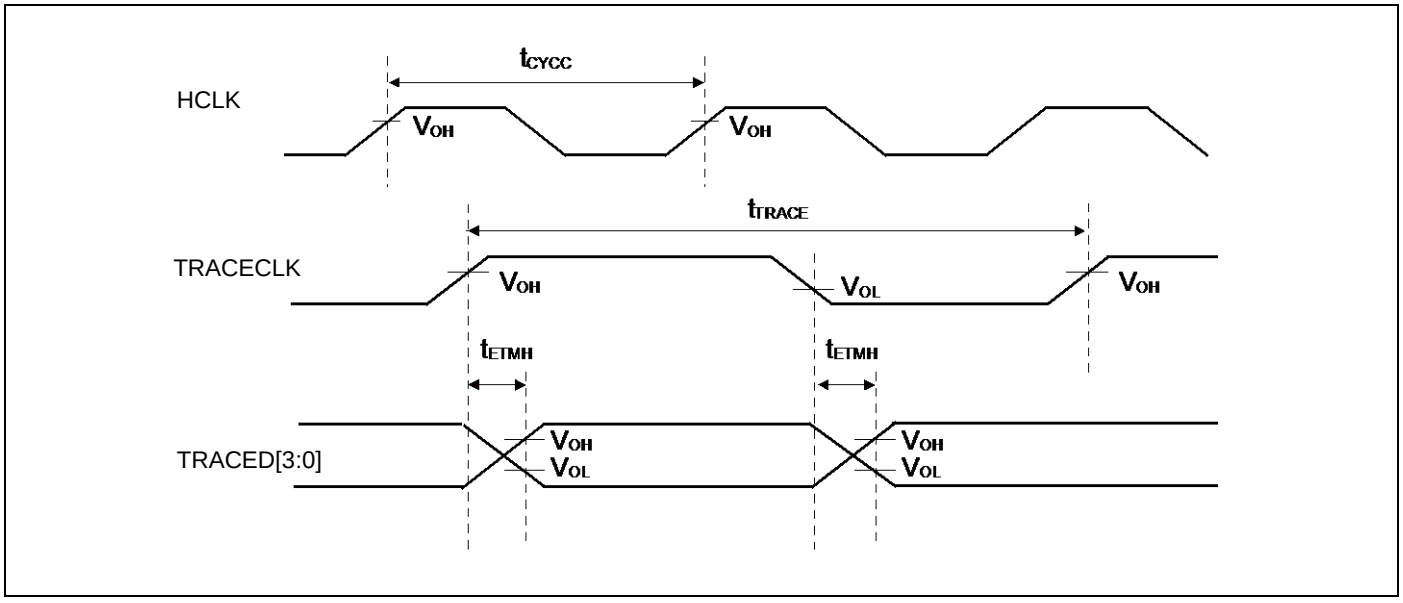
12.4.14 ETM timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK TRACED[3:0]	V_{CC}≥ 4.5 V	2	9	ns	
			V_{CC}< 4.5 V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	V_{CC}≥ 4.5 V	-	40	MHz	
			V_{CC} < 4.5 V	-	32	MHz	
TRACECLK Clock cycle time	t_{TRACE}		V_{CC}≥ 4.5 V	25	-	ns	
			V_{CC} < 4.5 V	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*



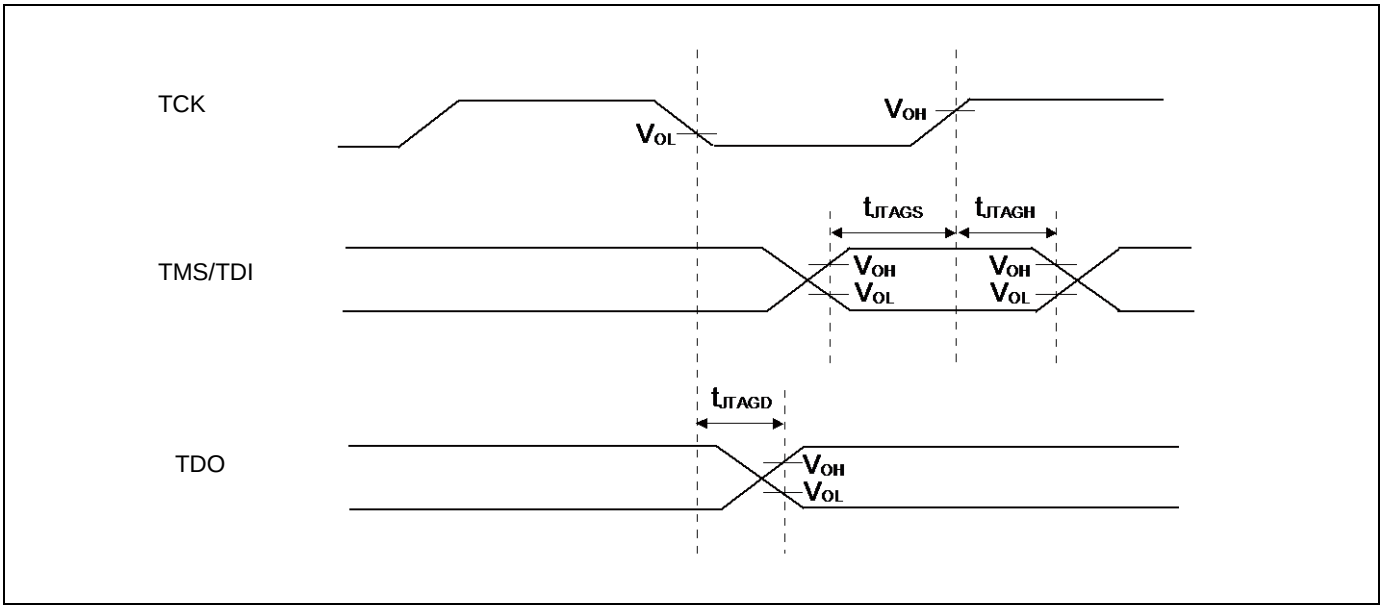
12.4.15 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK TMS,TDI	V_{CC}≥ 4.5 V	15	-	ns	
			V_{CC} < 4.5 V				
TMS, TDI hold time	t_{JTAGH}	TCK TMS,TDI	V_{CC}≥ 4.5 V	15	-	ns	
			V_{CC} < 4.5 V				
TDO delay time	t_{JTAGD}	TCK TDO	V_{CC}≥ 4.5 V	-	25	ns	
			V_{CC} < 4.5 V	-	45		

Note:

- *When the external load capacitance C_L = 30 pF.*



12.5 12-bit A/D Converter

Electrical characteristics for the A/D converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 1.7	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 1.7	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 8	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH±8	AVRH±15	mV	
Conversion time	-	-	1.0*1	-	-	µs	AV_{CC} ≥ 4.5 V
			1.2*1				AV_{CC} < 4.5 V
Sampling time	Ts	-	*2	-	-	ns	AV_{CC} ≥ 4.5 V
			*2	-	-		AV_{CC} < 4.5 V
Compare clock cycle*3	Tcck	-	50	-	2000	ns	
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	12.9	pF	
Analog input resistor	R_{AIN}	-	-	-	2	kΩ	AV_{CC} ≥ 4.5 V
					3.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AVSS	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AVCC	V	

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 4.5 V, HCLK=40 MHz sampling time: 300 ns, compare time: 700 ns

AV_{CC}< 4.5 V, HCLK=40 MHz sampling time: 500 ns, compare time: 700 ns

Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).

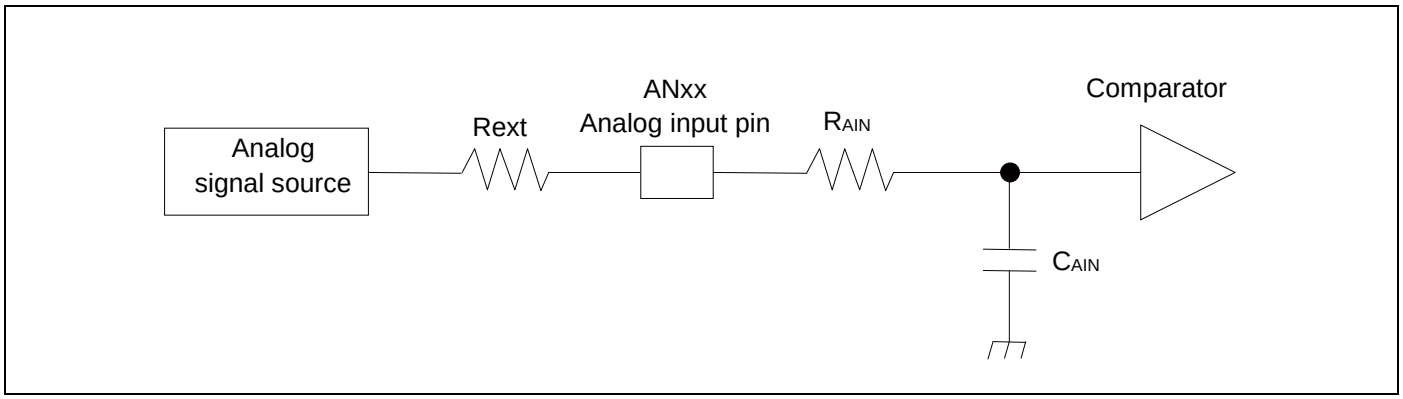
For setting of the sampling time and compare clock cycle, see "Chapter 1-1: A/D Converter" in "FM3 Family Peripheral Manual Analog Macro Part".

The A/D Converter register is set at APB bus clock timing. The sampling clock and compare clock are set at Base clock (HCLK). About the APB bus number which the A/D Converter is connected to, see "8. Block Diagram" in this datasheet.

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1)

*3: The compare time (Tc) is the value of (Equation 2)



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

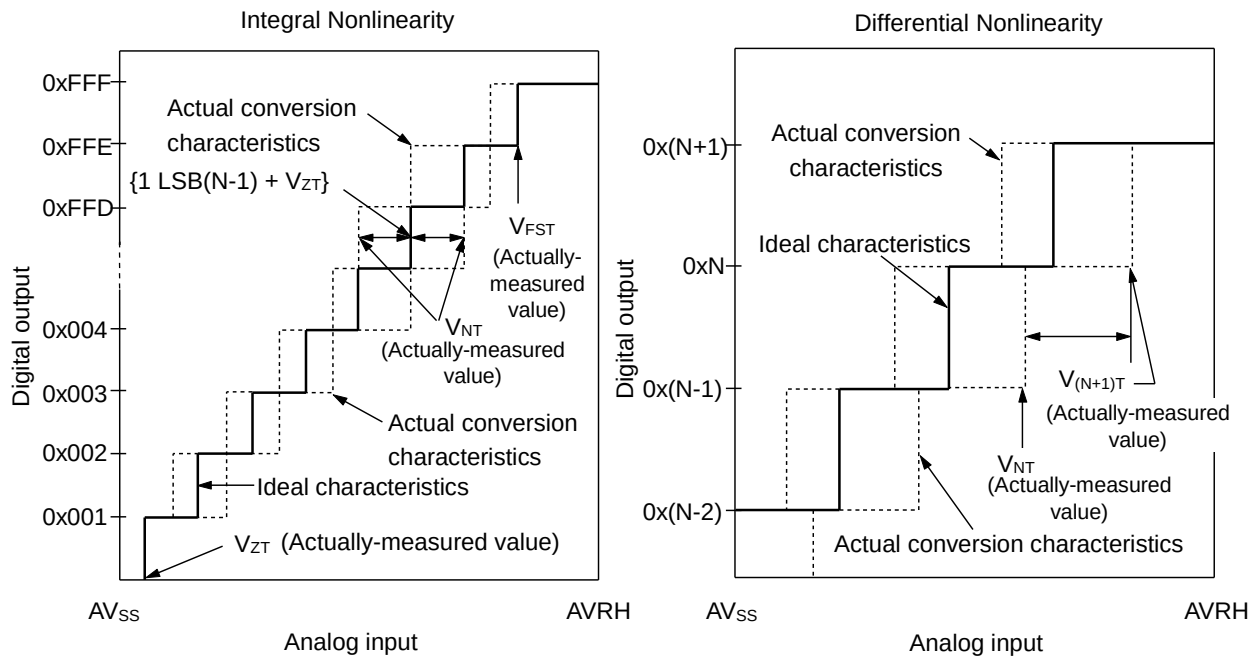
Ts:	Sampling time	
R_{AIN}:	Input resistor of A/D = 2 kΩ	4.5 V ≤ AV_{CC} ≤ 5.5 V
	Input resistor of A/D = 3.8 kΩ	2.7 V ≤ AV_{CC} < 4.5 V
C_{AIN}:	Input capacity of A/D = 12.9 pF	2.7 V ≤ AV_{CC} ≤ 5.5 V
Rext:	Output impedance of external circuit	

(Equation 2) $Tc = Tcck \times 14$

Tc:	Compare time
Tcck:	Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000⟷0b000000000001) and the full-scale transition point (0b111111111110⟷0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 Low-voltage detection characteristics

Low-voltage detection reset

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

Interrupt of low-voltage detection

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	2240 × t_{CYCP} *	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.7 Flash Memory Write/Erase Characteristics

12.7.1 Write / Erase time

(Vcc = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	0.3	1.1		
Half word (16-bit) write time		12	384	µs	Not including system-level overhead time
Chip erase time	64K/128K/256KByte	5.2	23.6	s	Includes write time prior to internal erase
	384K/512KByte	8	38.4	s	

*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

12.7.2 Erase/Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	
100,000	5*	

*: At average + 85°C

12.8 Return Time from Low-Power Consumption Mode

12.8.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

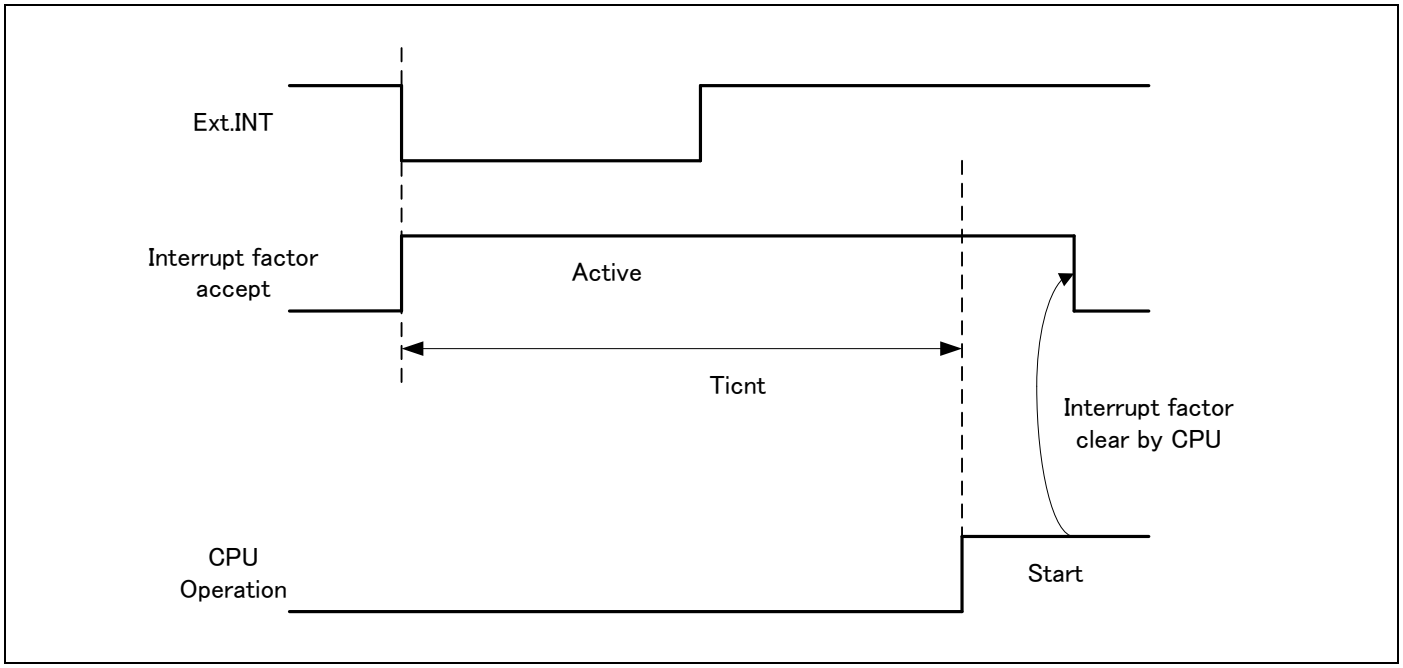
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Ticnt	t_{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		40	80	µs	
Low-speed CR TIMER mode		453	737	µs	
Sub TIMER mode		453	737	µs	
STOP mode		453	737	µs	

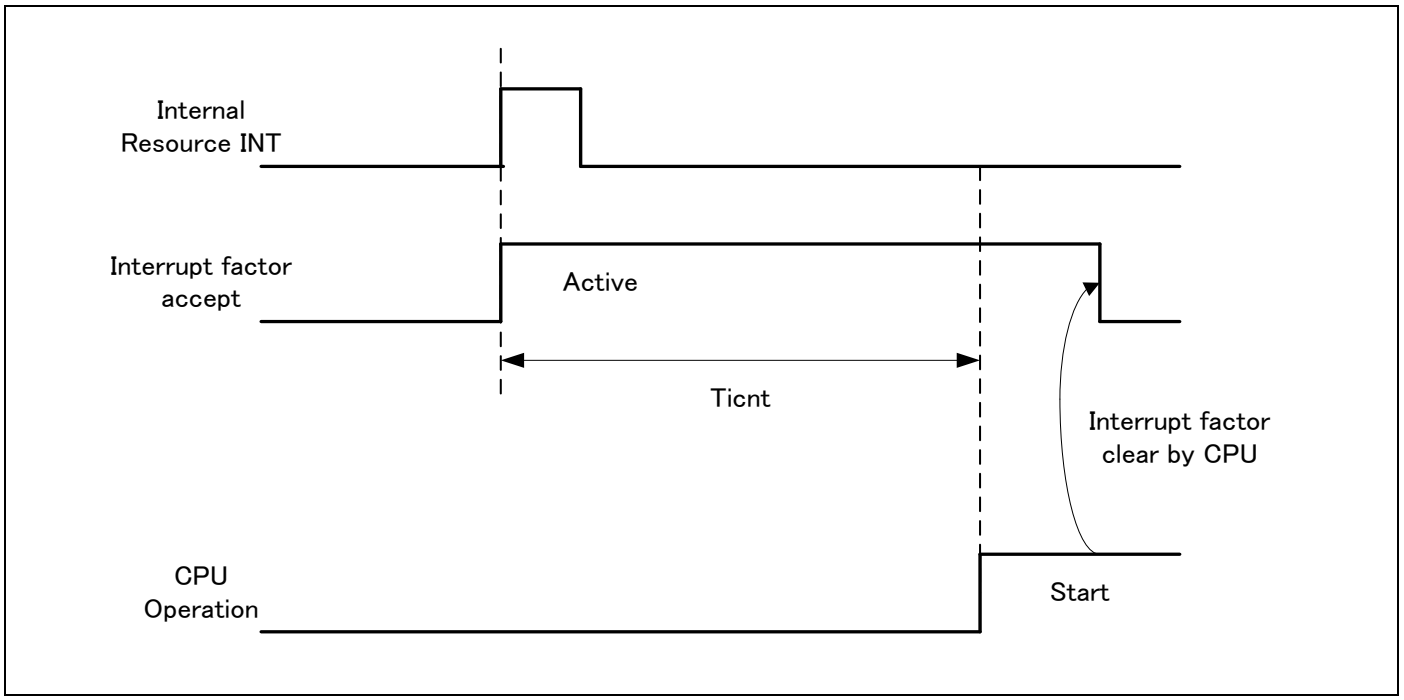
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual about the return factor from Low-Power consumption mode.
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".*

12.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

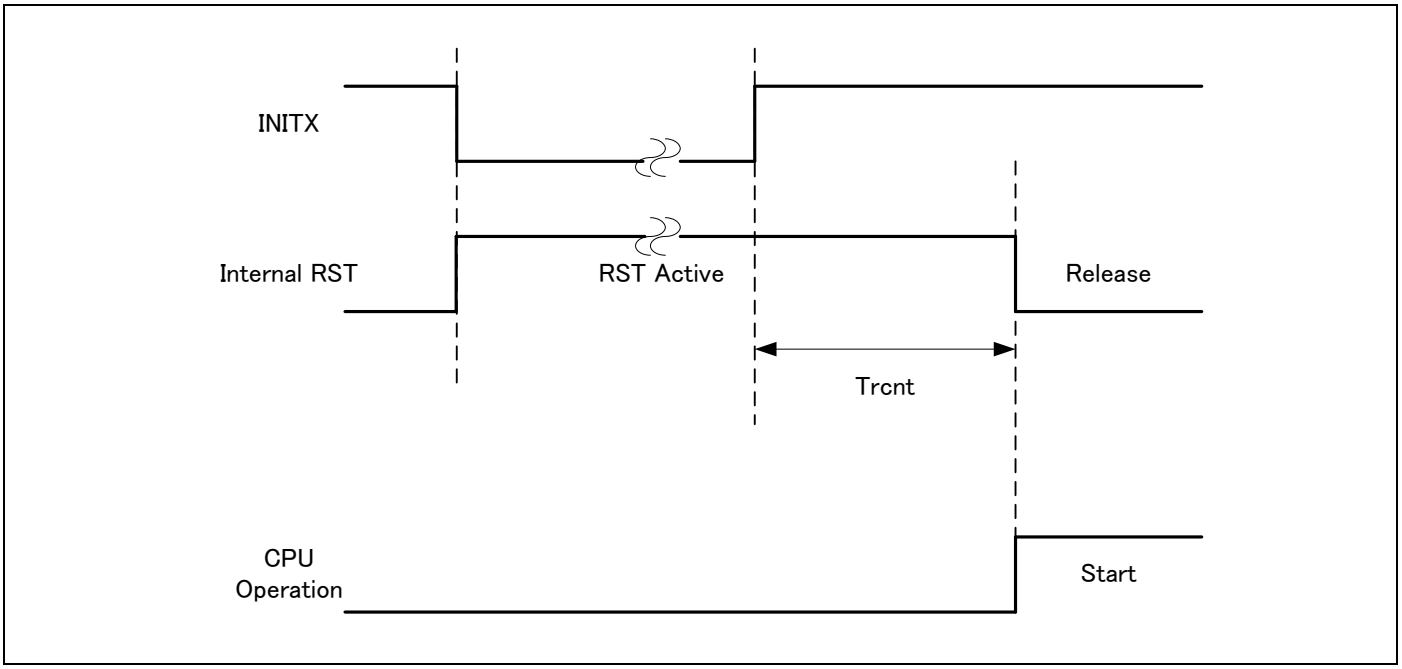
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

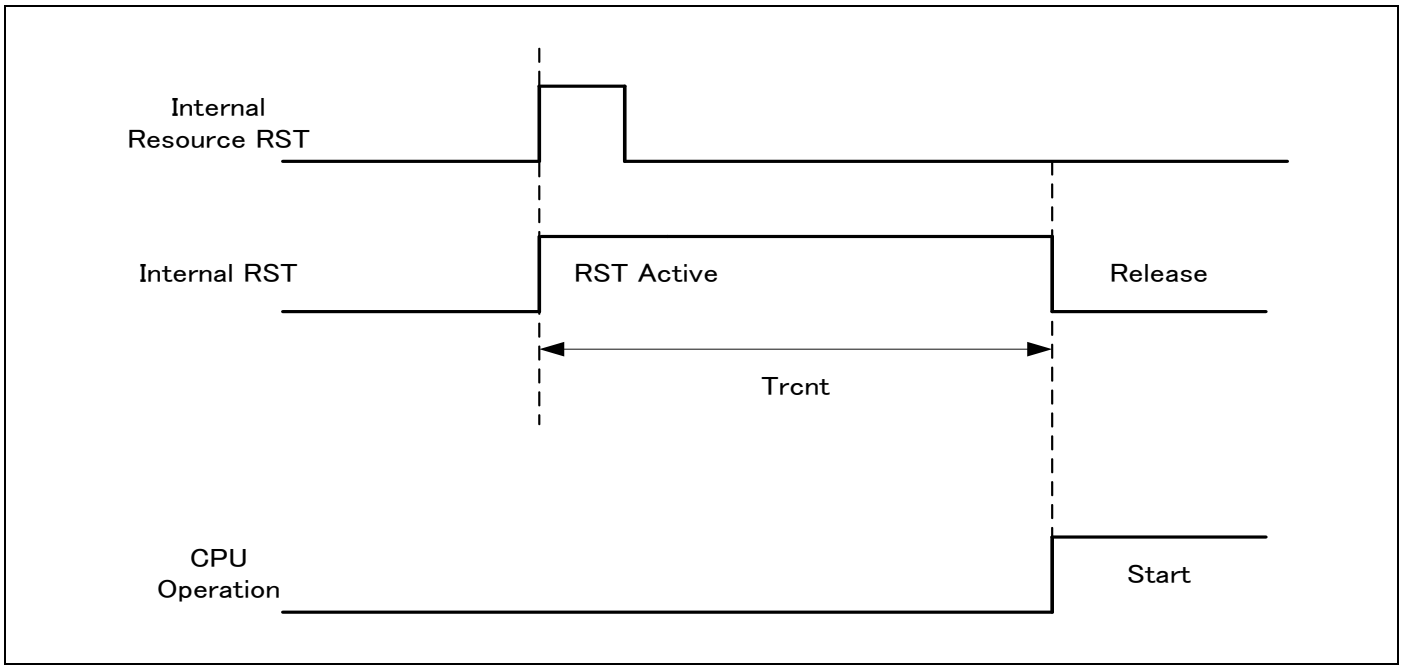
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Trcnt	308	444	µs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		308	444	µs	
Low-speed CR TIMER mode		428	684	µs	
Sub TIMER mode		428	684	µs	
STOP mode		428	684	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

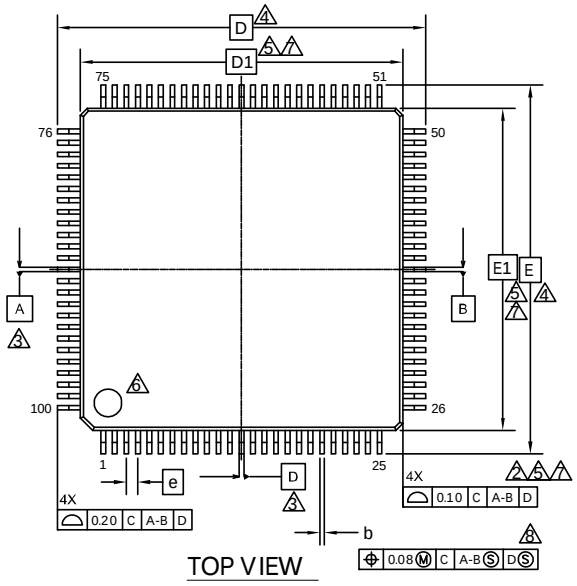
- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "12.4.7. Power-on Reset Timing in 12.4. AC Characteristics in 12. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

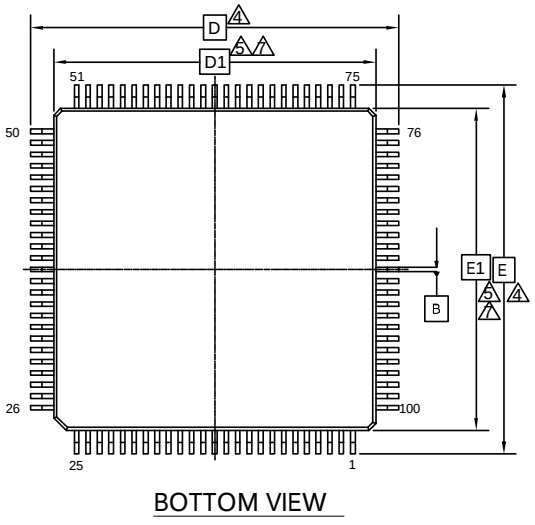
13. Ordering Information

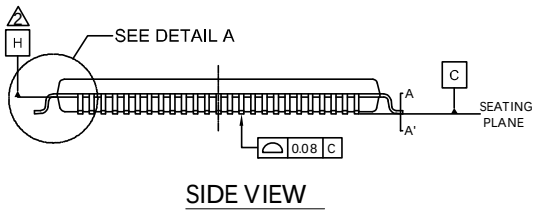
Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9AF111LAPMC1-G-JNE2	64 Kbyte	16 Kbyte	Plastic • LQFP (0.5 mm pitch), 64-pin (LQD064)	Tray
MB9AF112LAPMC1-G-JNE2	128 Kbyte	16 Kbyte		
MB9AF114LAPMC1-G-JNE2	256 Kbyte	32 Kbyte		
MB9AF111LAPMC-G-JNE2	64 Kbyte	16 Kbyte	Plastic • LQFP (0.65 mm pitch), 64-pin (LQG064)	
MB9AF112LAPMC-G-JNE2	128 Kbyte	16 Kbyte		
MB9AF114LAPMC-G-JNE2	256 Kbyte	32 Kbyte		
MB9AF112LPMC-G-MJE1	128 Kbyte	16 Kbyte		
MB9AF114LPMC-G-MJE1	256 Kbyte	32 Kbyte		
MB9AF111LAQN-G-AVE2	64 Kbyte	16 Kbyte	Plastic • QFN (0.5 mm pitch), 64-pin (VNC064)	
MB9AF112LAQN-G-AVE2	128 Kbyte	16 Kbyte		
MB9AF114LAQN-G-AVE2	256 Kbyte	32 Kbyte		
MB9AF111MAPMC-G-JNE2	64 Kbyte	16 Kbyte	Plastic • LQFP (0.5 mm pitch), 80-pin (LQH080)	
MB9AF112MAPMC-G-JNE2	128 Kbyte	16 Kbyte		
MB9AF114MAPMC-G-JNE2	256 Kbyte	32 Kbyte		
MB9AF115MAPMC-G-JNE2	384 Kbyte	32 Kbyte		
MB9AF116MAPMC-G-JNE2	512 Kbyte	32 Kbyte		
MB9AF111NAPMC-G-JNE2	64 Kbyte	16 Kbyte	Plastic • LQFP (0.5 mm pitch), 100-pin (LQI100)	
MB9AF112NAPMC-G-JNE2	128 Kbyte	16 Kbyte		
MB9AF114NAPMC-G-JNE2	256 Kbyte	32 Kbyte		
MB9AF115NAPMC-G-JNE2	384 Kbyte	32 Kbyte		
MB9AF116NAPMC-G-JNE2	512 Kbyte	32 Kbyte		
MB9AF111NAPF-G-JNE1	64 Kbyte	16 Kbyte	Plastic • QFP (0.65 mm pitch), 100-pin (PQH100)	
MB9AF112NAPF-G-JNE1	128 Kbyte	16 Kbyte		
MB9AF114NAPF-G-JNE1	256 Kbyte	32 Kbyte		
MB9AF115NAPF-G-JNE1	384 Kbyte	32 Kbyte		
MB9AF116NAPF-G-JNE1	512 Kbyte	32 Kbyte		
MB9AF111NABGL-GE1	64 Kbyte	16 Kbyte	Plastic • PFBGA (0.8 mm pitch), 112-pin (LBC112)	
MB9AF112NABGL-GE1	128 Kbyte	16 Kbyte		
MB9AF114NABGL-GE1	256 Kbyte	32 Kbyte		

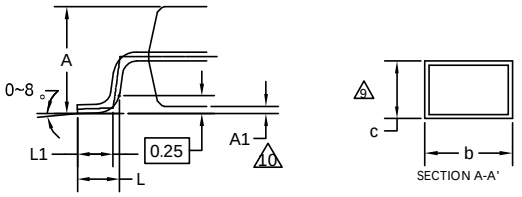
14. Package Dimensions

Package Type	Package Code
LQFP 100	LQI100









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

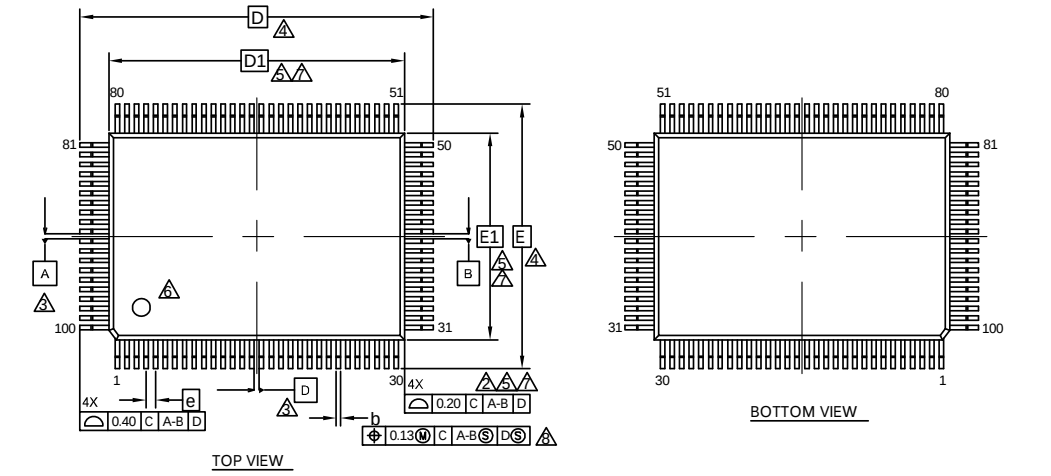
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

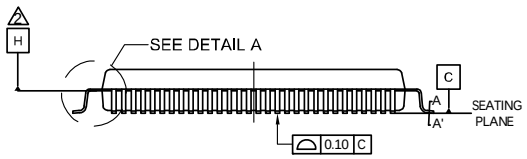
002-11500 *A

Package Type	Package Code
QFP 100	PQH100

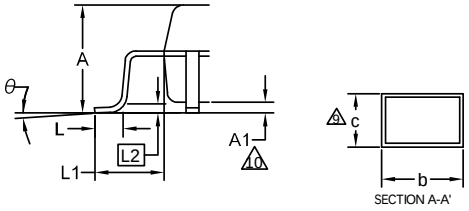


TOP VIEW

BOTTOM VIEW



SIDE VIEW



DETAIL A

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.35
A1	0.05	—	0.45
b	0.27	0.32	0.37
c	0.11	—	0.23
D	23.90 BSC		
D1	20.00 BSC		
e	0.65 BSC		
E	17.90 BSC		
E1	14.00 BSC		
θ	0°	—	8°
L	0.73	0.88	1.03
L1	1.95 REF		
L2	0.25 BSC		

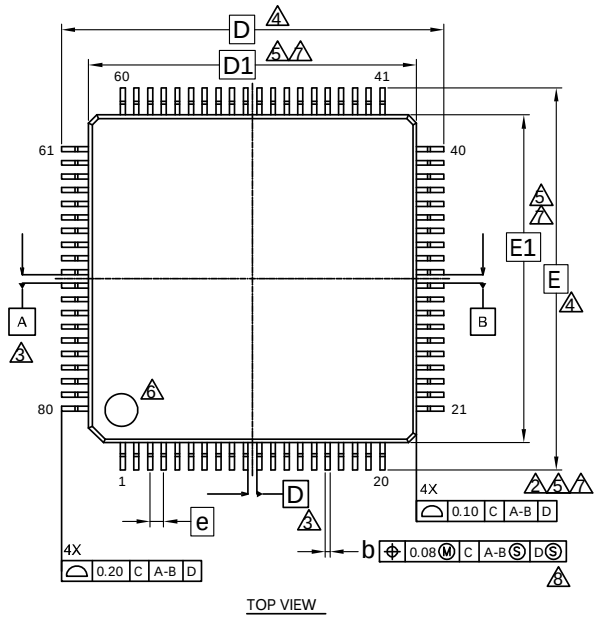
NOTES

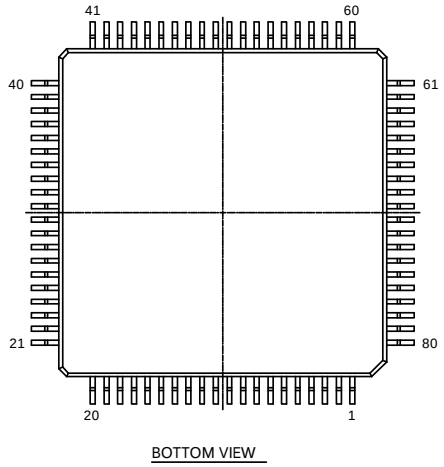
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

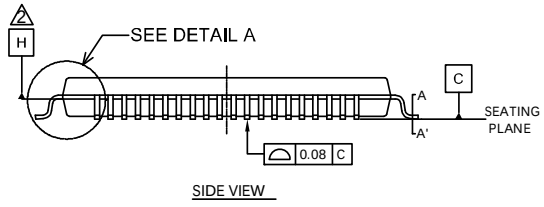
002-15156 **

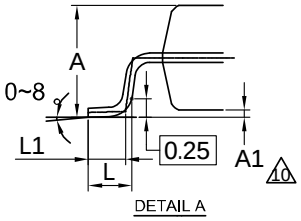
PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

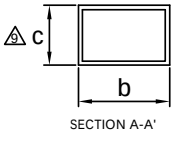
Package Type	Package Code
LQFP 80	LQH080











SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

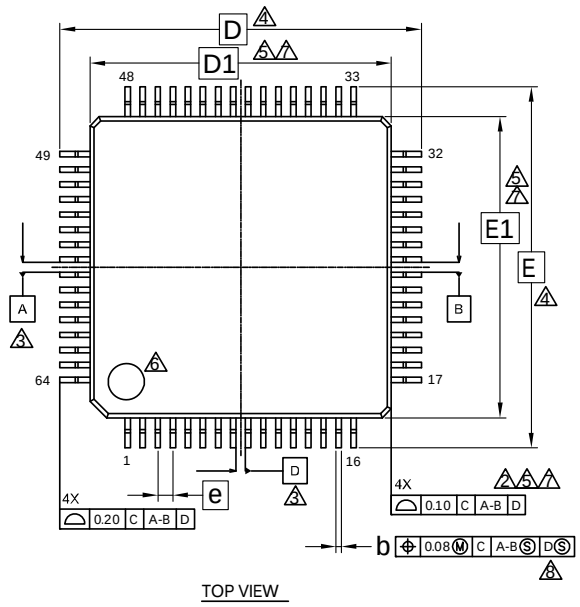
NOTES

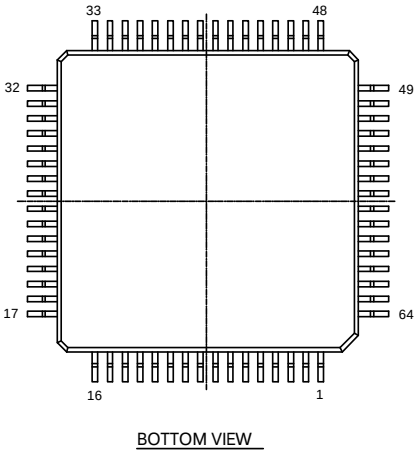
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

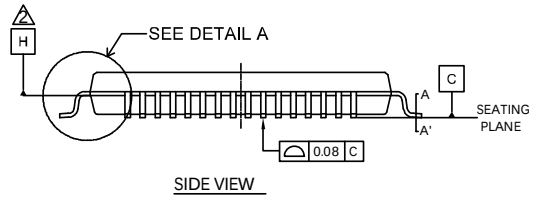
002-11501 **

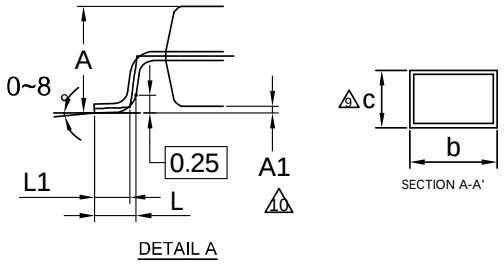
PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **

Package Type	Package Code
LQFP 64	LQD064









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

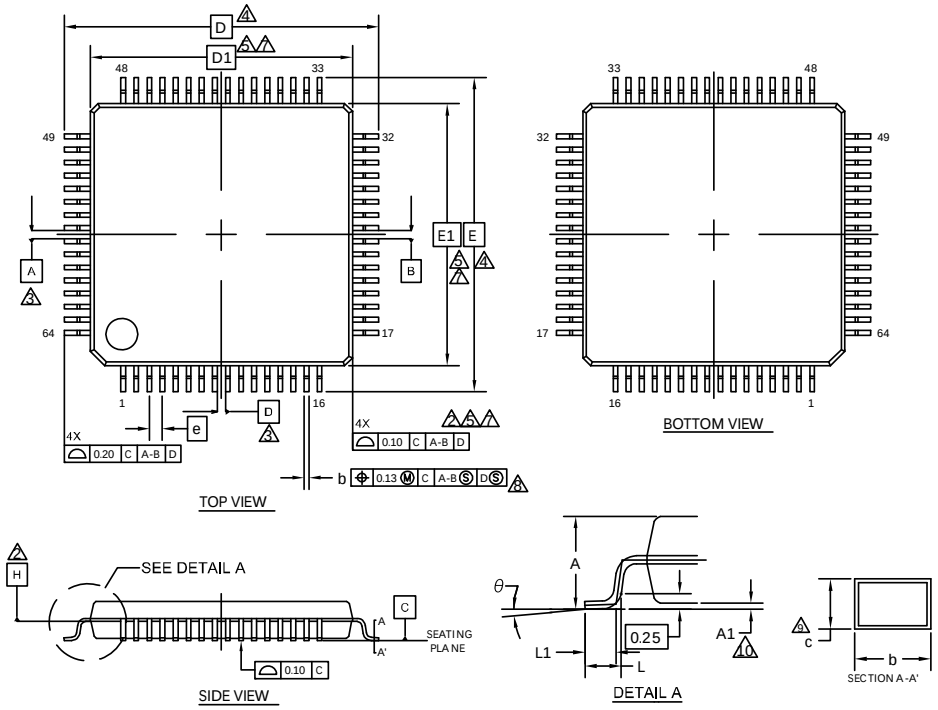
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

Package Type	Package Code
LQFP 64	LQG064



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.27	0.32	0.37
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

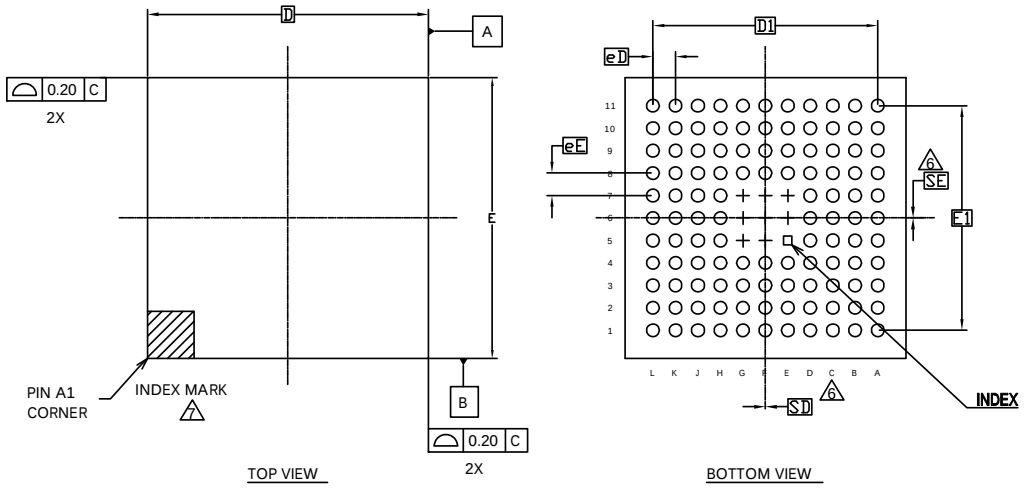
NOTES

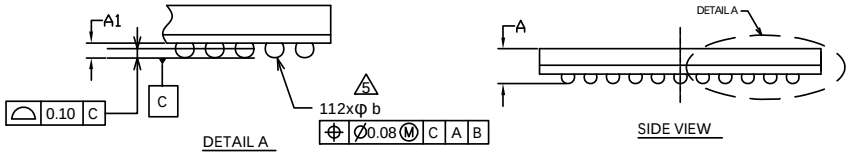
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

Package Type	Package Code
PFBGA 112	LBC112





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.45
A1	0.25	0.35	0.45
D		10.00 BSC	
E		10.00 BSC	
D1		8.00 BSC	
E1		8.00 BSC	
MD		11	
ME		11	
N		112	
Ø b	0.35	0.45	0.55
eD		0.80 BSC	
eE		0.80 BSC	
SD		0.00	
SE		0.00	

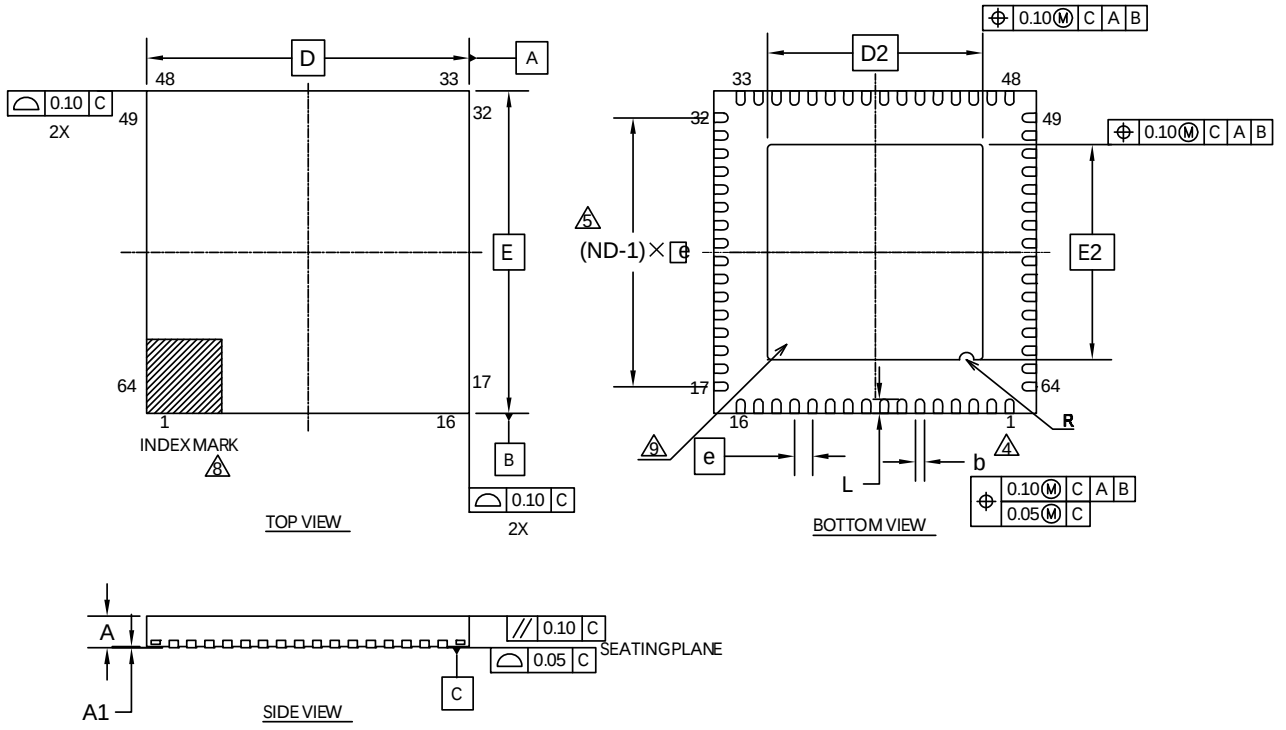
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-13225 **

PACKAGE OUTLINE, 112 BALL FBGA
10.00X10.00X1.45 MM LBC112 REV**

Package Type	Package Code
QFN 64	VNC064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.90
A1	0.00	—	0.05
D	9.00 BSC		
E	9.00 BSC		
b	0.20	0.25	0.30
D2	6.00 BSC		
E2	6.00 BSC		
e	0.50 BSC		
R	0.20 REF		
L	0.35	0.40	0.45
N	64		
ND	16		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

002-13234 **

PACKAGE OUTLINE, 64 LEAD QFN
9.0X9.0X0.9 MM VNC064 6.0X6.0 MM EPAD (SAWN) Rev*.*

15. Errata

This chapter describes the errata for MB9A110 product family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

15.1 Part Numbers Affected

Part Number
Initial Revision
MB9AF111LPMC1-G-JNE2, MB9AF112LPMC1-G-JNE2, MB9AF114LPMC1-G-JNE2, MB9AF111LPMC-G-JNE2, MB9AF112LPMC-G-JNE2, MB9AF114LPMC-G-JNE2, MB9AF112LPMC-G-MJE1, MB9AF114LAPMC-G-JNE2, MB9AF111LQN-G-AVE2, MB9AF112LQN-G-AVE2, MB9AF114LQN-G-AVE2, MB9AF111MPMC-G-JNE2, MB9AF112MPMC-G-JNE2, MB9AF114MPMC-G-JNE2, MB9AF115MPMC-G-JNE2, MB9AF116MPMC-G-JNE2, MB9AF111NPMC-G-JNE2, MB9AF112NPMC-G-JNE2, MB9AF114NPMC-G-JNE2, MB9AF115NPMC-G-JNE2, MB9AF116NPMC-G-JNE2, MB9AF111NPF-G-JNE1, MB9AF112NPF-G-JNE1, MB9AF114NPF-G-JNE1, MB9AF115NPF-G-JNE1, MB9AF116NPF-G-JNE1, MB9AF111NBGL-GE1, MB9AF112NBGL-GE1, MB9AF114NBGL-GE1

15.2 Qualification Status

Product Status: In Production − Qual.

15.3 Errata Summary

This table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
Watch Counter issue	Refer to 15.1	Rev. initial rev.	Fixed in Rev. A

Watch Counter issue

■PROBLEM DEFINITION
The underflow interruption does not occur.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
The condition is when underflow interruption occurs.

■SCOPE OF IMPACT
The underflow interruption does not occur as specified.

■WORKAROUND
This error cannot be avoided by any software, except not using Watch Counter interrupt.

■FIX STATUS
This issue was fixed in Rev. A.

16. Major Changes

Spansion Publication Number: DS706-00011

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
-	-	Revised series name and part number: MB9A110 Series→MB9A110A Series MB9AF111L → MB9AF111LA MB9AF112L → MB9AF112LA MB9AF114L → MB9AF114LA MB9AF111M → MB9AF111MA MB9AF112M → MB9AF112MA MB9AF114M → MB9AF114MA MB9AF115M → MB9AF115MA MB9AF116M → MB9AF116MA MB9AF111N → MB9AF111NA MB9AF112N → MB9AF112NA MB9AF114N → MB9AF114NA MB9AF115N → MB9AF115NA MB9AF116N → MB9AF116NA Added the package. LCC-64P-M24
8	PRODUCT LINEUP Function Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)	Added the following description. ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO
	External Interrupts	Corrected the following description. 7pins (Max) → 8pins (Max)
34 to 37	SIGNAL DESCRIPTION Multi-function Serial (ch.0 to ch.7)	Corrected the description for function. Added "LIN pin" Deleted "UART pin"
42, 43	I/O CIRCUIT TYPE	Corrected the following schematic for "TypeB". CMOS level hysteresis input → Digital input Corrected the following schematic for "TypeC". Control Pin → Digital output
51	HANDLING DEVICES Power supply pins	Corrected the description.
54	MEMORY SIZE	Added "MEMORY SIZE".
69	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Main Clock Input Characteristics	Added the items F_{CM} to the Internal operating clock frequency.
71	(4-2) Operating Conditions of Main PLL	Added the description.
72	(7) External Bus Timing External bus clock output Characteristics	
79	(8) Base Timer Input Timing Trigger input timing	Added the Note.
88	(10) External input timing	Corrected the footnote.
94	12-bit A/D Converter Electrical characteristics for the A/D converter	Corrected the value of "Full-scale transition voltage". Min: -20 → AVRH-20 Max: +20 → AVRH+20 Corrected the value of "Compare clock cycle". Max: 10000 → 2000 Corrected the value of "Reference voltage". Min: AVSS → 2.7
Revision 2.1		
-	-	Company name and layout design change
Revision 3.0		
3	FEATURES External Bus Interface	Added the description of Maximum area size

Page	Section	Change Results
9	PACKAGES	Deleted FPT-64P-M24, FPT-64P-M23, FPT-80P-M21, FPT-100P-M20
44, 46	I/O CIRCUIT TYPE	Added the description of I^2C to the type of E, F and I
44, 45	I/O CIRCUIT TYPE	Added about +B input
51	HANDLING DEVICES	Added "Stabilizing power supply voltage"
51	HANDLING DEVICES Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
52	HANDLING DEVICES C Pin	Changed the description
53	BLOCK DIAGRAM	Modified the block diagram
54	MEMORY SIZE	Changed to the following description See "Memory size" in "PRODUCT LINEUP" to confirm the memory size.
55	MEMORY MAP Memory map(1)	Modified the area of "External Device Area"
56, 57	MEMORY MAP Memory map(2)(3)	Added the summary of Flash memory sector and the note
64, 65	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Added the Clamp maximum current Added the output current of P80 and P81 Added about +B input
66	ELECTRICAL CHARACTERISTICS 2. Recommended Operation Conditions	Modified the minimum value of Analog reference voltage Added Smoothing capacitor Added the note about less than the minimum power supply voltage
67, 68	ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current rating	Changed the table format Added Main TIMER mode current Added Flash Memory Current Moved A/D Converter Current
71	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Added Frequency stability time at Built-in high-speed CR
72	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4-1)(4-2) Operating Conditions of Main PLL	Added Main PLL clock frequency Added the figure of Main PLL connection
73	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (6) Power-on Reset Timing	Added Time until releasing Power-on reset Changed the figure of timing
75-77	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (7) External Bus Timing	Modified Data output time
82-89	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (8) CSIO/UART Timing	Modified from UART Timing to CSIO/UART Timing Changed from Internal shift clock operation to Master mode Changed from External shift clock operation to Slave mode
96	ELECTRICAL CHARACTERISTICS 5. 12bit A/D Converter	Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage Modified Stage transition time to operation permission Modified the minimum value of Reference voltage
101	ELECTRICAL CHARACTERISTICS 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
105	ORDERING INFORMATION	Change to full part number
106	PACKAGE DIMENSIONS	Deleted FPT-64P-M24, FPT-64P-M23, FPT-80P-M21, FPT-100P-M20

Note: Please see “Document History” about later revised information.

Document History

Document Title: MB9A110A/MB9A110 Series 32-bit ARM® Cortex®-M3 FM3 Microcontroller
Document Number: 002-04672

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	AKIH	12/16/2014	Migrated to Cypress and assigned document number 002-04672. No change to document contents or format.
*A	5198491	AKIH	04/07/2016	Updated to Cypress format.
*B	5316949	MMIW	06/21/2016	Added series “MB9A110”. (Page1) Changed package code as the following in 2 Packages (Page 7), 3 Pin Assignment (Page 8 to 12), 12.2 Recommended Operating Conditions (Page 60), 13 Ordering Information (Page 99) and 14 Package Dimensions (Page 100 to 106). “FTP-64P-M38” to LQD064, “FTP-64P-M39” to LQG064, “LCC-64P-M24” to “VNC064”, FPT-80P-M37” to “LQH080”, “FPT-100P-M23” to “LQI100”, “FTP-100P-M06” to “PQH100”, “BGA-112P-M04” to “LBC112” Changed “J-TAG” to” JTAG” in 4 List of Pin Functions (Page 27). Added note 4 List of Pin Functions (Page 38). Changed “Ta” to “T_A” in 12.2 Recommended Operating Conditions (Page 60). Added Product number “MB9AF112L” and “MB9AF114L” in Features (Page1), in 1 Product Lineup (Page6), 2 Packages (Page7) and 10 Memory Map (Page51 to 52). Added Part number “MB9AF112LPMC-G-MJE1” and “MB9AF114LPMC-G-MJE1” in 13 Ordering Information (Page 99).
*C	5490454	YSKA	03/09/2017	Updated “12.4.7 Power-on Reset Timing”(page 67) Updated “14. Package Dimensions”(page 100-106) Added “15. Errata”(page 107) Corrected the following statement Analog port input current → Analog port input leak current in chapter 12.5. 12-bit A/D Converter (Page 90) Added the Baud rate spec in “12.4.10 CSIO/UART Timing”(Page 76, 78, 80, 82)
*D	5768637	YSAT	06/12/2017	Adapted new cypress logo

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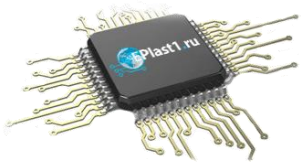

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