

# 74AHC273; 74AHCT273

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 03 — 13 May 2008

Product data sheet

## 1. General description

The 74AHC273; 74AHCT273 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC273; 74AHCT273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs.

The common clock (CP) and master reset ( $\overline{MR}$ ) inputs, load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW, independent of clock or data inputs, by a LOW on the  $\overline{MR}$  input.

The device is useful for applications where only the true output is required and the clock and master reset are common to all storage elements.

## 2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than  $V_{CC}$
- Ideal buffer for MOS microcontroller or memory
- Common clock and master reset
- Related product versions:
  - ◆ 74AHC377; 74AHCT377 for clock enable version
  - ◆ 74AHC373; 74AHCT373 for transparent latch version
  - ◆ 74AHC374; 74AHCT374 for 3-state version
- Input levels:
  - ◆ For 74AHC273: CMOS level
  - ◆ For 74AHCT273: TTL level
- ESD protection:
  - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
  - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<b>74AHC273</b>				
74AHC273D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC273PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHC273BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
<b>74AHCT273</b>				
74AHCT273D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT273PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHCT273BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

### 4. Functional diagram



Fig 1. Logic symbol



Fig 2. IEC logic symbol



Fig 3. Logic diagram

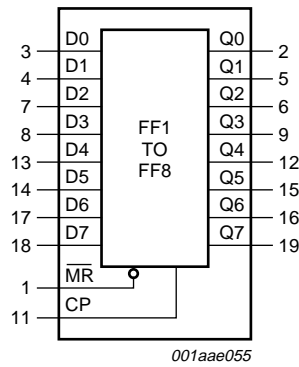


Fig 4. Functional diagram

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{\text{MR}}$	1	master reset input (active LOW)
Q0	2	flip-flop output
D0	3	data input
D1	4	data input
Q1	5	flip-flop output
Q2	6	flip-flop output
D2	7	data input
D3	8	data input
Q3	9	flip-flop output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH edge-triggered)
Q4	12	flip-flop output
D4	13	data input
D5	14	data input
Q5	15	flip-flop output
Q6	16	flip-flop output

Table 2. Pin description ...continued

Symbol	Pin	Description
D6	17	data input
D7	18	data input
Q7	19	flip-flop output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Control		Input	Output
	MR	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 ↑ = LOW-to-HIGH;  
 X = don't care.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	<sup>[1]</sup> -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	<sup>[1]</sup> -20	+20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-25	+25	mA
I <sub>CC</sub>	supply current		-	+75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	<sup>[2]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] For SO20 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 8 mW/K.  
 For TSSOP20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K.  
 For DHVQFN20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC273</b>						
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V
<b>74AHCT273</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC273</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0\text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5\text{ V}$	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0\text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5\text{ V}$	-	-	1.65	-	1.65	-	1.65	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -50\ \mu\text{A}$ ; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50\ \mu\text{A}$ ; $V_{CC} = 3.0\text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50\ \mu\text{A}$ ; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	2.58	-	-	2.48	-	2.40	-	V
	$I_O = -8.0\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	3.94	-	-	3.80	-	3.70	-	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 50\ \mu\text{A}$ ; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}$ ; $V_{CC} = 3.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}$ ; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	-	-	0.36	-	0.44	-	0.55	V
	$I_O = 8.0\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	-	-	0.36	-	0.44	-	0.55	V	

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$C_I$	input capacitance		-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF
<b>74AHCT273</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	-	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance		-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74AHC273</b>										
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	6.0	13.6	1.0	16.0	1.0	17.0	ns
		$C_L = 50\text{ pF}$	-	8.6	17.1	1.0	19.5	1.0	21.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.2	9	1.0	10.5	1.0	11.5	ns
		$C_L = 50\text{ pF}$	-	6.0	11.0	1.0	12.5	1.0	14.0	ns
		MR to Qn; see <a href="#">Figure 8</a> <sup>[3]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.1	13.6	1.0	16.0	1.0	17.0	ns
		$C_L = 50\text{ pF}$	-	7.3	17.1	1.0	19.5	1.0	21.5	ns
		$f_{max}$	maximum frequency	see <a href="#">Figure 7</a>						
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$										
$C_L = 15\text{ pF}$	75			120	-	65	-	65	-	MHz
$C_L = 50\text{ pF}$	50			75	-	45	-	45	-	MHz
$V_{CC} = 4.5\text{ V to }5.5\text{ V}$										
$C_L = 15\text{ pF}$	120			165	-	100	-	100	-	MHz
$t_W$	pulse width	CP HIGH or LOW; see <a href="#">Figure 7</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5.0	-	-	6.5	-	6.5	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5.0	-	-	6.0	-	6.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 9</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.0	-	-	3.0	-	3.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	3.0	-	-	3.0	-	3.0	-	ns
$t_h$	hold time	Dn to CP; see <a href="#">Figure 9</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	-	-	1.0	-	1.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	-	-	1.0	-	1.0	-	ns



**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
t <sub>rec</sub>	recovery time	MR to CP; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.5	-	-	2.5	-	2.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	14	-	-	-	-	-	pF
<b>74AHCT273; V<sub>CC</sub> = 4.5 V to 5.5 V</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		C <sub>L</sub> = 15 pF	-	4.0	7.5	1.0	8.8	1.0	9.5	ns
		C <sub>L</sub> = 50 pF	-	5.8	9.2	1.0	10.5	1.0	11.5	ns
		MR to Qn; see <a href="#">Figure 8</a> <sup>[3]</sup>								
		C <sub>L</sub> = 15 pF	-	3.9	10.0	1.0	11.6	1.0	12.5	ns
		C <sub>L</sub> = 50 pF	-	5.6	11.0	1.0	12.6	1.0	14.0	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 7</a>								
		C <sub>L</sub> = 15 pF	75	120	-	65	-	65	-	MHz
		C <sub>L</sub> = 50 pF	50	75	-	45	-	45	-	MHz
t <sub>W</sub>	pulse width	CP HIGH or LOW; see <a href="#">Figure 7</a>	5.0	-	-	6.5	-	6.5	-	ns
		MR LOW; see <a href="#">Figure 8</a>	5.0	-	-	6.0	-	6.0	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see <a href="#">Figure 9</a>	3.0	-	-	3.0	-	3.0	-	ns
t <sub>h</sub>	hold time	Dn to CP; see <a href="#">Figure 9</a>	1.0	-	-	1.0	-	1.0	-	ns
t <sub>rec</sub>	recovery time	MR to CP; see <a href="#">Figure 8</a>	2.5	-	-	2.5	-	2.5	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	18	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] t<sub>pd</sub> is the same as t<sub>PHL</sub> only.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

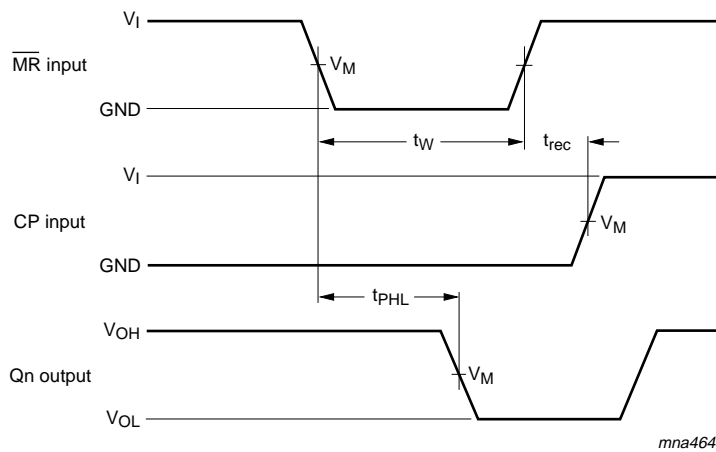
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

11. Waveforms



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Clock pulse width, maximum frequency and input to output propagation delays**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. Master reset pulse width, recovery time and propagation delay**

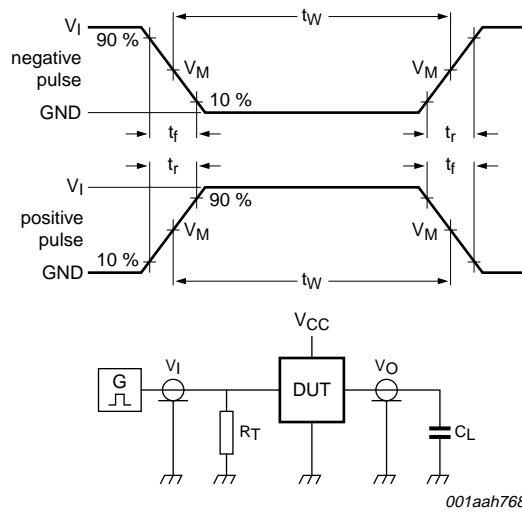


Measurement points are given in [Table 8](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 9. Data set-up and hold times**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC273	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT273	1.5 V	$0.5 \times V_{CC}$



001aah768

Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 10. Load circuitry for measuring switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74AHC273	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74AHCT273	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

## 12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig 13. Package outline SOT764-1 (DHVQFN20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
MOS	Metal-Oxide Semiconductor

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT273_3	20080513	Product data sheet	-	74AHC_AHCT273_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 6</a>: the conditions for input leakage current have been changed.</li> </ul>			
74AHC_AHCT273_2	20030721	Product specification	-	74AHC_AHCT273_1
74AHC_AHCT273_1	19990901	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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