Low VD with Individual SENSE Pin and Delay Function for Automotive Applications

NO.EC-242-140130

OUTLINE

The R3118x is a CMOS-based voltage detector IC with individual sense pin, high detector threshold accuracy and delay time, and ultra-low supply current, which can be operated at an extremely low voltage and is used for system reset as an example.

Each of the IC consists of a voltage reference unit, a hysteresis comparator, resistors net for detector threshold setting, an output driver transistor, and a delay circuit.

V_{DD} supply pin for the IC and voltage supervisory sense pin are individual, therefore the output pin can keep "L" level even if the sense pin voltage is going down to 0V, or there is no indefinite range for the sense pin.

Since a delay circuit is built-in, by connecting an external capacitor, any output delay time can be set. In the R3118x series, detector released delay time can be set, and detector delay time is not influenced by the external capacitor for the delay time.

The detector threshold is fixed with high accuracy internally and does not require any adjustment.

The tolerance of the detector threshold is ±22.5mV ($-V_{DET_S}$<1.6V) or ±1.5% ($-V_{DET_S}$≥1.6V).

Minimum detector threshold voltage is 0.6V, ultra low voltage detector threshold can be set.

Output delay time for the detector release can be set with high accuracy. The tolerance of the IC side is ±30%.

Two output types, Nch open drain type and CMOS type are available. If the sense pin voltage becomes to equal or lower than the detector threshold voltage, the output voltage becomes "L", and if the sense pin voltage becomes to released voltage, the output voltage becomes "H" after the set delay time.

The R3118x supports SOT-23-5 package.

FEATURES*

- Operating Voltage Range (Maximum Rating) ..... 1.0V to 6.0V (7.0V)
- Supply Current ..... Typ. 0.4μA (V_{SENSE}≥+V_{DET}, V_{DD}=6V)
  Consumption current through SENSE pin is not included.
- Detector Threshold Range ..... 0.6V to 5.0V (0.1V steps)
  For other voltages, refer to *MARK INFORMATIONS*.
- Accuracy Detector Threshold ..... ±1.5% ($-V_{DET_S}$≥1.6V), ±22.5mV ($-V_{DET_S}$<1.6V)
- Temperature-Drift Coefficient of Detector Threshold ..... Typ. ±30ppm/°C
- Accuracy Detector Released ..... ±30%
- Temperature-Drift Coefficient of Detector Released ..... Typ. ±0.16ppm/°C
- Output Types ..... Nch Open Drain and CMOS
- Packages SOT-23-5

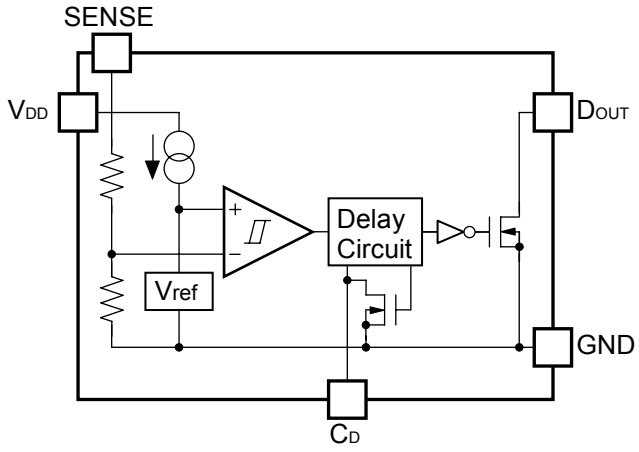
∗ Ta=25°C, unless otherwise noted.

APPLICATIONS

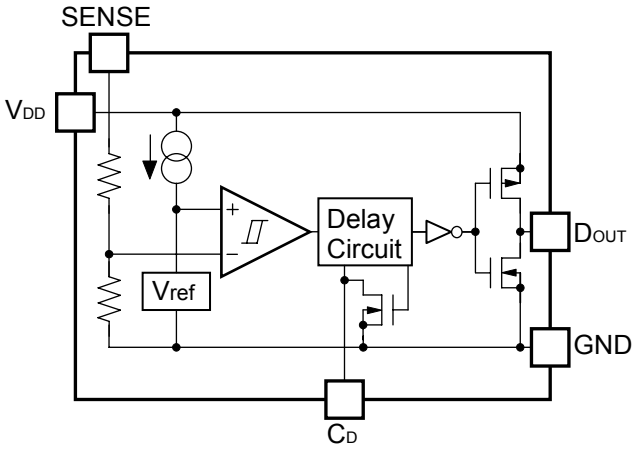
- Power source for car accessories including car audio equipment, car navigation system, and ETC system.

BLOCK DIAGRAMS

Nch Open Drain Output (R3118xxxxA)



CMOS Output (R3118xxxxC)



SELECTION GUIDE

The package type, the detector threshold, the output type and the taping type for the IC can be selected at the users' request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3118Nxx1∗-TR-#E	SOT-23-5	3,000 pcs	Yes	Yes

xx: The detector threshold can be designated in the range from 0.6V(06) to 5.0V(50) in 0.1V steps.
For other voltages, please refer to *MARK INFORMATIONS*.

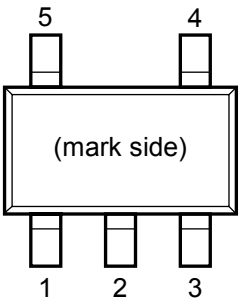
∗ : Designation of Output Type
(A) Nch Open Drain
(C) CMOS

: Specify Automotive Class Code

	Operating Temperature Range	Guaranteed Specs Temperature Range	Screening
A	−40°C to 85°C	25°C	High temperature

PIN DESCRIPTIONS

- **SOT-23-5**



- **SOT-23-5**

Pin No.	Symbol	Description
1	D_{OUT}	Output Pin ("L" at detection)
2	V_{DD}	Input Pin
3	GND	Ground Pin
4	C_D	Pin for External Capacitor (for setting output delay)
5	SENSE	Voltage Detector Voltage Sense Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{DD}	Supply Voltage	−0.3 to 7.0	V
V_{SENSE}	SENSE Pin Voltage	−0.3 to 7.0	V
V_{DOUT}	Output Voltage (Nch Open Drain Output)	−0.3 to 7.0	V
	Output Voltage (CMOS Output)	−0.3 to V_{DD}+0.3	
I_{DOUT}	Output Current Nch Driver (Sink Current)	20	mA
	Output Current Pch Driver (Source Current)	−5	
P_D	Power Dissipation (SOT-23-5) *	420	mW
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

*) For Power Dissipation, please refer to PACKAGE INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING RATINGS

Symbol	Item	Rating	Unit
V_{DD}	Supply Voltage	1.0 to 6.0	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING RATINGS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating ratings. The semiconductor devices cannot operate normally over the recommended operating ratings, even if when they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating ratings.

ELECTRICAL CHARACTERISTICS

- **R3118xxxxA/C**

☐ **values indicate −40°C≤Ta≤85°C, $-V_{DET_S}$ means set detector threshold, V_{DD}=1V to 6V, unless otherwise noted.**

- **R3118xxxA/C** **(Ta=25°C)**

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	$-V_{DET_S}$ <1.6V	Ta=25°C	$-V_{DET_S}$ −0.0225	$-V_{DET_S}$	$-V_{DET_S}$ +0.0225	V
			−40°C≤Ta≤85°C	$-V_{DET_S}$ −0.0375	$-V_{DET_S}$	$-V_{DET_S}$ +0.0375	
		$-V_{DET_S}$≥1.6V	Ta=25°C	$-V_{DET_S}$ × 0.985	$-V_{DET_S}$	$-V_{DET_S}$ × 1.015	
			−40°C≤Ta≤85°C	$-V_{DET_S}$ × 0.975	$-V_{DET_S}$	$-V_{DET_S}$ × 1.025	
V_{HYS}	Detector threshold Hysteresis	Ta=25°C		$-V_{DET_S}$ × 0.040	$-V_{DET_S}$ × 0.055	$-V_{DET_S}$ × 0.070	V
		−40°C≤Ta≤85°C		$-V_{DET_S}$ × 0.035	$-V_{DET_S}$ × 0.055	$-V_{DET_S}$ × 0.075	

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
I_{SS}	Supply Current *1	V_{SENSE}=0V, V_{DD}=6V			0.480	1.450	μA
		V_{SENSE}=6V, V_{DD}=6V			0.400	1.200	
R_{SENSE}	Sense Resistor	V_{SENSE}=6V, V_{DD}=6V		9	34	58	MΩ
I_{DOUT}	Output Current (Driver Output Pin)	Nch V_{SENSE}=0V	V_{DD}=1V, V_{DOUT}=0.1V	0.150			mA
			V_{DD}=3V, V_{DOUT}=0.1V	0.550			
			V_{DD}=5V, V_{DOUT}=0.1V	0.850			
			V_{DD}=1V, V_{DOUT}=0.4V	0.400			
			V_{DD}=3V, V_{DOUT}=0.4V	2.100			
			V_{DD}=5V, V_{DOUT}=0.4V	3.300			
		Pch*2 V_{SENSE}=6V	V_{DD}=1V, V_{DOUT}=0.9V	6			μA
			V_{DD}=3V, V_{DOUT}=2.9V	30			
			V_{DD}=5V, V_{DOUT}=4.9V	45			
I_{LEAK}	Nch Driver Leakage Current *3	V_{SENSE}=6V, V_{DD}=6V, V_{DOUT}=6V				80	nA
R_{DIS}	C_D pin Discharge Tr. On Resistance	V_{SENSE}=6V, V_{DD}=1V, V_{CD}=0.4V		2.200		6.200	kΩ
		V_{SENSE}=6V, V_{DD}=3V, V_{CD}=0.4V		0.400		1.250	
		V_{SENSE}=6V, V_{DD}=5V, V_{CD}=0.4V		0.250		0.800	
t_{reset}	Detect Output Delay Time *4	Ta=25°C			80		μs
t_{delay}	Release Output Delay Time *5	Ta=25°C		70	100	130	ms
		−40°C≤Ta≤85°C		65	100	145	

All of unit are tested and specified under load conditions such that Tj≈Ta=25°C except for Detector Output Delay Time and Release Output Delay Time.

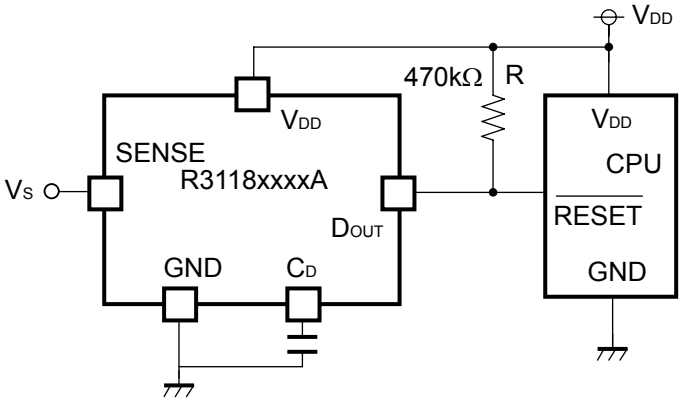
*1 Consumption current through SENSE pin is not included.

*2 In case of CMOS type
*3 In case of Nch Open Drain type
*4 In the case of CMOS output type: In the case that a 0.022μF capacitor is connected to the C_D pin, the time interval from forcing pulsive voltage between $-V_{DET_S}\times1.155V$ and $-V_{DET_S}\times0.9$ to SENSE pin, to when the output voltage of the D_{OUT} pin will reach from "H" to $V_{DD}/2$.
In the case of Nch Open drain output type: In the case that a 0.022μF capacitor is connected to the C_D pin and the D_{OUT} pin is pulled up to 5V with 470kΩ, the time interval from forcing pulsive voltage between $-V_{DET_S}\times1.155V$ and $-V_{DET_S}\times0.9V$ to SENSE pin, to when the output voltage reaches from "H" to 2.5V.
*5 In the case of CMOS output type: In the case that a 0.022μF capacitor is connected to the C_D pin, the time interval from forcing pulsive voltage between $-V_{DET_S}\times0.9$ and $-V_{DET_S}\times1.155V$ to SENSE pin, to when the output voltage of the D_{OUT} pin will reach from "L" to $V_{DD}/2$.
In the case of Nch Open drain output type: In the case that a 0.022μF capacitor is connected to the C_D pin and the D_{OUT} pin is pulled up to 5V with 470kΩ, the time interval from forcing pulsive voltage between $-V_{DET_S}\times0.9V$ and $-V_{DET_S}$x1.155V to SENSE pin, to when the output voltage reaches from "L" to 2.5V.

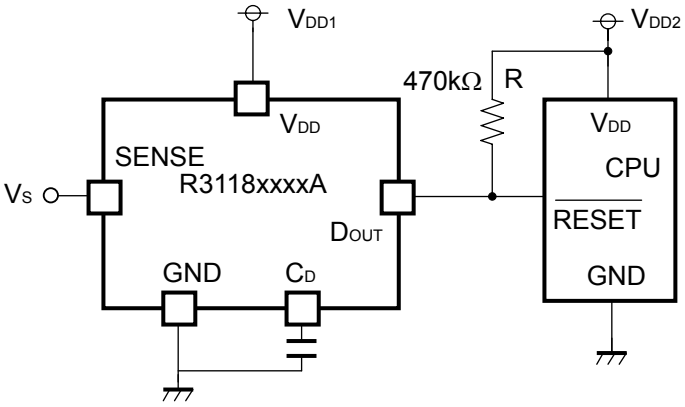
TYPICAL APPLICATION

- **R3118xxxxA CPU Reset Circuit (Nch Open Drain Output)**

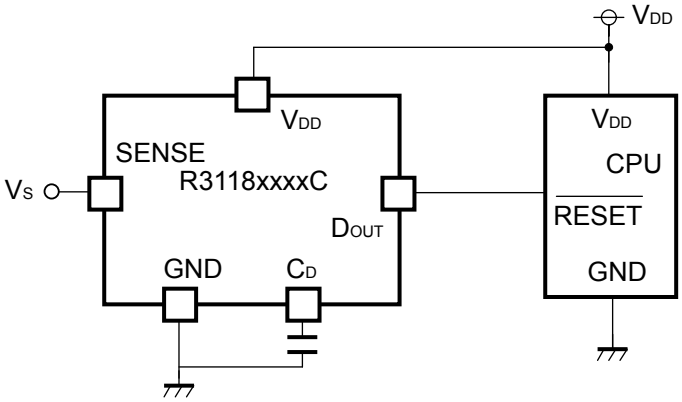
(1) V_{DD} pin Voltage to R3118xxxxA is equal to V_{DD} pin Voltage to CPU



(2) V_{DD} pin Voltage to R3118xxxxA is unequal to V_{DD} pin Voltage to CPU



- **R3118xxxxC CPU Reset Circuit (CMOS Output)**



TECHNICAL NOTES

When connecting resistors to the device's input pin

When connecting a resistor (R1) to an input of this device, the input voltage decreases by [Device's Consumption Current] x [Resistance Value] only. And, the cross conduction current*1, which occurs when changing from the detecting state to the release state, is decreased the input voltage by [Cross Conduction Current] x [Resistance Value] only. And then, this device will enter the re-detecting state if the input voltage reduction is larger than the difference between the detector voltage and the released voltage.

When the input resistance value is large and the VDD is gone up at mildly in the vicinity of the released voltage, repeating the above operation may result in the occurrence of output.

As shown in Figure A/B, set R1 to become 100kΩ or less as a guide, and connect C_{IN} of 0.1μF and more to between the input pin and GND. Besides, make evaluations including temperature properties under the actual usage condition, with using the evaluation board like this way. As result, make sure that the cross conduction current has no problem.

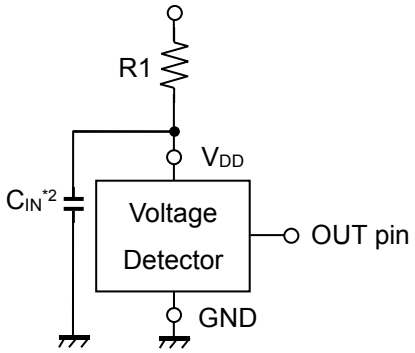


Figure A

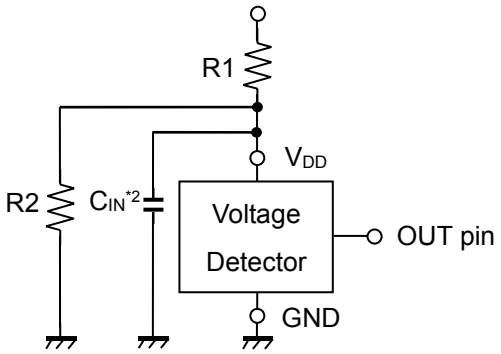
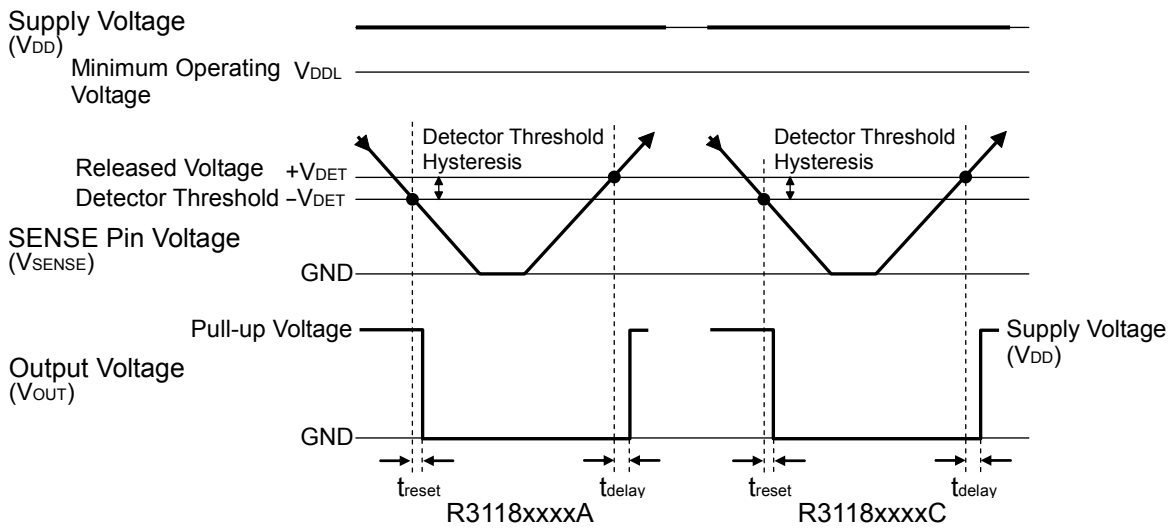


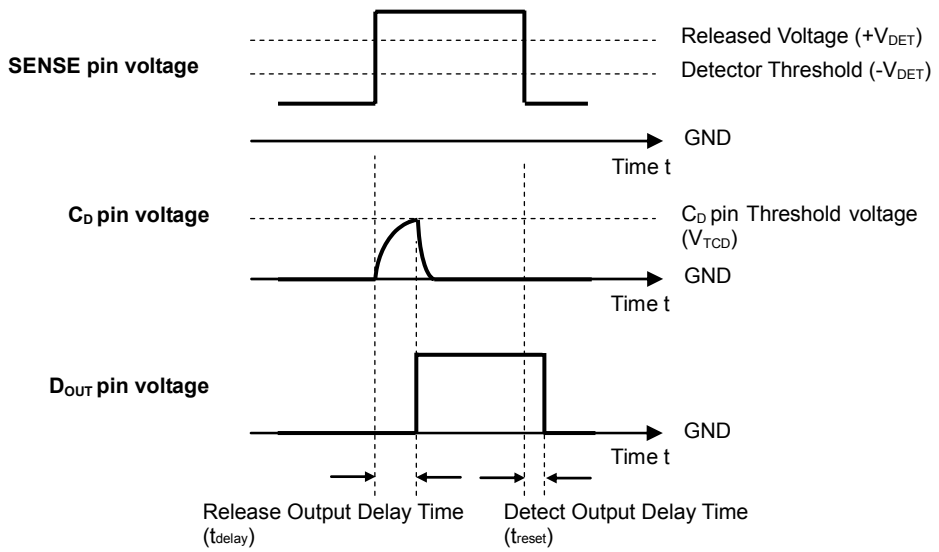
Figure B

*1 In the CMOS output type, a charging current for OUT pin is included.
*2 Note the bias dependence of capacitors.

TIMING CHART



DESCRIPTION OF OUTPUT DELAY OPERATION



Output Delay Operation Diagram

A higher voltage than the released voltage is forced to the SENSE pin, charge to the capacitor connected to C_D pin is started, then the C_D pin voltage increases. Until C_D pin voltage reaches to C_D pin threshold voltage, the output of D_{OUT} pin voltage keeps "L", then when C_D pin voltage is higher than C_D pin threshold voltage, the D_{OUT} pin voltage changes from "L" to "H". The released output delay time means the time interval from when the released voltage threshold or more voltage level is forced to SENSE pin to when D_{OUT} voltage changes from "L" to "H".

When the voltage of D_{OUT} pin reverses from "L" to "H", the discharge of the external capacitor connected to C_D pin starts. Therefore, the time interval from when the voltage lower than the detector threshold is forced to SENSE pin, to when the output voltage reverses from "H" to "L", or detector output delay time is constant and independent from the external capacitance value.

∗1. After the D_{OUT} pin voltage reverses from "L" to "H", if a voltage lower than the detector threshold is forced to SENSE pin before the capacitor connected to C_D pin is discharged, delay time will increase. The time interval (t_{DIS}) from when the capacitor connected to C_D pin is discharged completely to when the capacitor is charged to a certain C_D pin voltage (described as V_{CD} herein) can be calculated by power supply voltage (V_{DD}), external capacitance (C_D), on resistance of the C_D pin discharge transistor (R_{DIS}) as in the next formula:

$$t_{DIS} = -R_{DIS} \times C_D \times \ln(V_{CD}/V_{DD} \times 0.45))$$

∗2. During the released delay operation, only a small current will charge the external capacitor connected to C_D pin. If the leakage current between C_D pin and GND is large, the released delay time may increase or the detector may not be released.

∗3. During the released delay operation, if the V_{DD} pin voltage varies, the released output delay time will be also shift.

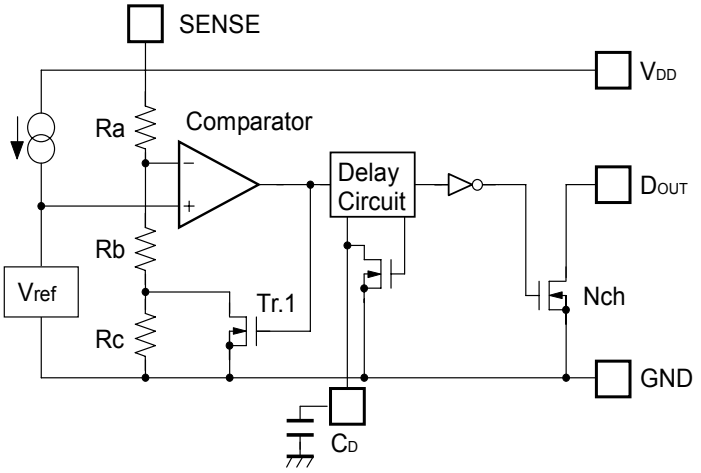
• How To Calculate Released Output Delay Time

The release output delay time (t_{delay}) can be calculated as in the next formula with an external capacitance value (C_D):

$$t_{delay}(s) = 4.545 \times 10^6 \times C_D(F)$$

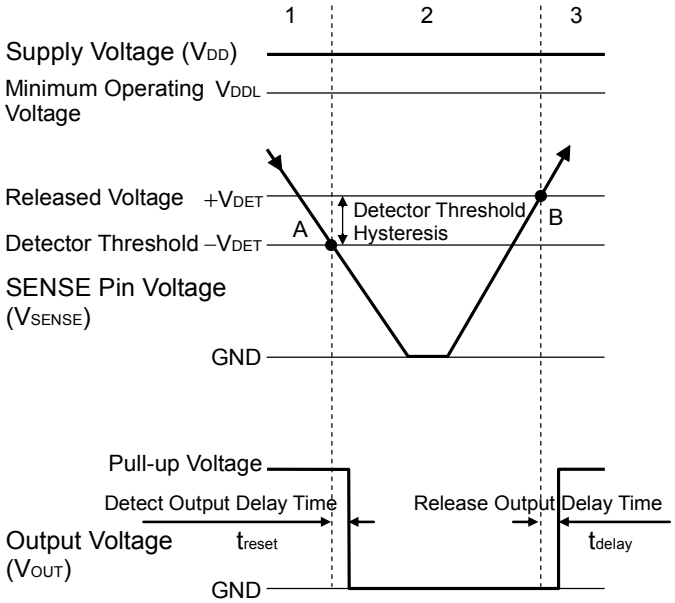
OPERATION

- **R3118xxxxA**



∗)D_{OUT} pin should be pulled-up to V_{DD} or an external voltage level.

Block diagram with an external capacitor (R3118xxxxA)



Step		1	2	3
Comparator (–) Pin Input Voltage		I	II	I
Comparator Output		L	H	L
Tr.1		OFF	ON	OFF
Output Tr.	Nch	OFF	ON	OFF

I $\frac{Rb+Rc}{Ra+Rb+Rc} \times V_{SENSE}$

II $\frac{Rb}{Ra+Rb} \times V_{SENSE}$

Operation Diagram

- **Explanation**

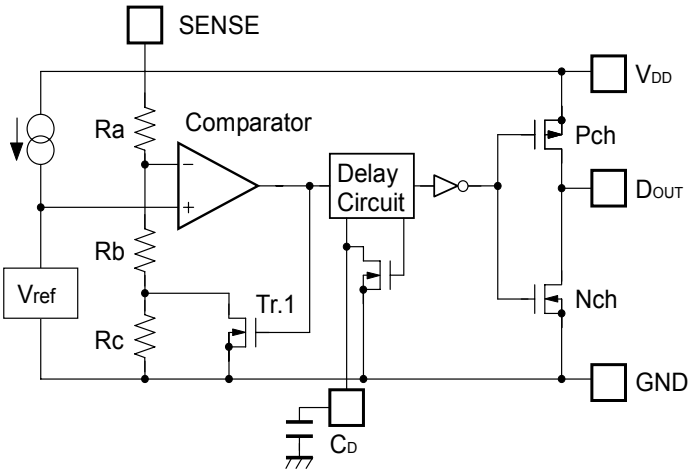
Step 1. The output voltage is equal to the pull-up voltage.

Step 2. At Point "A", Vref ≤ V_{SENSE}×(Rb+Rc)/(Ra+Rb+Rc) is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage (-V_{DET}). (When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the GND level.)

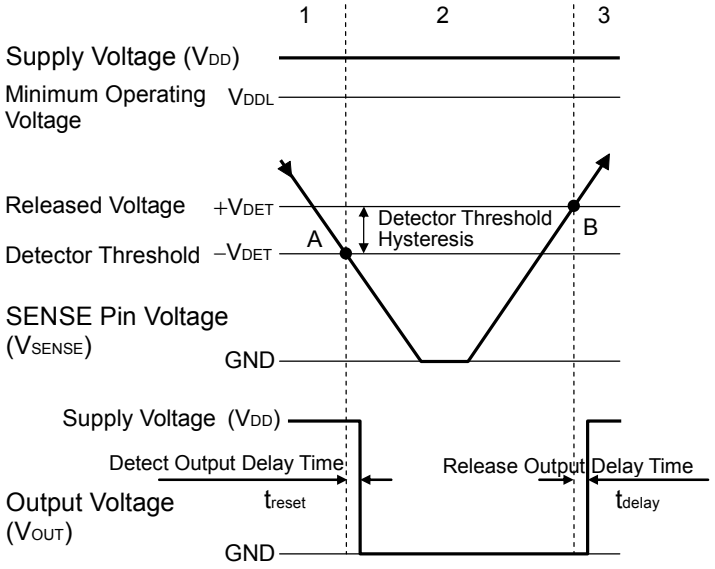
Step 3. At Point "B", V_{ref} ≤ V_{SENSE}×Rb/(Ra+Rb) is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the pull-up voltage. The voltage level of Point B means a released voltage (+V_{DET}).

∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

- **R3118xxxxC**



Block diagram with an external capacitor (R3118xxxxC)



Step		1	2	3
Comparator (−) Pin Input Voltage		I	II	I
Comparator Output		L	H	L
Tr.1		OFF	ON	OFF
Output Tr.	Pch	ON	OFF	ON
	Nch	OFF	ON	OFF

I $\frac{Rb+Rc}{Ra+Rb+Rc} \times V_{SENSE}$

II $\frac{Rb}{Ra+Rb} \times V_{SENSE}$

Operation Diagram

- **Explanation**

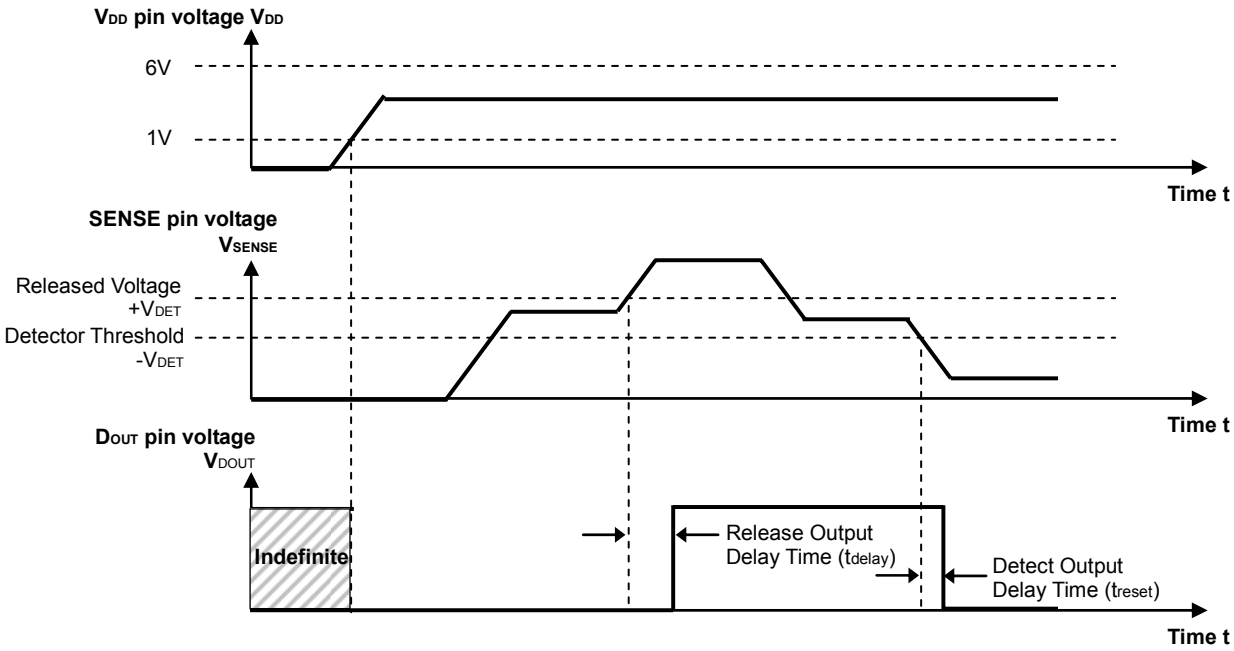
Step 1. The output voltage is equal to the supply voltage (V_{DD}).

Step 2. At Point "A", $V_{ref} \geq V_{SENSE} \times (Rb+Rc)/(Ra+Rb+Rc)$ is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage ($-V_{DET}$). (When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the GND level.)

Step 3. At Point "B", $V_{ref} \leq V_{SENSE} \times Rb/(Ra+Rb)$ is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the supply voltage (V_{DD}). The voltage level of Point B means a released voltage ($+V_{DET}$).

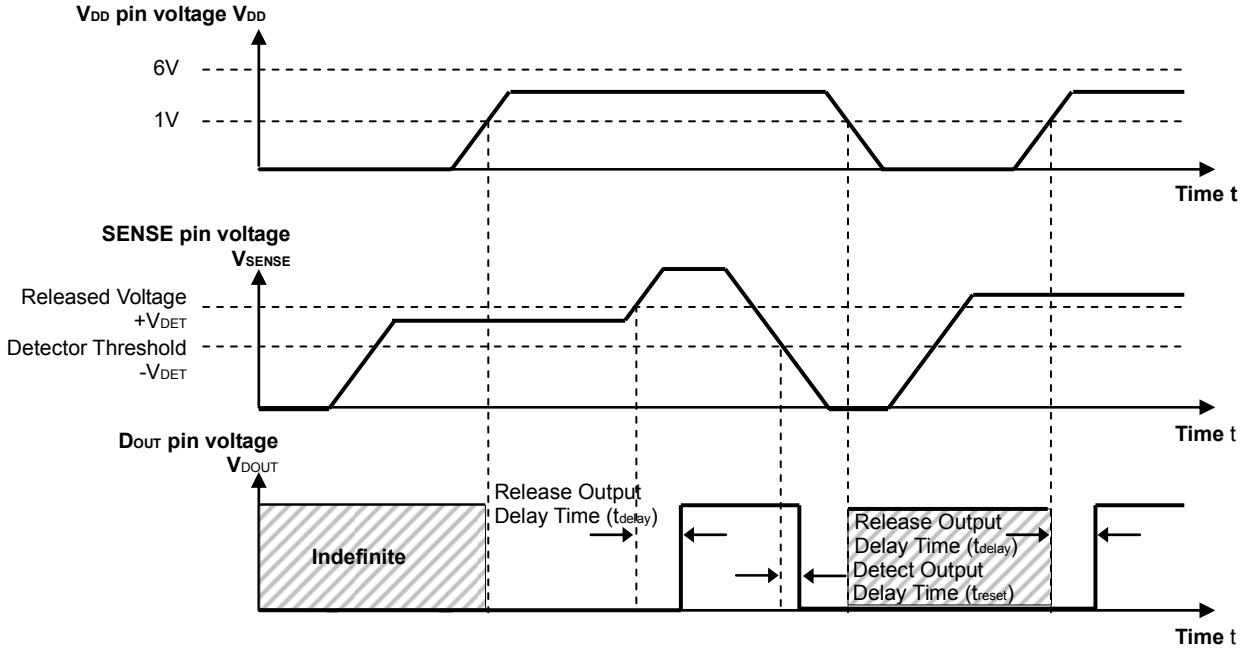
∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

- **In the case of the SENSE pin voltage is forced after the V_{DD} pin voltage is forced.**



If a voltage is applied to SENSE pin after a power (in the range from 1V to 6V) is applied to V_{DD} pin, D_{OUT} pin becomes "L" when the SENSE pin voltage is less than released voltage $+V_{DET}$, ,and D_{OUT} pin becomes "H" when the SENSE pin voltage is equal or more than the released voltage $+V_{DET}$.

- **In the case of the V_{DD} pin voltage is forced after the SENSE pin voltage is forced.**



In the case of the SENSE pin voltage is less than released voltage $+V_{DET}$, when the V_{DD} pin voltage becomes to 1V or more, "L" output of D_{OUT} is determined. In case of the SENSE pin voltage is equal or more than the released voltage $+V_{DET}$, when the V_{DD} pin voltage becomes to 1V or more, "H" output of D_{OUT} is determined.

∗ If the turn on speed of the supply voltage of the V_{DD} pin up to 1V is slower than the1V/s, connect 0.001μF or more capacitor to C_D pin, otherwise, the output of D_{OUT} pin may indefinite.

PACKAGE INFORMATION

Power Dissipation (SOT-23-5)

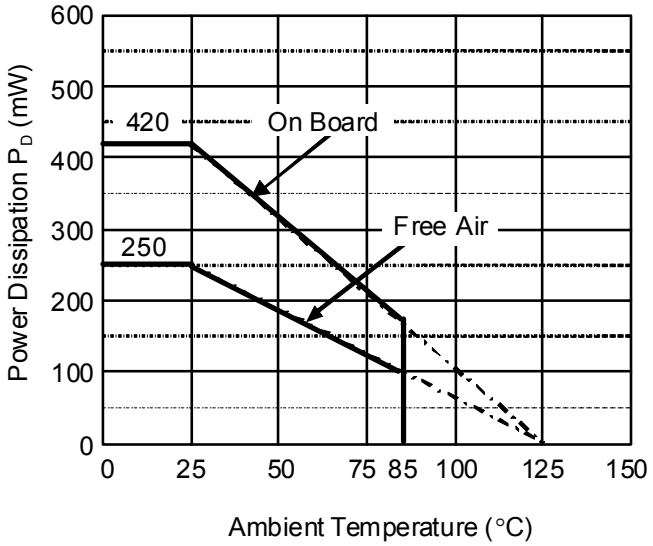
Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:
(Power Dissipation (SOT-23-5) is substitution of SOT-23-6.)

Measurement Conditions

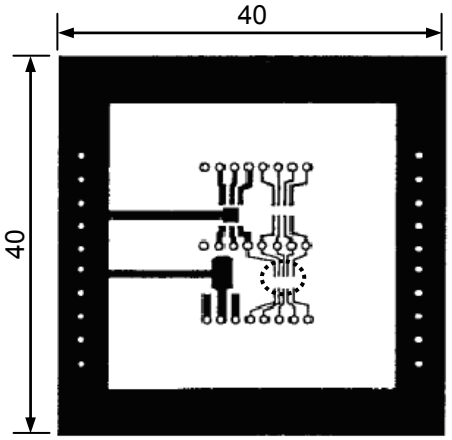
	Standard Test Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm x 40mm x 1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.5mm x 44pcs

Measurement Result **(Ta=25°C, Tjmax=125°C)**

	Standard Land Pattern	Free Air
Power Dissipation	420mW	250mW
Thermal Resistance	θja = (125-25°C)/0.42W= 238°C/W	400°C/W



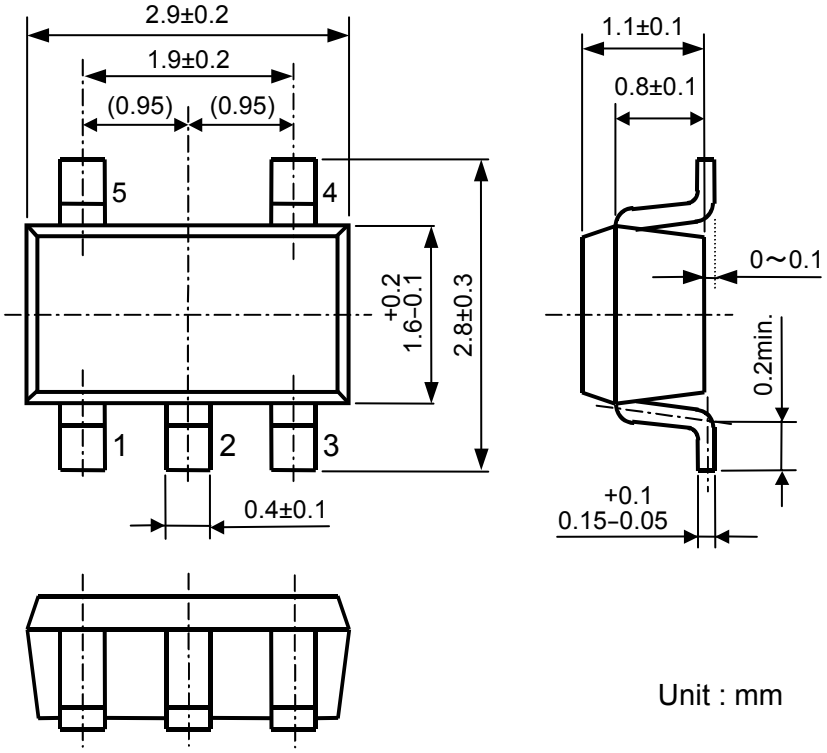
Power Dissipation



Measurement Board Pattern

IC Mount Area (Unit: mm)

Package Dimensions (SOT-23-5)

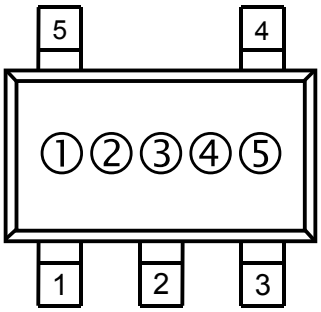


SOT-23-5 Package Dimensions

Mark Specifications (SOT-23-5)

①②③: Product Code … **Refer to *"Mark Specification Table"***

④⑤: Lot Number … Alphanumeric Serial Number



SOT-23-5 Mark Specifications

R3118N Mark Specification Table (SOT-23-5)

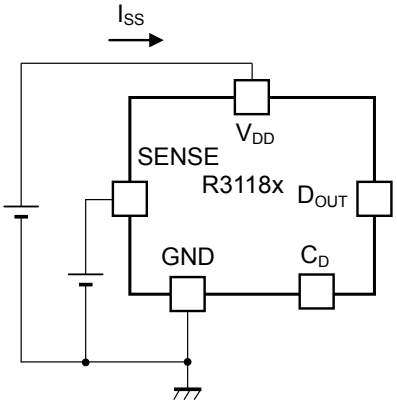
R3118Nxx1A

Product Name	①②③	V_{SET}
R3118N061A	SAA	0.6V
R3118N071A	SAB	0.7V
R3118N081A	SAC	0.8V
R3118N091A	SAD	0.9V
R3118N101A	SAE	1.0V
R3118N111A	SAF	1.1V
R3118N121A	SAG	1.2V
R3118N131A	SAH	1.3V
R3118N141A	SAJ	1.4V
R3118N151A	SAK	1.5V
R3118N161A	SAL	1.6V
R3118N171A	SAM	1.7V
R3118N181A	SAN	1.8V
R3118N191A	SAP	1.9V
R3118N201A	SAQ	2.0V
R3118N211A	SAR	2.1V
R3118N221A	SAS	2.2V
R3118N231A	SAT	2.3V
R3118N241A	SAU	2.4V
R3118N251A	SAV	2.5V
R3118N261A	SAW	2.6V
R3118N271A	SAX	2.7V
R3118N281A	SAY	2.8V
R3118N291A	SAZ	2.9V
R3118N301A	TAA	3.0V
R3118N311A	TAB	3.1V
R3118N321A	TAC	3.2V
R3118N331A	TAD	3.3V
R3118N341A	TAE	3.4V
R3118N351A	TAF	3.5V
R3118N361A	TAG	3.6V
R3118N371A	TAH	3.7V
R3118N381A	TAJ	3.8V
R3118N391A	TAK	3.9V
R3118N401A	TAL	4.0V
R3118N411A	TAM	4.1V
R3118N421A	TAN	4.2V
R3118N431A	TAP	4.3V
R3118N441A	TAQ	4.4V
R3118N451A	TAR	4.5V
R3118N461A	TAS	4.6V
R3118N471A	TAT	4.7V
R3118N481A	TAU	4.8V
R3118N491A	TAV	4.9V
R3118N501A	TAW	5.0V

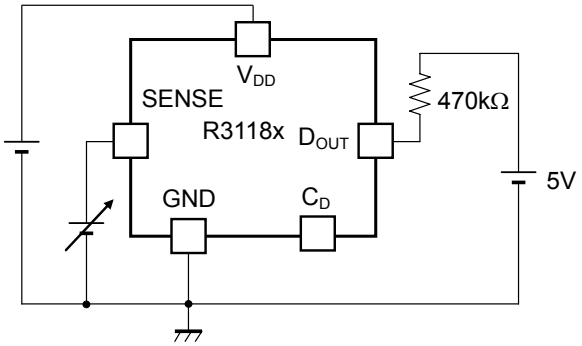
R3118Nxx1C

Product Name	①②③	V_{SET}
R3118N061C	SBA	0.6V
R3118N071C	SBB	0.7V
R3118N081C	SBC	0.8V
R3118N091C	SBD	0.9V
R3118N101C	SBE	1.0V
R3118N111C	SBF	1.1V
R3118N121C	SBG	1.2V
R3118N131C	SBH	1.3V
R3118N141C	SBJ	1.4V
R3118N151C	SBK	1.5V
R3118N161C	SBL	1.6V
R3118N171C	SBM	1.7V
R3118N181C	SBN	1.8V
R3118N191C	SBP	1.9V
R3118N201C	SBQ	2.0V
R3118N211C	SBR	2.1V
R3118N221C	SBS	2.2V
R3118N231C	SBT	2.3V
R3118N241C	SBU	2.4V
R3118N251C	SBV	2.5V
R3118N261C	SBW	2.6V
R3118N271C	SBX	2.7V
R3118N281C	SBY	2.8V
R3118N291C	SBZ	2.9V
R3118N301C	TBA	3.0V
R3118N311C	TBB	3.1V
R3118N321C	TBC	3.2V
R3118N331C	TBD	3.3V
R3118N341C	TBE	3.4V
R3118N351C	TBF	3.5V
R3118N361C	TBG	3.6V
R3118N371C	TBH	3.7V
R3118N381C	TBJ	3.8V
R3118N391C	TBK	3.9V
R3118N401C	TBL	4.0V
R3118N411C	TBM	4.1V
R3118N421C	TBN	4.2V
R3118N431C	TBP	4.3V
R3118N441C	TBQ	4.4V
R3118N451C	TBR	4.5V
R3118N461C	TBS	4.6V
R3118N471C	TBT	4.7V
R3118N481C	TBU	4.8V
R3118N491C	TBV	4.9V
R3118N501C	TBW	5.0V

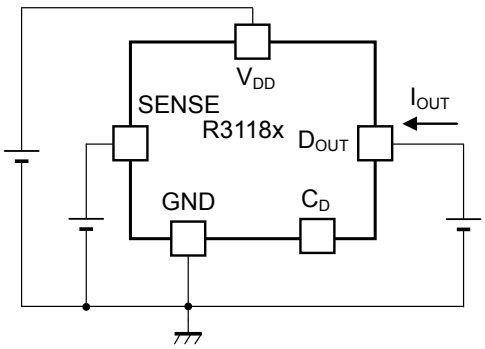
TEST CIRCUITS



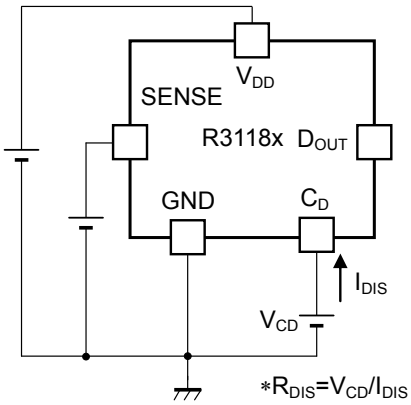
Supply Current Test Circuit



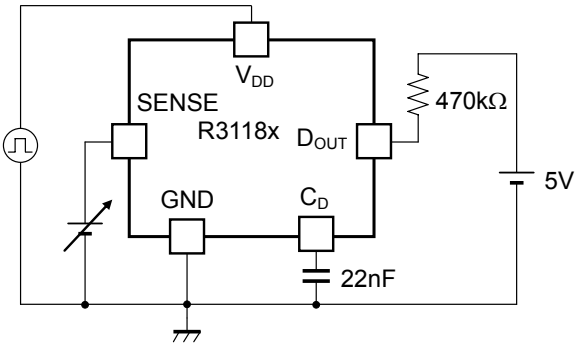
Detector Threshold Test Circuit
(Pull-up circuit is not necessary for CMOS Output type.)



Nch/Pch Driver Output Current Test Circuit



C_D pin Discharge Transistor On resistance Test Circuit



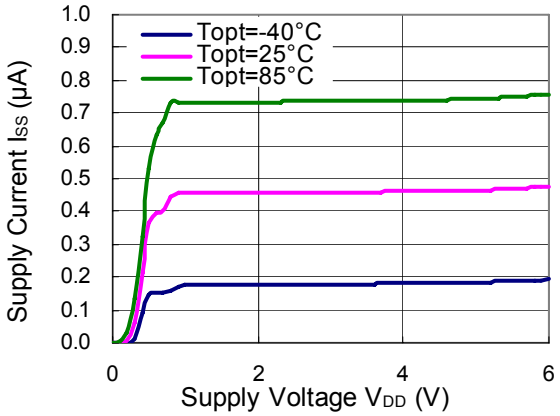
Detect output delay time/Release output delay time Test Circuit
(Pull-up circuit is not necessary for CMOS Output type.)

TYPICAL CHARACTERISTICS

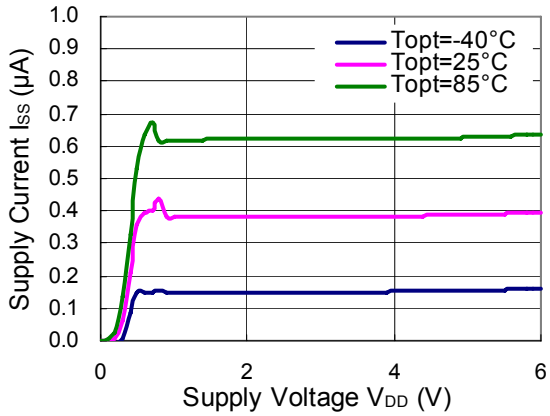
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Supply Current vs. Supply Voltage

R3118xxxxA/C (V_{SENSE}=0V)

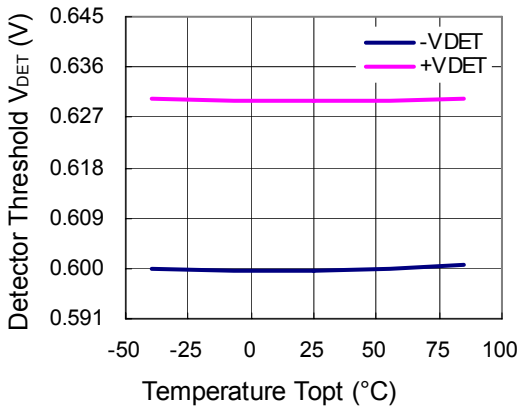


R3118xxxxA/C (V_{SENSE}=6V)

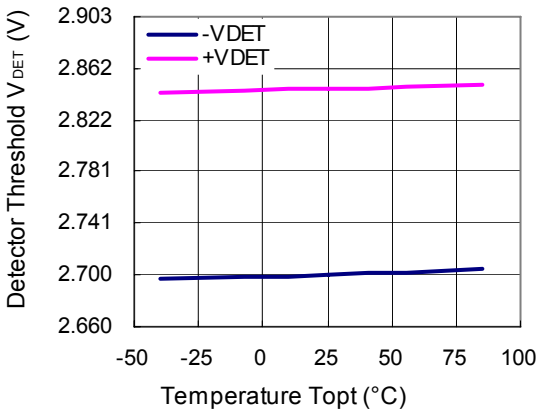


2) Detector Threshold vs. Temperature

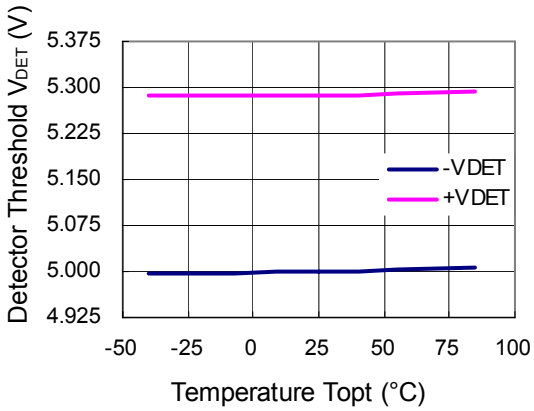
R3118x06xA/C (V_{DD}=5.3V)



R3118x27xA/C (V_{DD}=5.3V)

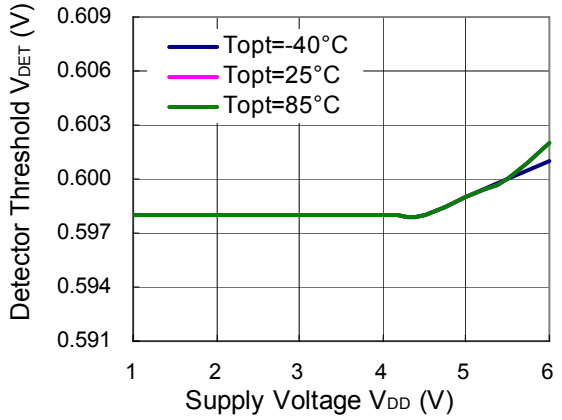


R3118x50xA/C (V_{DD}=5.3V)

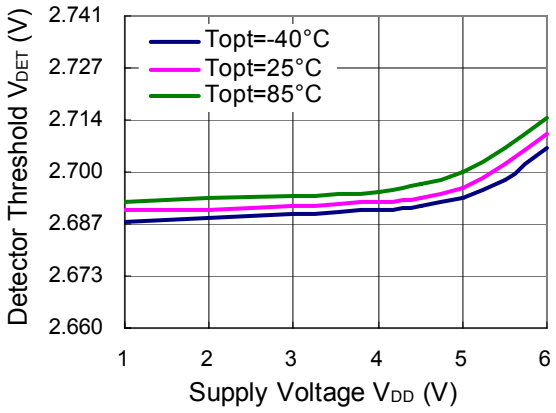


3) Detector Threshold vs. Supply Voltage

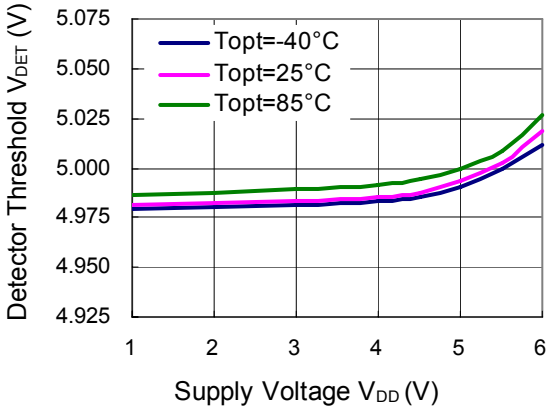
R3118x06xA/C



R3118x27xA/C

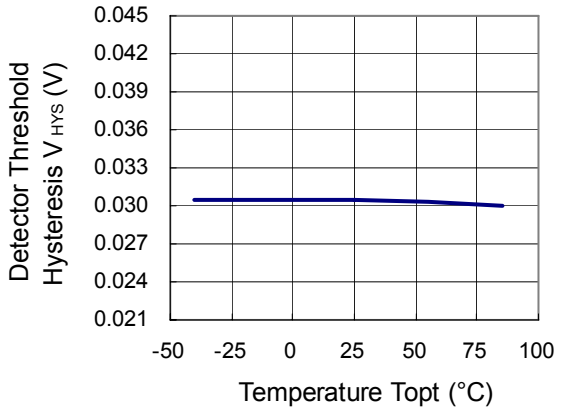


R3118x50xA/C

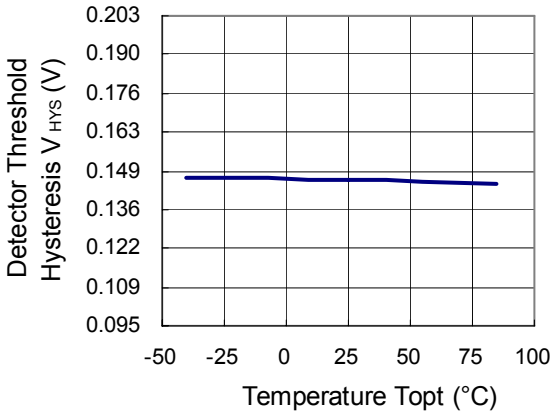


4) Hysteresis vs. Temperature

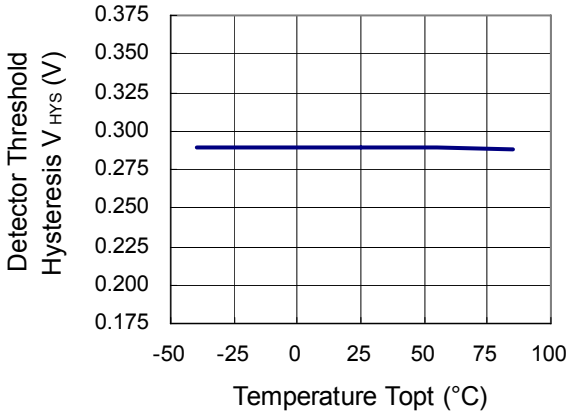
R3118x06xA/C (V_{DD}=5.3V)



R3118x27xA/C (V_{DD}=5.3V)

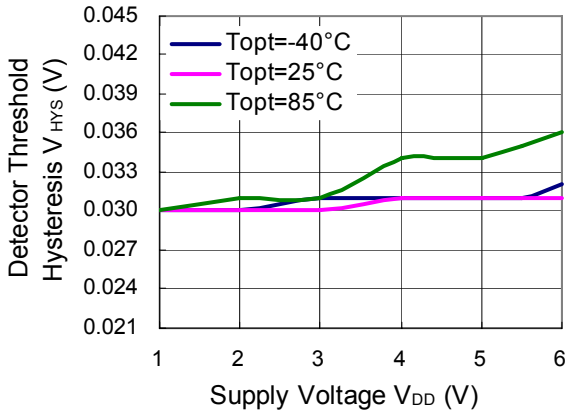


R3118x50xA/C (V_{DD}=5.3V)

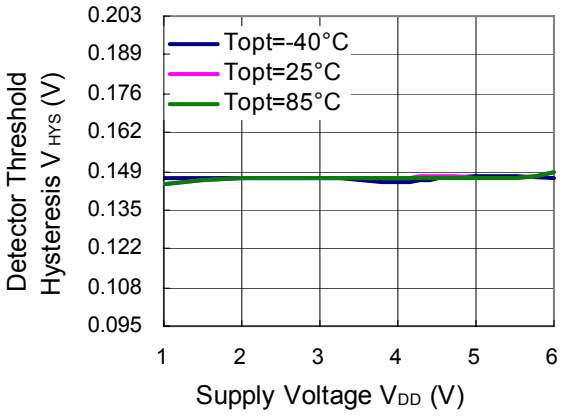


5) Hysteresis vs. Supply Voltage

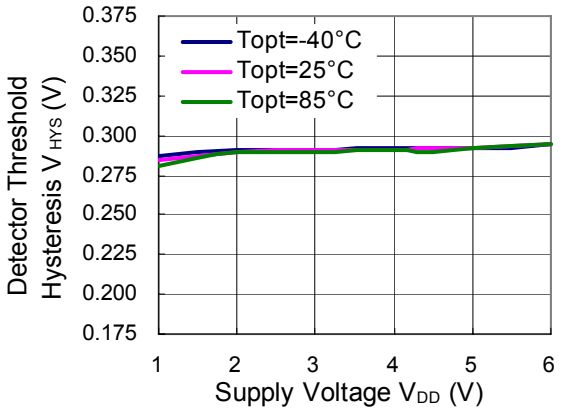
R3118x06xA/C



R3118x27xA/C

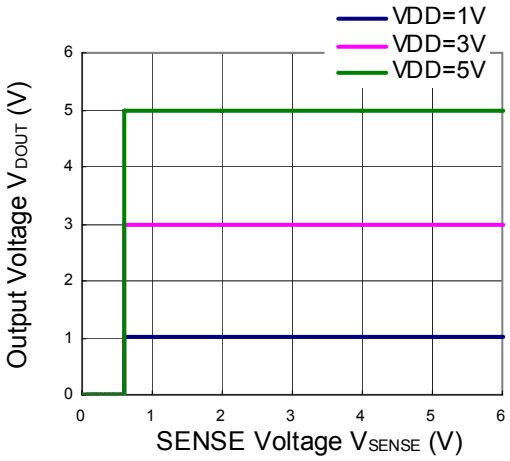


R3118x50xA/C

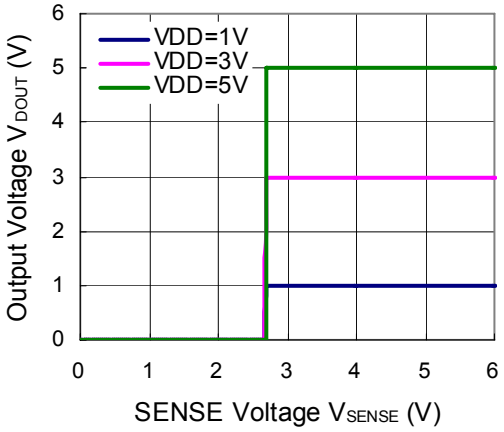


6) Output Voltage vs. SENSE Voltage (DOUT pin is pulled up to VDD pin via 470kΩ.)

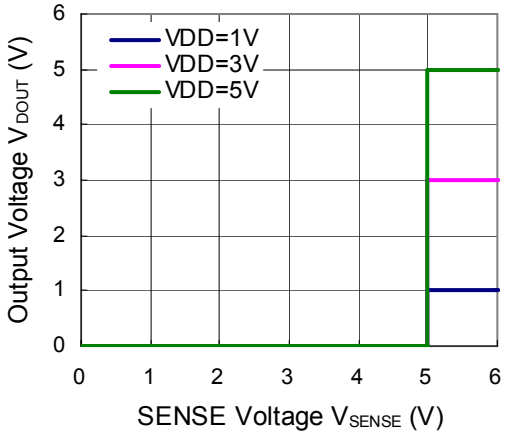
R3118x06xA/C



R3118x27xA/C

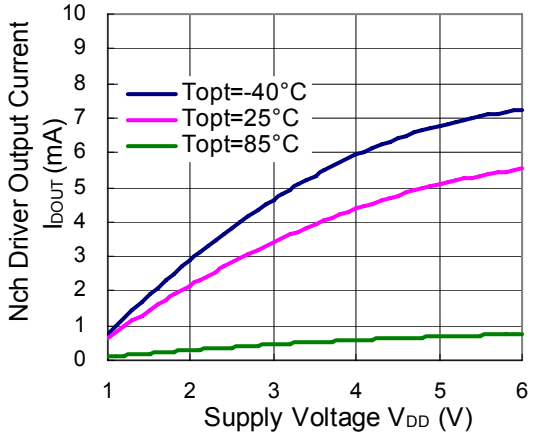


R3118x50xA/C



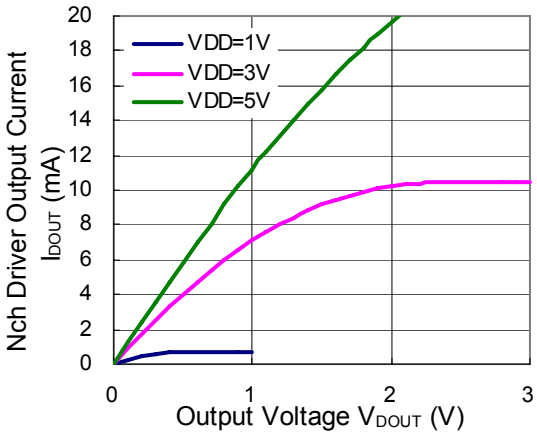
7) Nch Driver Output Current vs. Supply Voltage

R3118xxxxA/C (VDOUT=0.4V)



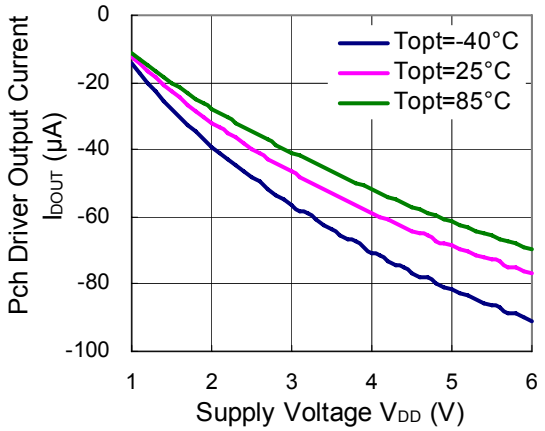
8) Nch Driver Output Current vs. Output Voltage

R3118xxxxA/C



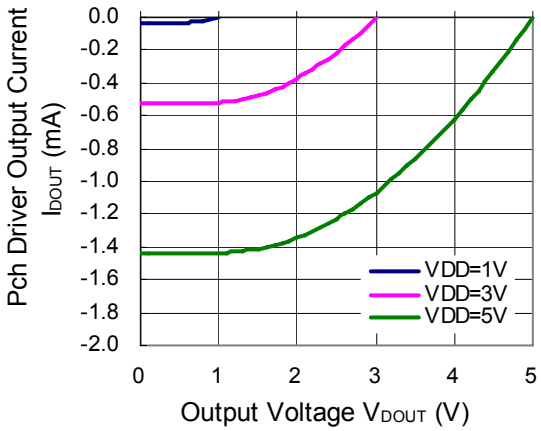
9) Pch Driver Output Current vs. Supply Voltage

R3118xxxxA/C (V_{DOUT}=V_{DD}–0.1V)



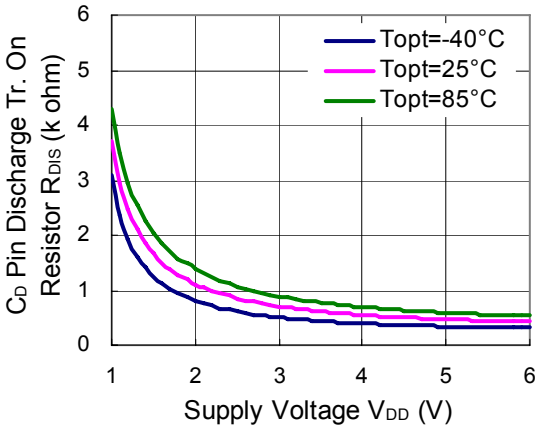
10) Pch Driver Output current vs. Output voltage

R3118xxxxA/C



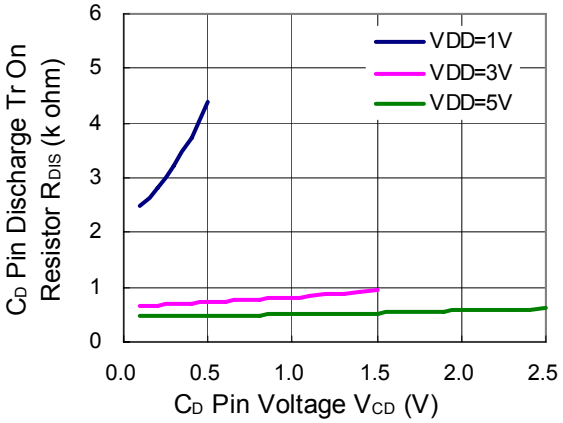
11) C_D pin Discharge Tr. On Resistance vs. Supply Voltage

R3118xxxxA/C (V_{CD}=0.4V)



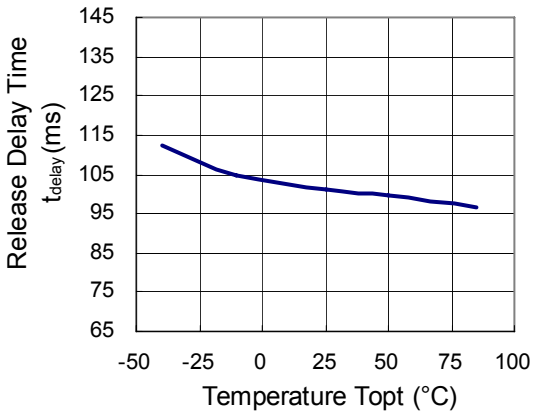
12) C_D pin Discharge Transistor On Resistance vs. C_D pin voltage

R3118xxxxA/C



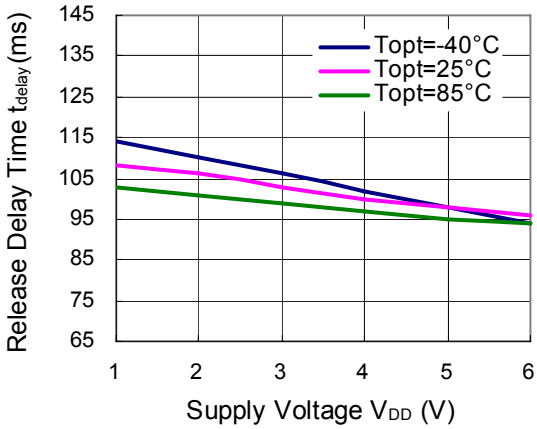
13) Release Output Delay Time vs. Temperature

R3118xxxxA/C (V_{DD}=4V, C_D=0.022μF)



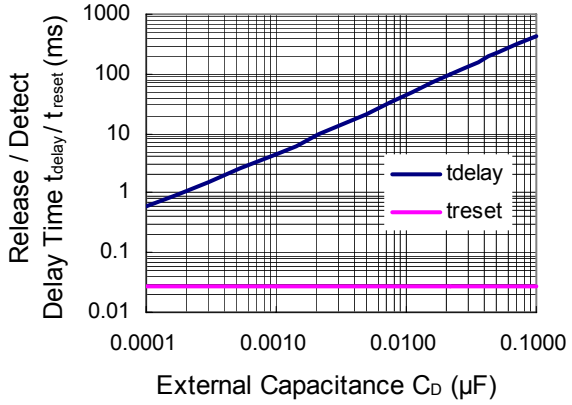
14) Release Output Delay Time vs. Supply Voltage

R3118xxxxA/C (C_D=0.022μF)

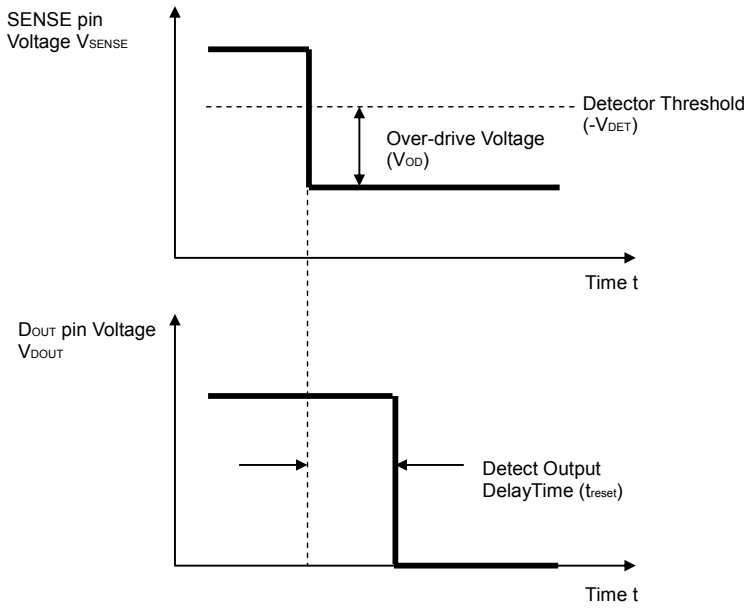


15) Detect Output Delay Time/Release Output Delay Time vs. C_D pin External Capacitance

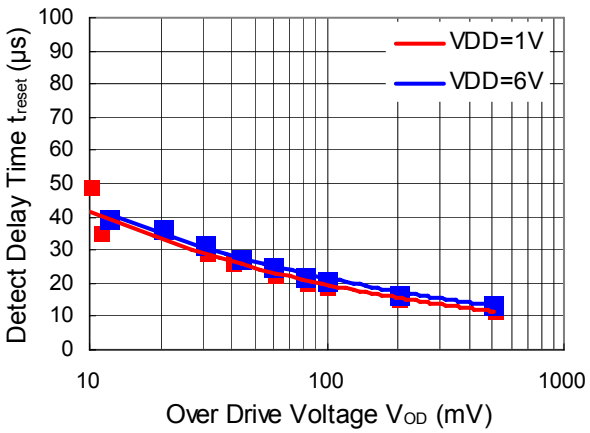
R3118xxxxA/C (V_{DD}=4V)



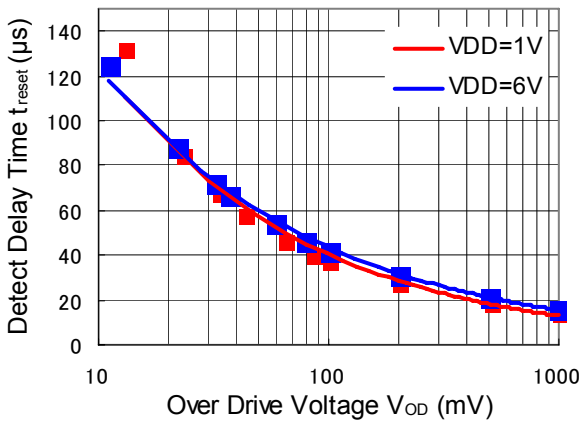
16) Detect Output Delay time vs. Over-drive Voltage



R3118x06xA/C（CD=none）

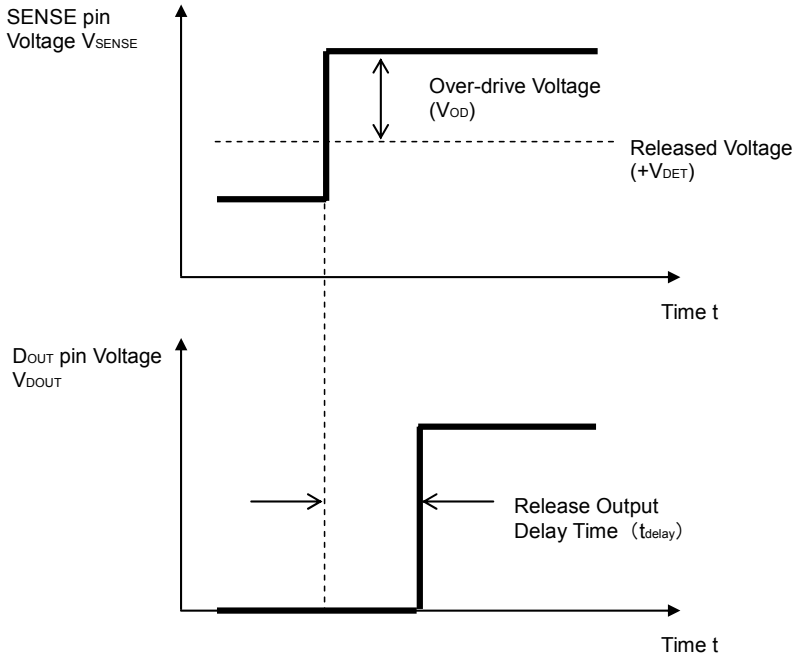


R3118x50xA/C（CD=none）

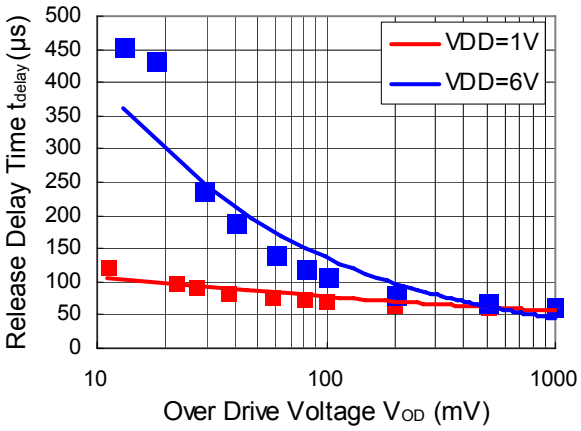


The pulse shorter than the detect output delay time cannot be detected, and "L" does not output from DOUT pin.

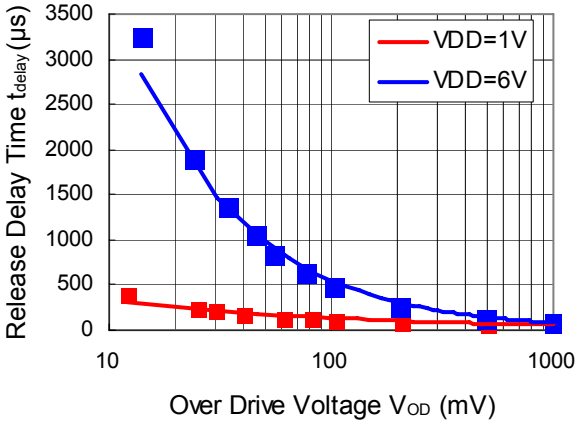
17) Release Output Delay time vs. Over-drive Voltage



R3118x06xA/C（CD=none）



R3118x50xA/C（CD=none）



· If the pulse is shorter than the output release delay time, the R3118 cannot be released and "H" does not output from DOUT pin.
· If the attachment capacitor for CD pin for setting a delay time is too small and the difference between the released voltage threshold and the actual released voltage is too small or the slope for rising voltage of the SENSE pin is too slow, the output delay time tolerance will be worse.
Ex. Attachment capacitor=0.0001μF, Released voltage threshold=4.725V, Actual released voltage=4.75V In this case, the calculated delay time=0.4545ms, however, over-drive voltage is only 25mV. Therefore, the actual delay time will be approximately 2.4545ms. If the attachment capacitor=0.001μF and other conditions are same as above, the calculated delay time=4.545ms, and the actual delay time will be approximately 6.545ms. If the attachment capacitor=0.01μF and other conditions are same as above, the calculated delay time=45.45ms, and the actual delay time will be approximately 47.45ms.

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to Ricoh sales representatives for the latest information thereon.
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