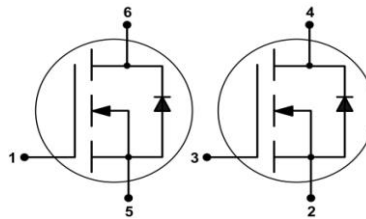
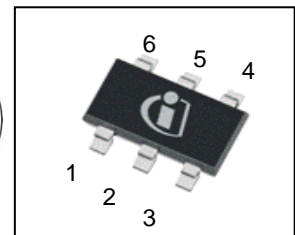


OptiMOS™ 2 Small-Signal-Transistor
Features

- Dual N-channel
- Enhancement mode
- Super Logic level (2.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen free according to IEC61249-2-21


PG-TSOP6


| Type | Package | Tape and Reel Information | Marking | Lead Free | Packing |
|---------|---------|---------------------------|---------|-----------|---------|
| BSL207N | TSOP-6 | H6327: 3000 pcs/ reel | sPL | Yes | Non dry |

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter ¹⁾ | Symbol | Conditions | Value | Unit |
|-------------------------------------|-------------------|--|-------------|-------------------|
| Continuous drain current | I_D | $T_A=25\text{ °C}$ | 2.1 | A |
| | | $T_A=70\text{ °C}$ | 1.7 | |
| Pulsed drain current | $I_{D,pulse}$ | $T_A=25\text{ °C}$ | 8.4 | |
| Avalanche energy, single pulse | E_{AS} | $I_D=2.1\text{ A}$, $R_{GS}=25\ \Omega$ | 10.8 | mJ |
| Reverse diode dv/dt | dv/dt | $I_D=2.1\text{ A}$, $V_{DS}=16\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$ | 6 | kV/ μs |
| Gate source voltage | V_{GS} | | ± 12 | V |
| Power dissipation ¹⁾ | P_{tot} | $T_A=25\text{ °C}$ | 0.5 | W |
| Operating and storage temperature | T_j , T_{stg} | | -55 ... 150 | °C |
| ESD Class | | JESD22-A114 -HBM | 0 (<250V) | |
| Soldering Temperature | | | 260 °C | |
| IEC climatic category; DIN IEC 68-1 | | | 55/150/56 | |

¹⁾ Remark: one of both transistors in operation

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Thermal characteristics

| | | | | | | |
|--|------------|---------------------------------|---|---|-----|-----|
| Thermal resistance, junction - ambient | R_{thJA} | minimal footprint ²⁾ | - | - | 250 | K/W |
|--|------------|---------------------------------|---|---|-----|-----|

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|------|-----|------------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$ | 20 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=11\text{ }\mu\text{A}$ | 0.7 | 0.95 | 1.2 | |
| Drain-source leakage current | I_{DSS} | $V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$ | - | - | 1 | μA |
| | | $V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$ | - | - | 100 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=12\text{ V}, V_{DS}=0\text{ V}$ | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=2.5\text{ V}, I_D=1.7\text{ A}$ | - | 81 | 110 | $\text{m}\Omega$ |
| | | $V_{GS}=4.5\text{ V}, I_D=2.1\text{ A}$ | - | 58 | 70 | |
| Transconductance | g_{fs} | $ V_{DS} >2 I_D R_{DS(on)max}, I_D=1.7\text{ A}$ | - | 7 | - | S |

²⁾ Performed on a 40mm² FR4 PCB. The traces are 1mm wide, 70 μm thick and 20mm long; they are present on both sides of the PCB.

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics

| | | | | | | |
|------------------------------|--------------|---|---|-----|-----|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=10\text{ V},$ $f=1\text{ MHz}$ | - | 315 | 419 | pF |
| Output capacitance | C_{oss} | | - | 114 | 152 | |
| Reverse transfer capacitance | C_{rss} | | - | 16 | 24 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=10\text{ V}, V_{GS}=4.5\text{ V},$ $I_D=2.1\text{ A}, R_{G,ext}=6\ \Omega$ | - | 5.4 | - | ns |
| Rise time | t_r | | - | 2.8 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 11 | - | |
| Fall time | t_f | | - | 2.4 | - | |

Gate Charge Characteristics

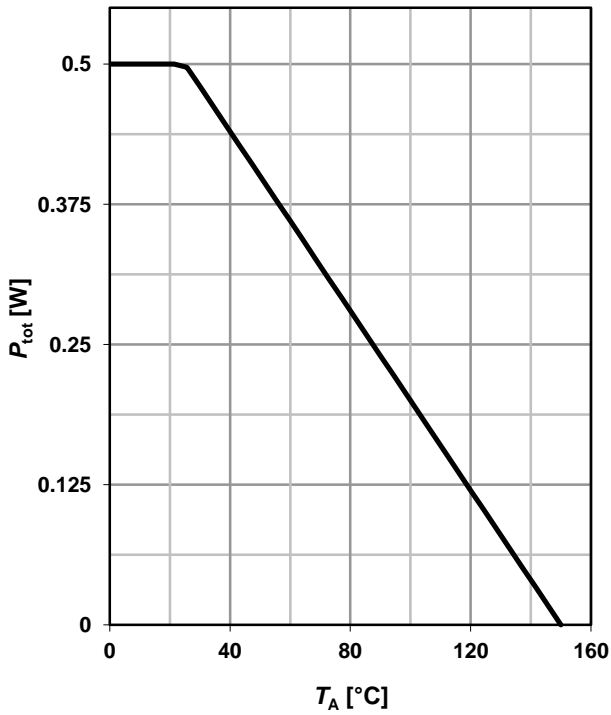
| | | | | | | |
|-----------------------|---------------|--|---|------|---|----|
| Gate to source charge | Q_{gs} | $V_{DD}=10\text{ V}, I_D=2.1\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$ | - | 0.65 | - | nC |
| Gate to drain charge | Q_{gd} | | - | 0.4 | - | |
| Gate charge total | Q_g | | - | 2.1 | - | |
| Gate plateau voltage | $V_{plateau}$ | | - | 2 | - | V |

Reverse Diode

| | | | | | | |
|----------------------------------|---------------|--|---|-----|-----|----|
| Diode continuous forward current | I_S | $T_A=25\text{ }^\circ\text{C}$ | - | - | 0.5 | A |
| Diode pulse current | $I_{S,pulse}$ | | - | - | 8.4 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=2.1\text{ A},$ $T_j=25\text{ }^\circ\text{C}$ | - | 0.8 | 1.2 | V |
| Reverse recovery time | t_{rr} | $V_R=10\text{ V}, I_F=2.1\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$ | - | 10 | - | ns |
| Reverse recovery charge | Q_{rr} | | - | 2.4 | - | nC |

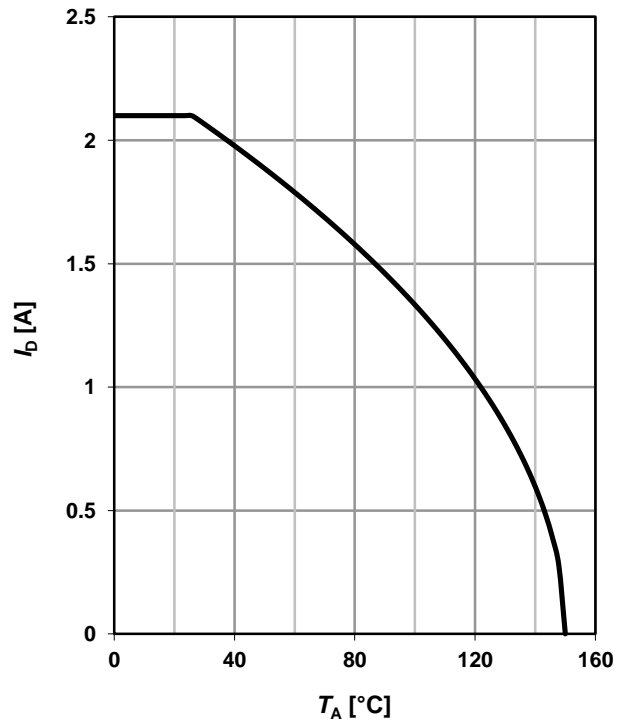
1 Power dissipation

$P_{tot}=f(T_A)$



2 Drain current

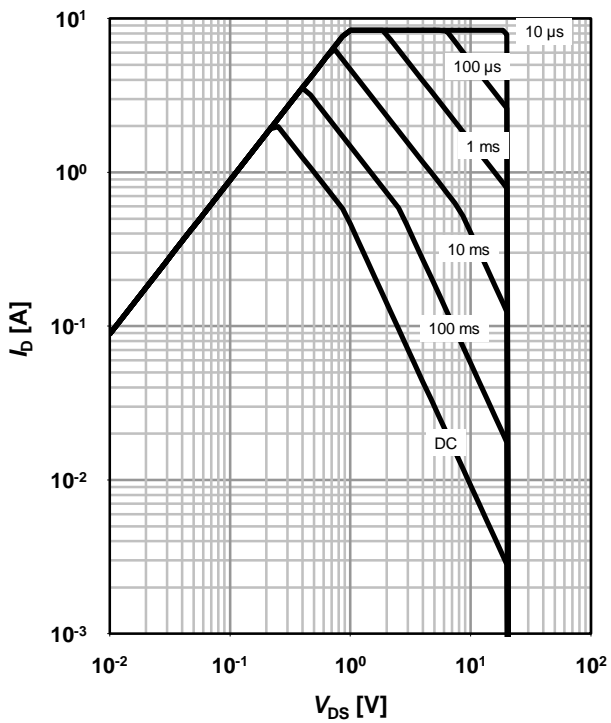
$I_D=f(T_A); V_{GS} \geq 4.5 V$



3 Safe operating area

$I_D=f(V_{DS}); T_A=25\text{ °C}; D=0$

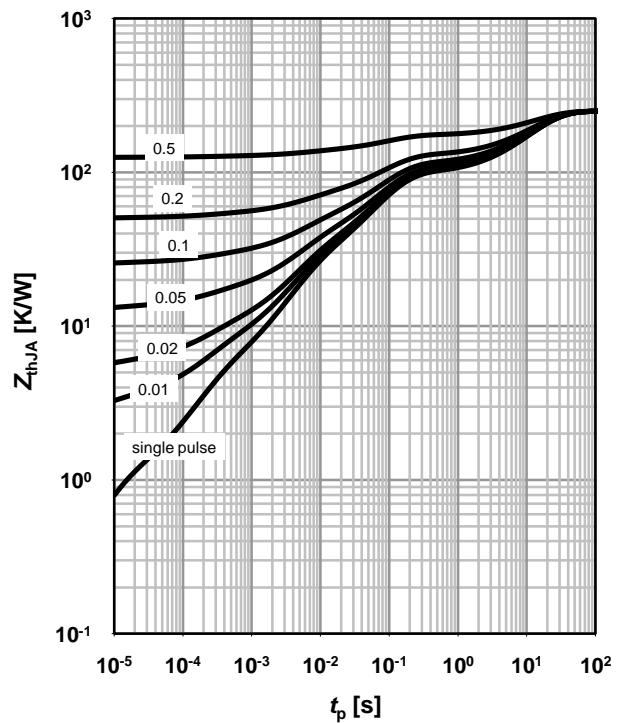
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJA}=f(t_p)$

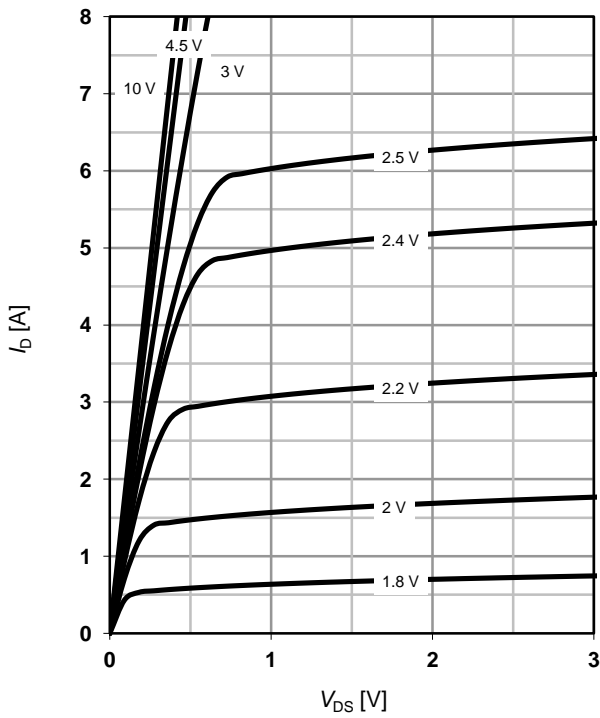
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

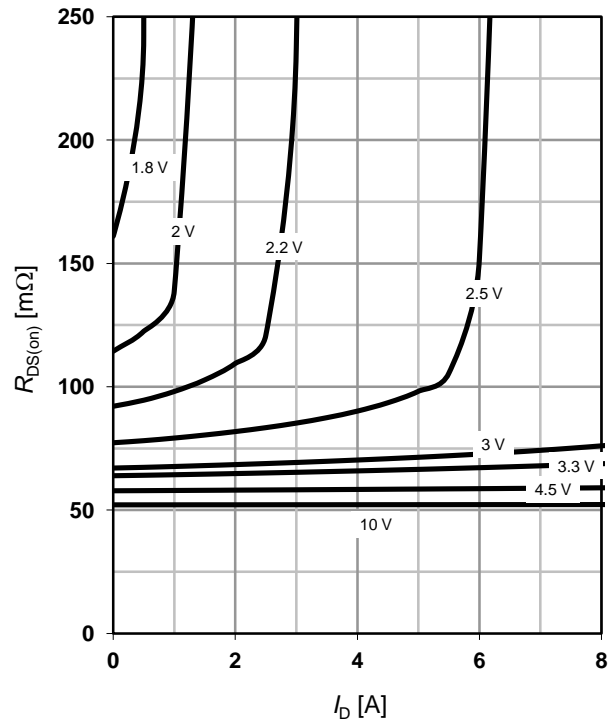
parameter: V_{GS}



6 Typ. drain-source on resistance

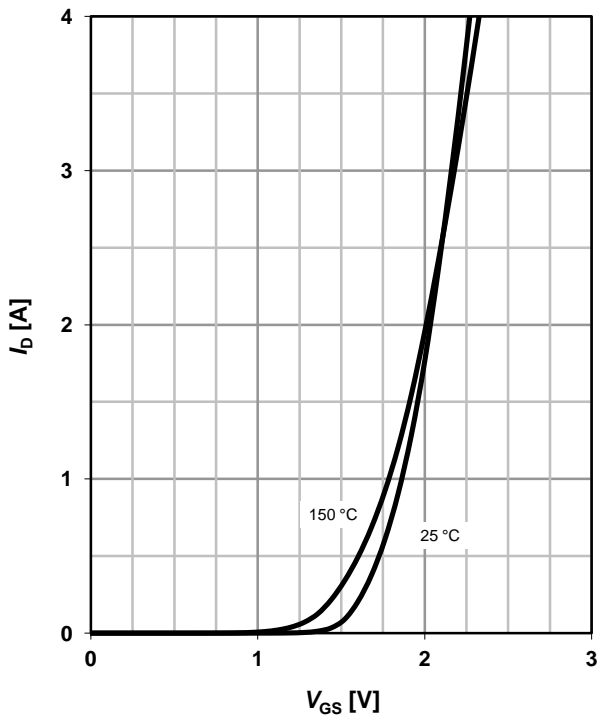
$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

parameter: V_{GS}



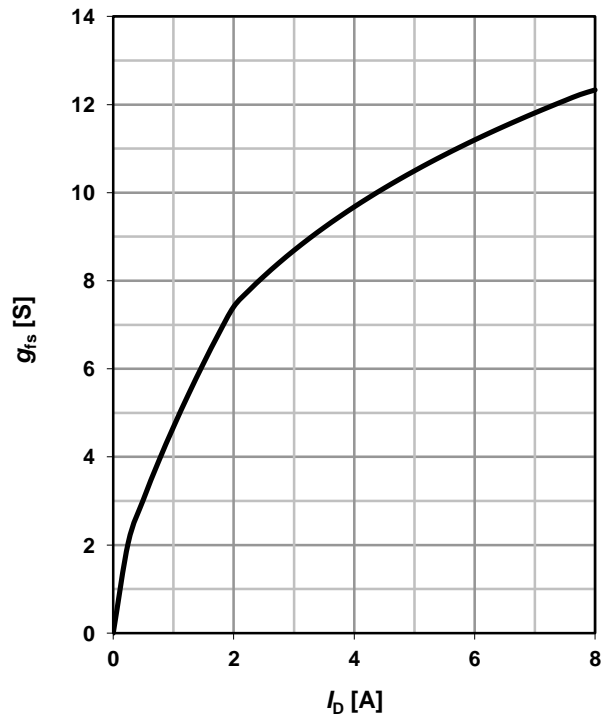
7 Typ. transfer characteristics

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$



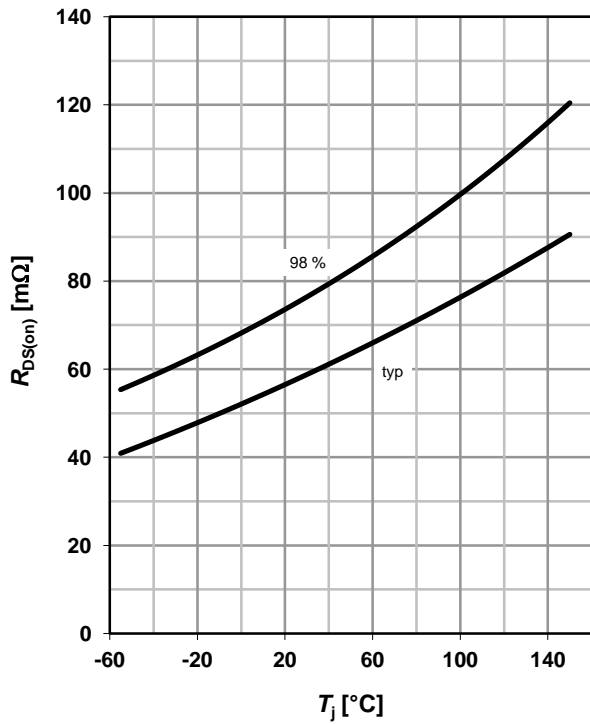
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

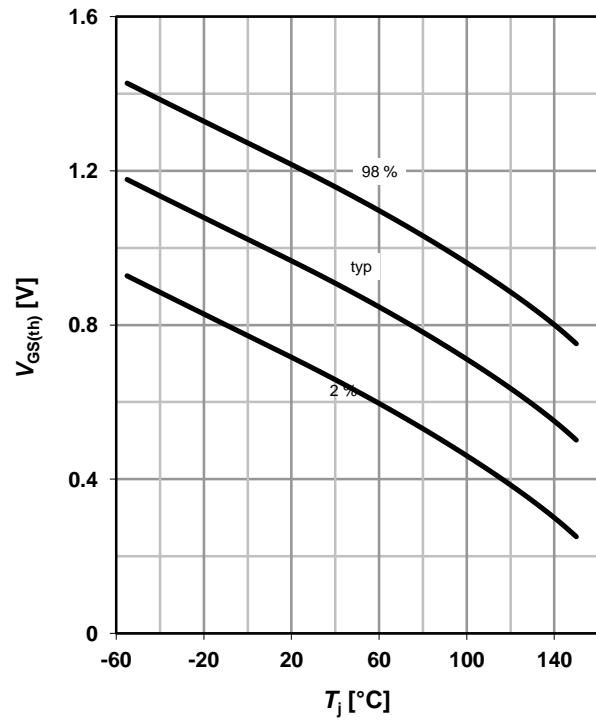
$R_{DS(on)}=f(T_j); I_D=2.1A; V_{GS}=4.5V$



10 Typ. gate threshold voltage

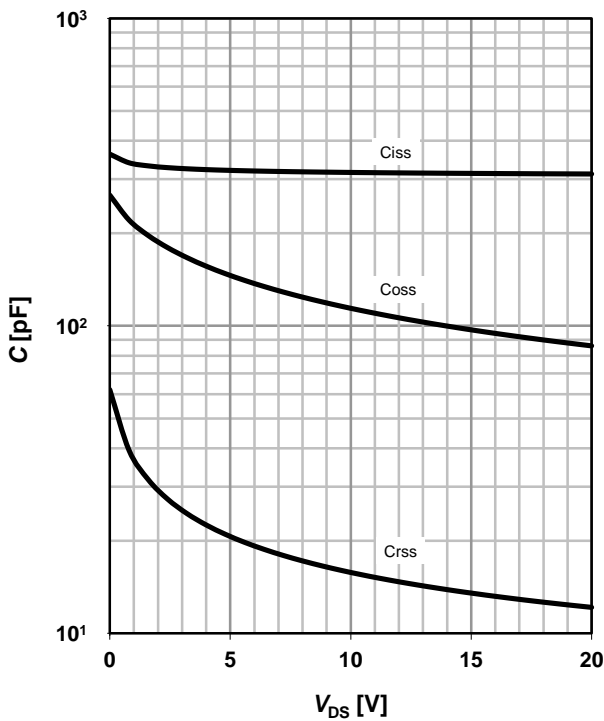
$V_{GS(th)}=f(T_j); V_{DS}=V_{GS}; I_D=11\mu A$

parameter: I_D



11 Typ. capacitances

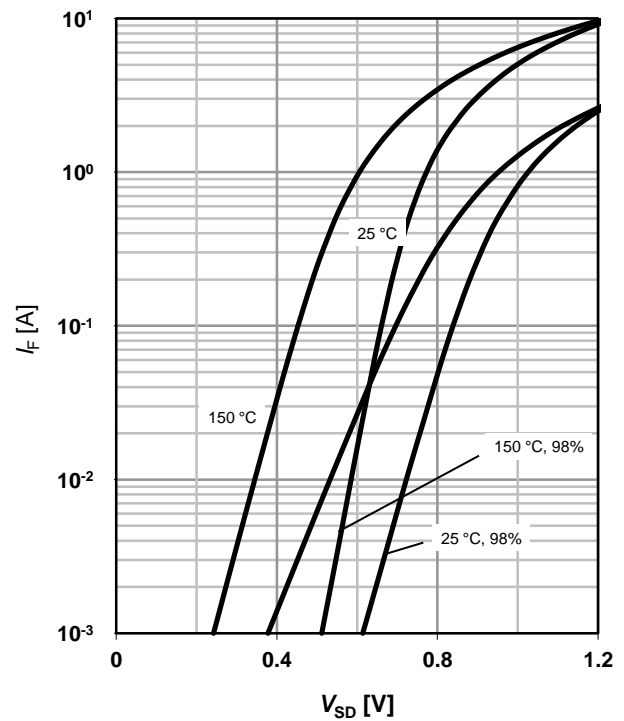
$C=f(V_{DS}); V_{GS}=0V; f=1MHz; T_j=25°C$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

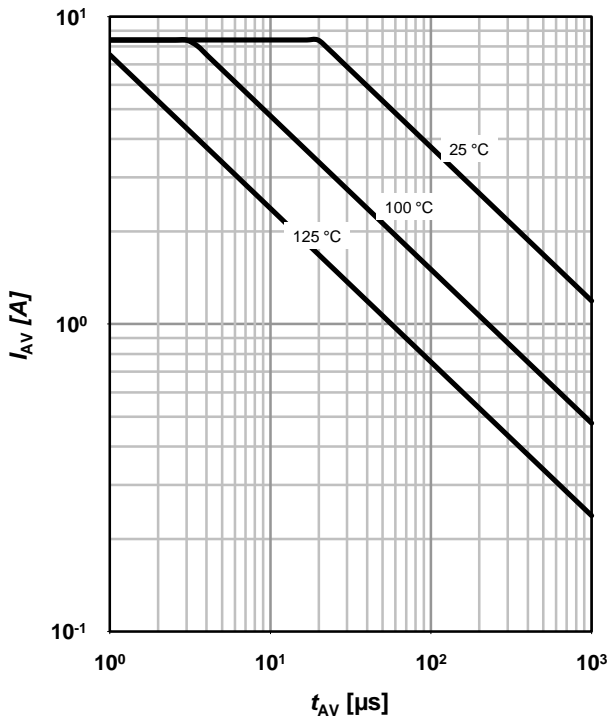
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

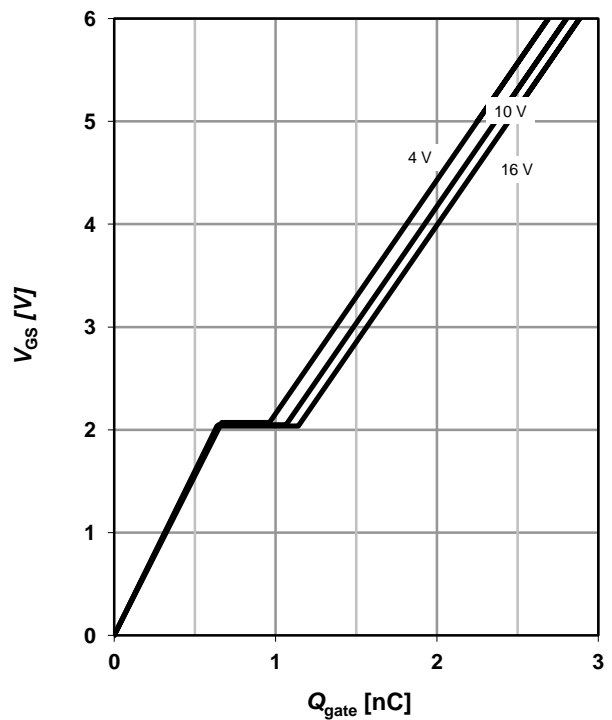
parameter: $T_{j(start)}$



14 Typ. gate charge

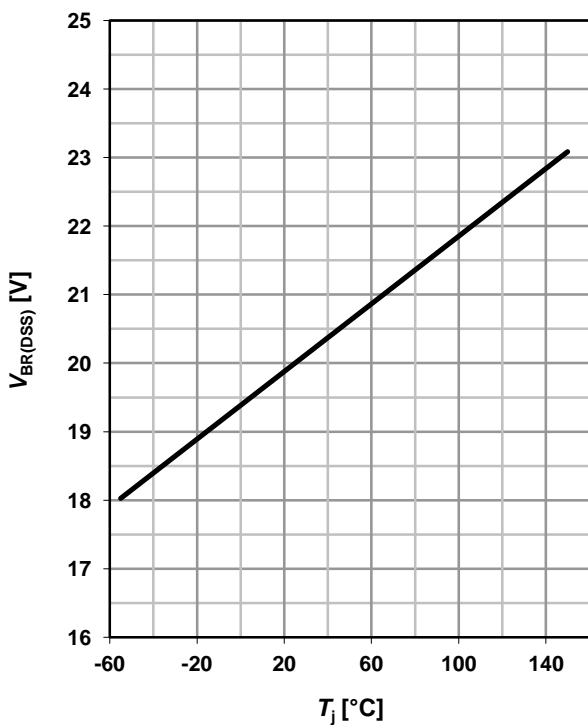
$V_{GS}=f(Q_{gate}); I_D=2.1A$ pulsed

parameter: V_{DD}



15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=250 \mu A$



16 Gate charge waveforms

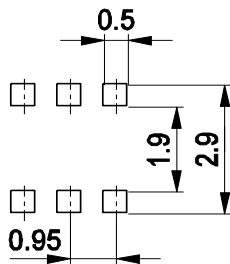


Package Outline:

TSOP6

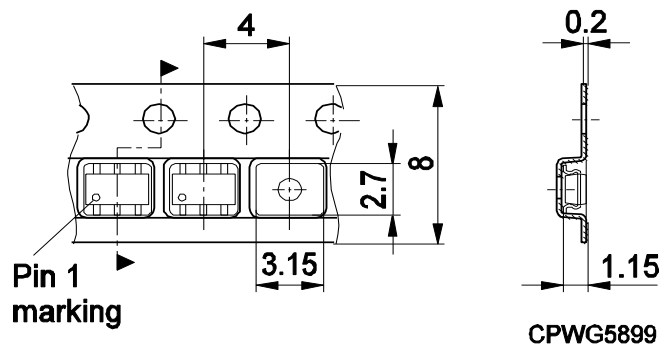


Footprint:



Remark: Wave soldering possible dep. on customers process conditions
HLG09283

Packaging:



Dimensions in mm

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