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February 2008

MM74HCT00 Quad 2 Input NAND Gate

Features

■ TTL, LS pin-out and threshold compatible

■ Fast switching: t_{PLH}, t_{PHL}=14ns (typ.)

■ Low power: 10µW at DC

■ High fan out, 10 LS-TTL loads

General Description

The MM74HCT00 is a NAND gates fabricated using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. This device is input and output characteristic and pin-out compatible with standard 74LS logic families. All inputs are protected from static discharge damage by internal diodes to $V_{\rm CC}$ and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Ordering InformationOrdering Information

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Order Number	Package Number		Package Description	
MM74HCT00M	M14A	14-Lead Smal	l Outline Integrated Circuit (SOIC), JEDEC MS-	-012, 0.150" Narrow
MM74HCT00SJ	M14D	14-Lead Smal	l Outline Package (SOP), EIAJ TYPE II, 5.3mm	Wide
MM74HCT00MTC	MTC14	14-Lead Thin	Shrink Small Outline Package (TSSOP), JEDE	C MO-153, 4.4mm Wide
MM74HCT00N	N14A	14-Lead Plast	ic Dual-In-Line Package (PDIP), JEDEC MS-00	1, 0.300" Wide

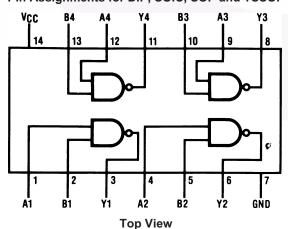
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

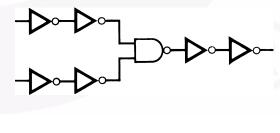
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Logic Diagram

(1 of 4 gates)



Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5 to +7.0V
V _{IN}	DC Input Voltage	–1.5 to V _{CC} +1.5V
V _{OUT}	DC Output Voltage	–0.5 to V _{CC} +0.5V
I _{IK} , I _{OK}	Clamp Diode Current	±20mA
I _{OUT}	DC Output Current, per pin	±25mA
I _{CC}	DC V _{CC} or GND Current, per pin	±50mA
T _{STG}	Storage Temperature Range	−65°C to +150°C
P _D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
TL	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

- 1. Unless otherwise specified all voltages are referenced to ground.
- 2. Power Dissipation temperature derating plastic "N" package: -12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Max.	Units
V _{CC}	Supply Voltage	4.5	5.5	V
V _{IN} , V _{OUT}	DC Input or Output Voltage		V _{CC}	V
T _A	Operating Temperature Range		+85	°C
t _r , t _f	Input Rise or Fall Times		500	ns

DC Electrical Characteristics

 $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

				= 25°C	T _A = -40°C to 85°C	T _A = -55°C to 125°C	
Symbol	Parameter	Conditions	Typ. G		uaranteed Limits		Units
V _{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V _{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} = 20\mu\text{A}$	V _{CC}	V _{CC} – 0.1	V _{CC} – 0.1	V _{CC} - 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} = 4.0\text{mA},$ $V_{CC} = 4.5\text{V}$	4.2	3.98	3.84	3.7	
		$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} = 4.8\text{mA},$ $V_{CC} = 5.5\text{V}$	5.2	4.98	4.84	4.7	
V _{OL}	Maximum LOW Level Voltage	$V_{IN} = V_{IH},$ $ I_{OUT} = 20 \mu A$	0	0.1	0.1	0.1	V
		$\begin{aligned} &V_{IN} = V_{IH}, \\ & I_{OUT} = 4.0 \text{mA}, \\ &V_{CC} = 4.5 \text{V} \end{aligned}$	0.2	0.26	0.33	0.4	
		$\begin{aligned} &V_{IN} = V_{IH}, \\ & I_{OUT} = 4.8 \text{mA}, \\ &V_{CC} = 5.5 \text{V} \end{aligned}$	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		±0.05	±0.5	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0 \mu A$		1.0	10	40	μA
		$V_{IN} = 2.4 \text{V or } 0.5 \text{V}^{(3)}$	0.18	0.3	0.4	0.5	mA

Note:

3. This is measured per input with all other inputs held at $\rm V_{\rm CC}$ or ground.

AC Electrical Characteristics

 V_{CC} = 5.0V, t_r = t_r = 6ns, C_L = 15pF, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Тур.	Guaranteed Limit	Units
t _{PLH} , t _{PHL}	Maximum Propagation Delay		14	18	ns

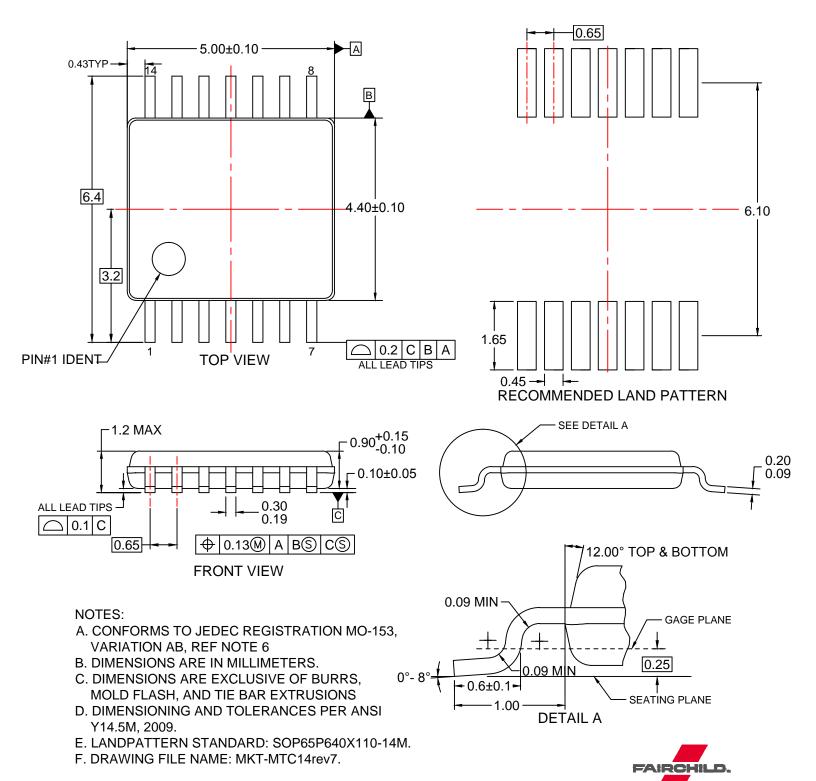
AC Electrical Characteristics

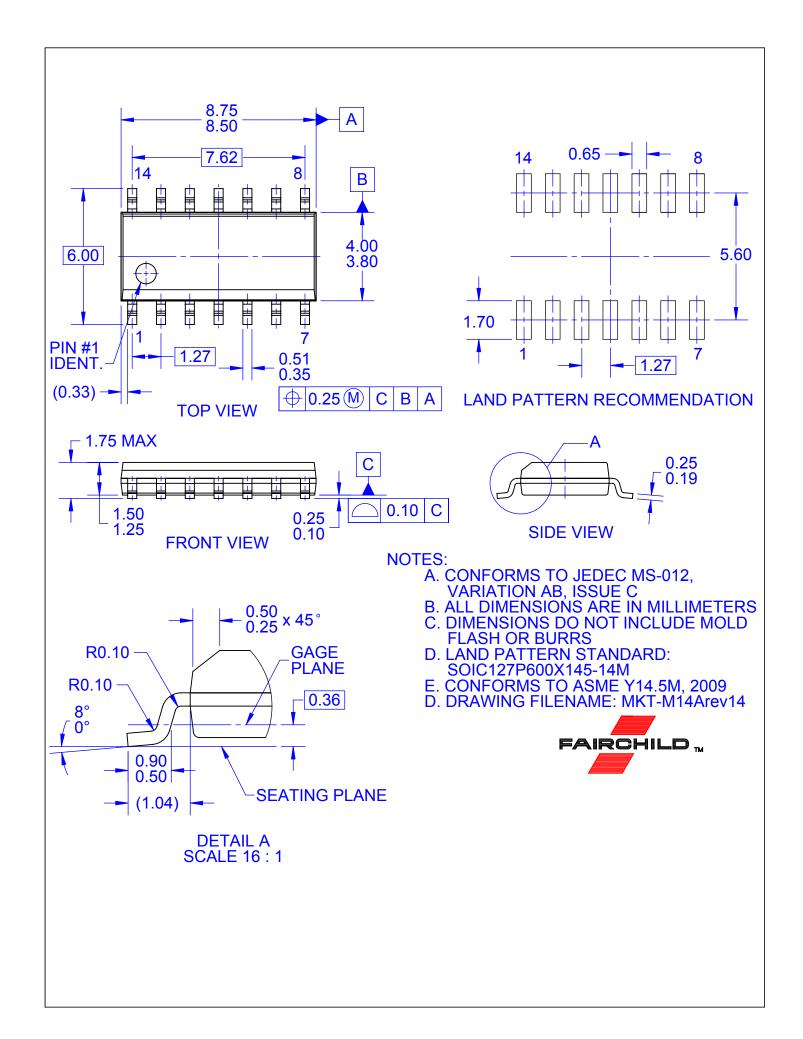
 V_{CC} = 5.0V ±10%, t_r = t_f = 6ns, C_L = 50pF (unless otherwise noted)

			T _A =	25°C	T _A = -40°C to 85°C	T _A = -55°C to 125°C	
Symbol	Parameter	Conditions	Тур.		Guaranteed Limits		Units
t _{PLH} , t _{PHL}	Maximum Propagation Delay		18	23	29	35	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C _{PD}	Power Dissipation Capacitance	(4)	30				pF
C _{IN}	Input Capacitance		5	10	10	10	pF

Note

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$.





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