ATA663211

LIN Transceiver

DATASHEET

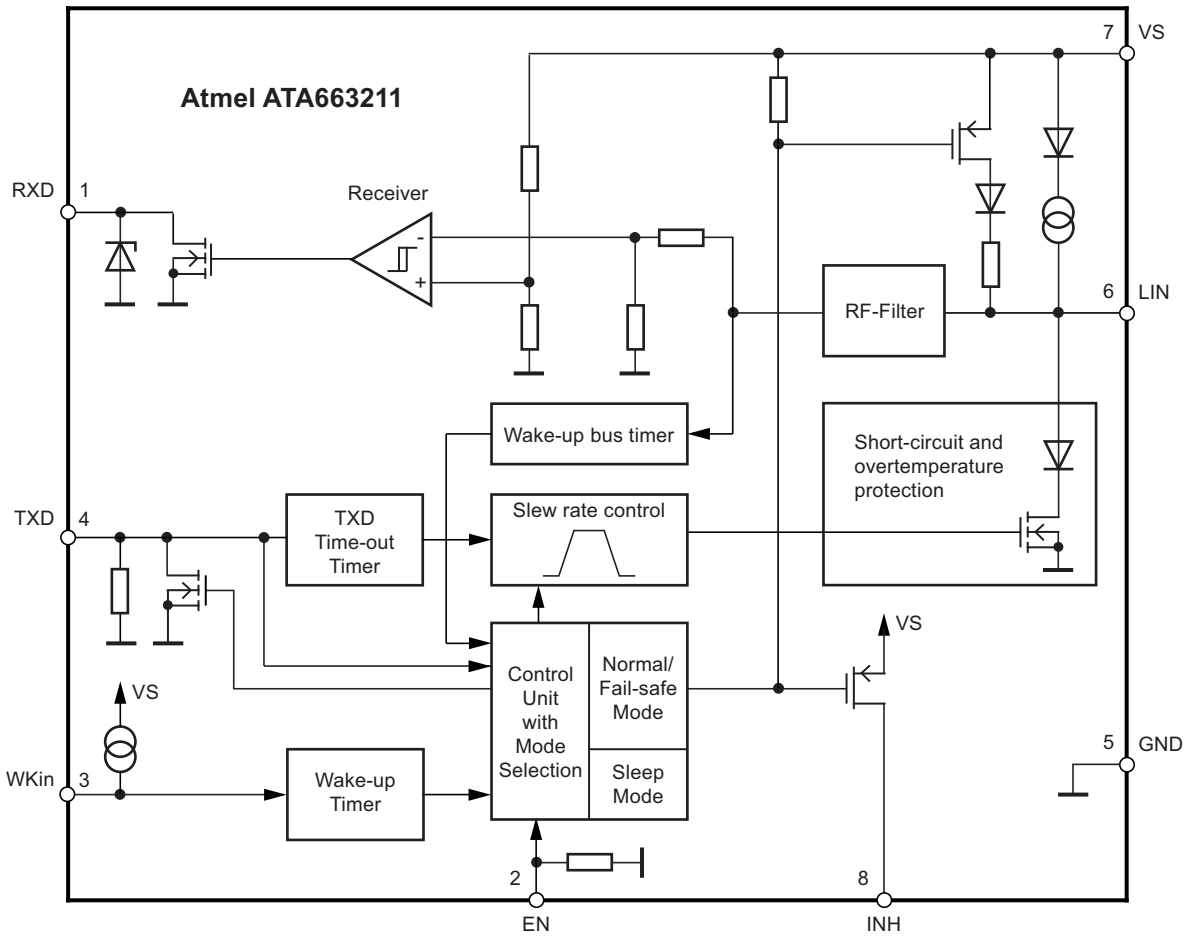
Features

- Supply voltage up to 40V
- Operating voltage V_S = 5V to 28V
- Very low supply current
  - Sleep mode: typically 9µA
  - Fail-safe mode: typically 80µA
  - Normal mode: typically 250µA
- Fully compatible with 3.3V and 5V devices
- LIN physical layer according to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Wake-up capability via LIN bus (100µs dominant)
- External wake-up via WKin pin (100µs low level)
- INH output to control an external voltage regulator or to switch the master pull-up
- Wake-up source recognition
- TXD time-out timer
- Bus pin is over-temperature and short-circuit protected vs. GND and battery
- Advanced EMC and ESD performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.3”
- Interference and damage protection according to ISO7637
- Qualified according to AEC-Q100
- Package: SO8, DFN8 with wettable flanks (Moisture Sensitivity Level 1)

1. Description

The Atmel® ATA663211 is a fully integrated LIN transceiver designed in compliance with the LIN specification 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN bus ensures data communication up to 20Kbaud. Sleep mode guarantees minimal current consumption even in the case of a floating bus line or a short circuit on the LIN bus to GND.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning DFN8 and SO8

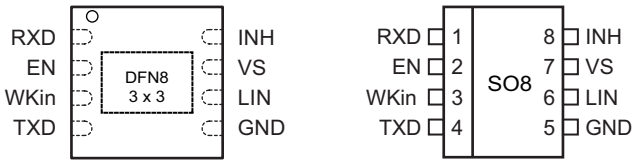


Table 2-1. Pin Description

Pin	Symbol	Function
1	RXD	Receive data output
2	EN	Enables normal mode if the input is high
3	WKin	High voltage input for local wake-up request. If not needed, connect directly to VS
4	TXD	Transmit data input
5	GND	Ground, heat slug
6	LIN	LIN bus line input/output
7	VS	Supply voltage
8	INH	Battery-related high-side switch output for controlling an external voltage regulator or to switch off the LIN master pull-up resistor; switched on after a wake-up request
Backside		Heat slug, internally connected to the GND pin

3. Pin Description

3.1 Supply Pin (VS)

LIN operating voltage is V_S = 5V to 28V. Undervoltage detection is implemented to disable transmission if V_S falls below typ. 4.5V, thereby avoiding false bus messages. After switching on V_S, the IC starts in fail-safe mode and the INH output is switched on.

The supply current in sleep mode is typically 9µA.

3.2 Ground Pin (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It is able to handle a ground shift of up to 11.5% of V_S.

3.3 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the event of a GND shift or V_{Bat} disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope-controlled.

During a short circuit at LIN to V_{Bat}, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high.

During a short circuit from LIN to GND the IC can be switched into sleep mode and even in this case the current consumption is lower than 100µA. If the short-circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2µA at pin LIN during loss of V_{Bat}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

3.4 Input/Output (TXD)

In normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high, the LIN output transistor is turned off and the bus is in the recessive state. If the TXD pin stays at GND level while switching into normal mode, it must be pulled to high level longer than 10µs before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to dominant state after normal mode has been activated (also in case of a short circuit at TXD to GND). During fail-safe mode, this pin is used as output and signals the fail-safe source.

The TXD pin provides a pull-down resistor in order to have a defined level if TXD is disconnected.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{dom} > 20ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (>10µs).

3.5 Output Pin (RXD)

In normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD; LIN low (dominant state) is indicated by a low level at RXD.

The output is an open drain; therefore, it is compatible with a 3.3V or 5V power supply. The AC characteristics are defined by an external pull-up resistor of 4.7kOhm to 5V and a load capacitor of 20pF.

In unpowered mode, RXD is switched off.

3.6 Enable Input Pin (EN)

The enable input pin controls the operating mode of the device. If EN is high, the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active.

If EN is switched to low while TXD is still high, the device is forced to sleep mode. No data transmission is then possible, and current consumption is reduced to $I_{VSsleep}$ typ. 9µA.

The EN pin provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.

3.7 Inhibit Output Pin (INH)

This pin is used to control an external voltage regulator or to switch the LIN master pull-up resistor ON/OFF in case the device is used in a master node. The inhibit pin provides an internal switch toward the VS pin which is protected by temperature monitoring. If the device is in normal or fail-safe mode, the inhibit high-side switch is turned on. When the device is in sleep mode, the inhibit switch is turned off, thus disabling the voltage regulator or other connected external devices.

A wake-up event on the LIN bus or at the WKin pin switches the INH pin to the VS level. After a system power-up (VS rises from zero), the INH pin switches to the VS level automatically.

3.8 WKin Pin

This pin is a high-voltage input used for waking up the device from sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10µA is implemented. The voltage threshold for a wake-up signal is typically 2V below the VS voltage.

If a local wake up is not needed in the application, the WKin pin can be connected directly to the VS pin.

4. Functional Description

4.1 Physical Layer Compatibility

Because the LIN physical layer is independent of higher LIN layers (e.g., LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes based on earlier versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

4.2 Operating Modes

Figure 4-1. Operating Modes

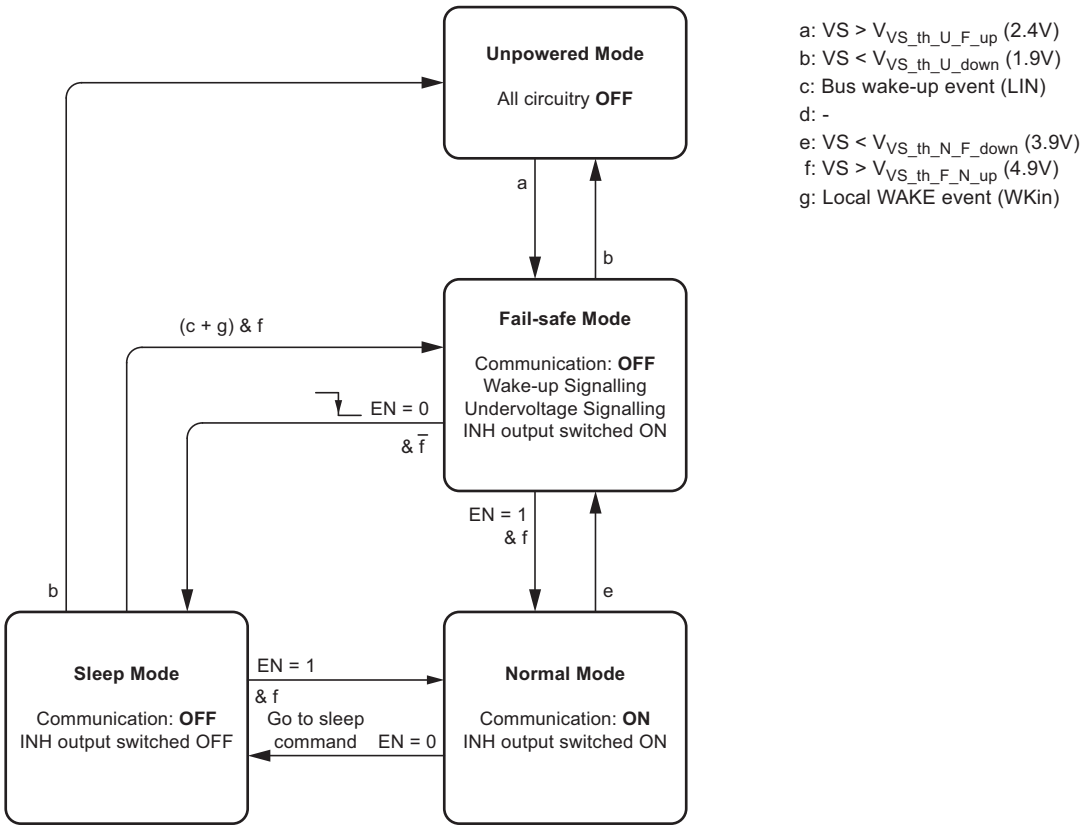


Table 4-1. Operating Modes

Operating Mode	Transceiver	INH	LIN	TXD	RXD
Fail-safe	OFF	ON, except VS < $V_{VS_th_N_F_down}$	Recessive	Signaling fail-safe sources (see Table 4-2)	
Normal	ON	ON	TXD-dependent	Follows data transmission	
Sleep/Unpowered	OFF	OFF	Recessive	High	High
				Low	Low

4.2.1 Normal Mode

This is the normal transmitting and receiving mode of the LIN Interface, in accordance with LIN specification 2.x.

4.2.2 Sleep Mode

A falling edge at EN switches the IC into sleep mode. In sleep mode the transmission path is disabled and the device is in low-power mode. Supply current from VBat is typically 9µA. In sleep mode the INH pin is switched off. The internal termination between the LIN pin and VS pin is disabled. Only a weak pull-up current (typical 10µA) between the LIN pin and VS pin is present. Sleep mode can be activated independently from the actual level on the LIN or WKin pin.

If the TXD pin is short-circuited to GND, it is possible to switch to sleep mode via EN after $t > t_{dom}$.

4.2.3 Fail-Safe Mode

The device automatically switches to fail-safe mode at system power-up or after a wake-up event. The INH output is switched on and the LIN transceiver is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to normal mode. During fail-safe mode the TXD pin is an output and, together with the RXD output pin, signals the fail-safe source.

If the device enters fail-safe mode coming from the normal mode (EN=1) due to an V_S undervoltage condition ($V_S < V_{VS_th_N_F_down}$), it is possible to switch into sleep mode by a falling edge at the EN input. With this feature the current consumption can be further reduced.

A wake-up event from sleep mode is signalled to the microcontroller using the RXD pin and the TXD pin. A V_S undervoltage condition is also signalled at these two pins. The coding is shown in the table below.

Table 4-2. Signaling in Fail-safe Mode

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
VS_{th} (battery) undervoltage detection (VS < 3.9V)	High	Low

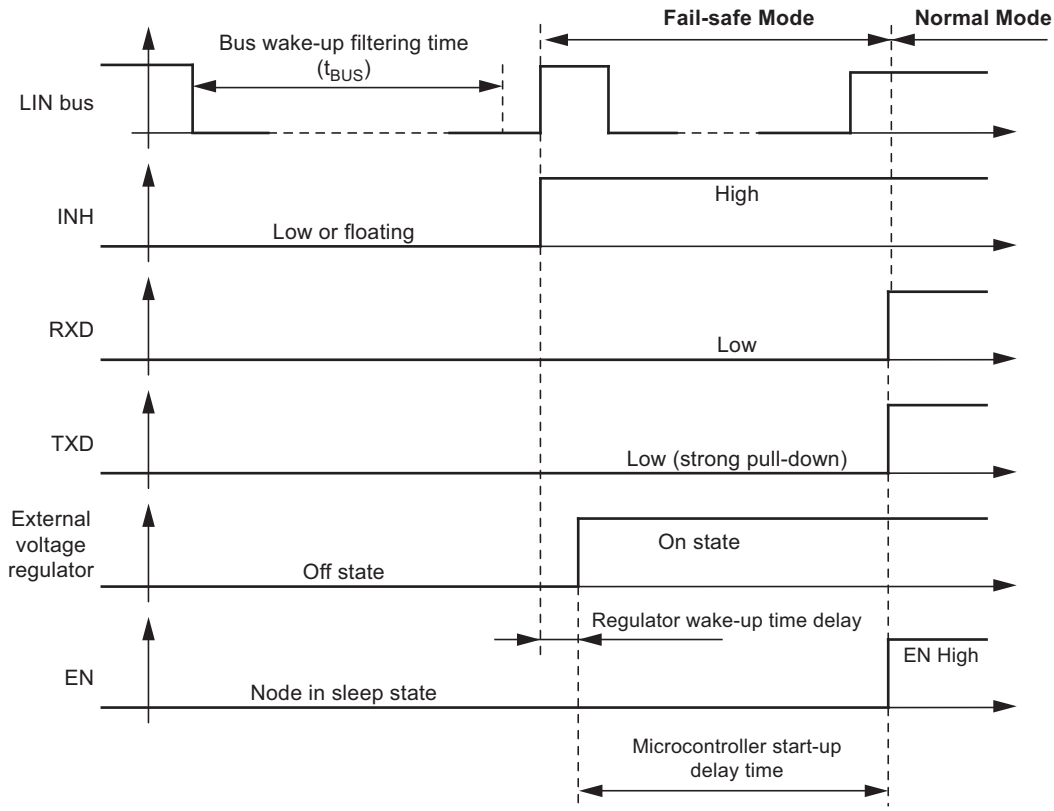
4.3 Wake-up Scenarios from Sleep Mode

4.3.1 Remote Wake-up via LIN Bus

4.3.1.1 Remote Wake-up from Sleep Mode

A voltage lower than the LIN pre-wake detection VLINL at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin, followed by a dominant bus level maintained for a certain period of time (> t_{BUS}) and following a rising edge at the LIN pin result in a remote wake-up request and the device switches to fail-safe mode. The INH pin is activated (switches to VS) and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD and interrupts the microcontroller.

Figure 4-2. LIN Wake-up from Sleep Mode

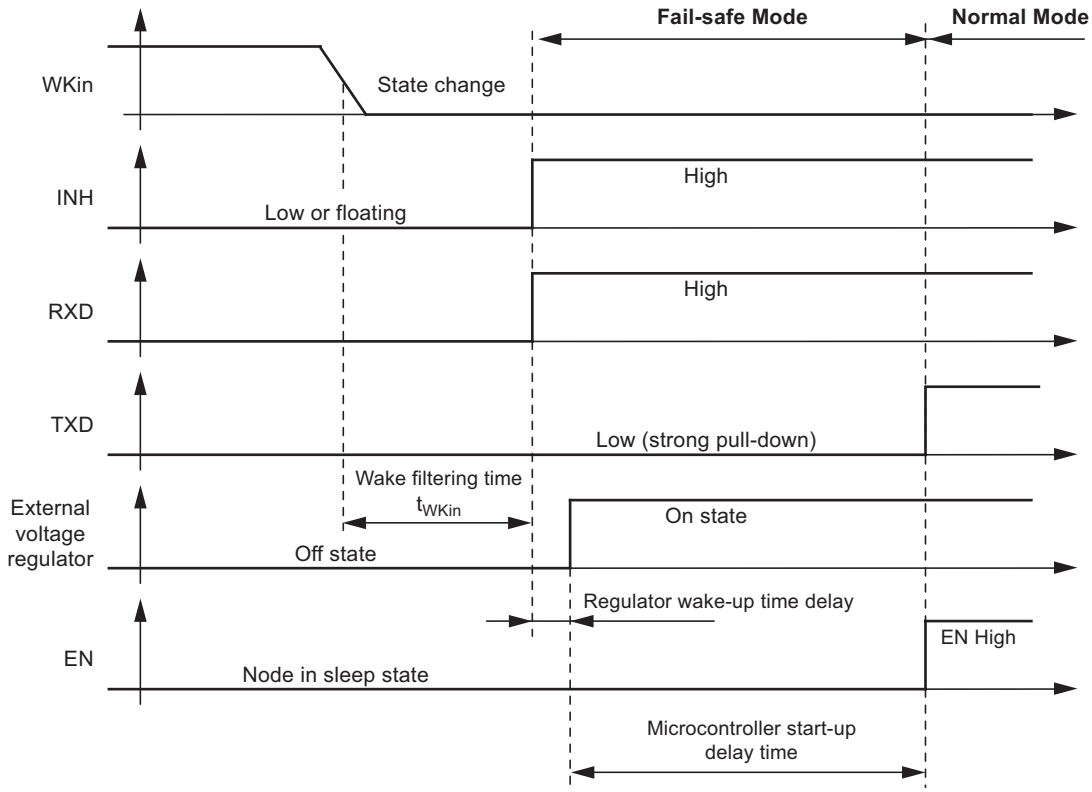


4.3.2 Local Wake-up via WKin Pin

A falling edge at the WKin pin followed by a low level maintained for a certain period of time (> t_{WKin}) result in a local wake-up request and the device switches to fail-safe mode. The INH pin is activated (switches to Vs) and the internal slave termination resistor is switched on.

The local wake-up request is indicated by a low level at the TXD pin and a high level at the RXD pin, generating an interrupt for the microcontroller. Even when the WKin pin is low, it is possible to switch to sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high > 10µs before the negative edge at WKin starts a new local wake-up request.

Figure 4-3. Local Wake-up from Wake-up Switch



4.3.3 Wake-up Source Recognition

The device can distinguish between different wake-up sources. The wake-up source can be read on the TXD and RXD pin in fail-safe mode. These flags are immediately reset if the microcontroller sets the EN pin to high and the IC is in normal mode.

Table 4-3. Signaling in Fail-safe Mode

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
VS_{th} (battery) undervoltage detection (VS < 3.9V)	High	Low

4.4 Behavior under Low Supply Voltage Condition

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor used in the application (see Fig. 5-1 on page 15). If V_{VS} is higher than the minimum VS operation threshold $V_{VS_th_U_F_up}$, the IC mode changes from unpowered mode to fail-safe mode, the INH output is switched on and the LIN transceiver can be activated.

If during **sleep mode** the voltage level of V_{VS} drops below the undervoltage detection threshold $V_{VS_th_N_F_down}$ (typ. 4.3V), the operation mode is not changed and no wake-up is possible. Only if the supply voltage on pin VS drops below the VS operation threshold $V_{VS_th_U_down}$ (typ. 2.05V), does the IC switch to unpowered mode.

If during **normal mode** the voltage level on the VS pin drops below the VS undervoltage detection threshold $V_{VS_th_N_F_down}$ (typ. 4.3V), the IC switches to fail-safe mode. This means the LIN transceiver is disabled in order to avoid malfunctions or false bus messages. If the supply voltage VS drops further below the VS operation threshold $V_{VS_th_U_down}$ (typ. 2.05V), the IC switches to unpowered mode and the INH output switches off.

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Logic pins voltage levels (RxD, TxD, EN, NRES)		–0.3		+5.5	V
Logic output DC currents	I_{Logic}	–5		+5	mA
LIN - DC voltage - Pulse time < 500ms		–27		+40 +43.5	V V
INH -DC voltage	INH	–0.3		Vs + 0,3	V
WKin voltage levels - DC voltage -Transient voltage according to ISO7637 (coupling 1nF), (with 2.7K serial resistor)	V_{WKin}	–0.3 –150		+40 +100	V
ESD according to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND, WKin (with ext. circuitry acc. applications diagram)		±6			KV
ESD HBM following STM5.1 with 1.5kΩ/100pF - Pin VS, LIN, INH to GND - Pin WKin to GND		±6 ±5			KV KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			KV
CDM ESD STM 5.3.1		±750			V
Machine Model ESD AEC-Q100-RevF(003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

6. Thermal Characteristics DFN8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thjC}		10		K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to JEDEC	R_{thja}		50		K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

7. Thermal Characteristics SO8

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction ambient	R_{thJA}			145	K/W
Special heat sink at GND (pin 5) on PCB (fused lead frame to pin 5)	R_{thJA}		80		K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	5	10	20	°C

8. Electrical Characteristics

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	VS pin								
1.1	Nominal DC voltage range		VS	V_S	5	13.5	28	V	A
1.3	Supply current in sleep mode	Sleep mode $V_{LIN} > V_S – 0.5V$ V_S < 14V, T = 27°C	VS	$I_{VSsleep}$	3	9	15	µA	B
		Sleep mode $V_{LIN} > V_S – 0.5V$ V_S < 14V	VS	$I_{VSsleep}$	3	11	18	µA	A
		Sleep mode, V_{LIN} = 0V bus shorted to GND V_S < 14V	VS	$I_{VSsleep_short}$	20	50	100	µA	A
1.4	Supply current in normal mode	Bus recessive V_S < 14V	VS	I_{VSrec}	150	250	320	µA	A
1.5	Supply current in normal mode	Bus dominant (internal LIN pull-up resistor active) V_S < 14V	VS	I_{VSdom}	200	700	950	µA	A
1.6	Supply current in fail-safe mode	Bus recessive V_S < 14V	VS	I_{VSfail}	40	80	110	µA	A
1.7	VS undervoltage threshold (switching from normal to fail-safe mode)	Decreasing supply voltage	VS	$V_{VS_th_N_F_down}$	3.9	4.3	4.7	V	A
		Increasing supply voltage	VS	$V_{VS_th_F_N_up}$	4.1	4.6	4.9	V	A
1.8	VS undervoltage hysteresis		VS	$V_{VS_hys_F_N}$	0.1	0.25	0.4	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.9	VS operation threshold (switching to unpowered mode)	Switch to unpowered mode	VS	$V_{VS_th_U_down}$	1.9	2.05	2.3	V	A
		Switch from unpowered to fail-safe mode	VS	$V_{VS_th_U_F_up}$	2.0	2.25	2.4	V	A
1.10	VS undervoltage hysteresis		VS	$V_{VS_hys_U}$	0.1	0.2	0.3	V	A
2	RXD output pin (open drain)								
2.1	Low-level output sink capability	Normal mode, V_{LIN} = 0V, I_{RXD} = 2mA	RXD	V_{RXDL}		0.2	0.4	V	A
2.3	High-level leakage current	Normal mode V_{LIN} = V_S, V_{RXD} = 5V	RXD	I_{RXDH}	-3		+3	µA	A
3	TXD input/output pin								
3.1	Low-level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		TXD	V_{TXDH}	2		5.5	V	A
3.5	Pull-down resistor	V_{TXD} = 5V	TXD	R_{TXD}	150	200	300	kΩ	A
3.6	Low-level leakage current	V_{TXD} = 0V	TXD	I_{TXD}	–3		+3	µA	A
3.7	Low-level output sink current at wake-up request	Fail-safe Mode V_{TXD} = 0.4V	TXD	I_{TXD}	2	2.5	8	mA	A
4	EN input pin								
4.1	Low-level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		EN	V_{ENH}	2		5.5	V	A
4.3	Pull-down resistor	V_{EN} = 5V	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
6	WKin input pin								
6.1	High-level input voltage		WKin	V_{WKinH}	VS – 1V		VS + 0.3V	V	A
6.2	Low-level input voltage	Initializes a wake-up signal	WKin	V_{WKinL}	–1		VS – 3.3V	V	A
6.3	WKin pull-up current	VS < 28V, V_{WKin} = 0V	WKin	I_{WKin}	–30	–10		µA	A
6.4	High-level leakage current	VS = 28V, V_{WKin} = 28V	WKin	I_{WKinL}	–5		+5	µA	A
6.5	Debounce time of low pulse for wake-up via WKin	V_{WKin} = 0V	WKin	t_{WKin}	50	100	150	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	INH output pin								
7.1	Switch on resistance between VS and INH	Normal or fail-safe mode	INH	$R_{DSon,INH}$		12	25	Ω	A
7.2	Leakage current	Transceiver in sleep mode, VINH = 0V/28V, VS = 28V	INH	$I_{leak,INH}$	–3		+3	µA	A
7.3	High-level voltage	Normal or fail-safe mode IINH = –15mA	INH	VINH	V_S – 0.75		V_S	V	A
10	LIN bus driver: bus load conditions: Load 1 (small): 1nF, 1kΩ; Load 2 (large): 10nF, 500Ω; External Pull-up R_{RXD} = 4.7kΩ ; C_{RXD} = 20pF, Load 3 (medium): 6.8nF, 660Ω characterized on samples 12.7 and 12.8 specifies the timing parameters for proper operation at 20kb/s and 12.9 and 12.10 at 10.4kb/s								
10.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	A
10.2	Driver dominant voltage	V_{VS} = 7V R_{load} = 500Ω	LIN	$V_{_LoSUP}$			1.2	V	A
10.3	Driver dominant voltage	V_{VS} = 18V R_{load} = 500Ω	LIN	$V_{_HiSUP}$			2	V	A
10.4	Driver dominant voltage	V_{VS} = 7V R_{load} = 1000Ω	LIN	$V_{_LoSUP_1k}$	0.6			V	A
10.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000Ω	LIN	$V_{_HiSUP_1k}$	0.8			V	A
10.6	Pull-up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	47	kΩ	A
10.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
10.8	LIN current limitation V_{BUS} = V_{Bat_max}		LIN	I_{BUS_LIM}	40	120	200	mA	A
10.9	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current driver off V_{BUS} = 0V V_{Bat} = 12V	LIN	$I_{BUS_PAS_dom}$	–1	–0.35		mA	A
10.10	Leakage current LIN recessive	Driver off 8V < V_{Bat} < 18V 8V < V_{BUS} < 18V V_{BUS} ≥ V_{Bat}	LIN	$I_{BUS_PAS_rec}$		10	20	µA	A
10.11	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	GND_{Device} = V_S V_{Bat} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS_NO_gnd}$	–10	+0.5	+10	µA	A
10.12	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{Bat} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS_NO_bat}$		0.1	2	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.13	Capacitance on pin LIN to GND		LIN	C_{LIN}			20	pF	D
11	LIN bus receiver								
11.1	Center of receiver threshold	V_{BUS_CNT} = $(V_{th_dom} + V_{th_rec})/2$	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
11.2	Receiver dominant state	V_{EN} = 5V	LIN	V_{BUSdom}	–27		0.4 × V_S	V	A
11.3	Receiver recessive state	V_{EN} = 5V	LIN	V_{BUSrec}	0.6 × V_S		40	V	A
11.4	Receiver input hysteresis	$V_{hys} = V_{th_rec} – V_{th_dom}$	LIN	V_{BUShys}	0.028 × V_S	0.1 x V_S	0.175 × V_S	V	A
11.5	Pre-wake detection LIN high-level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
11.6	Pre-wake detection LIN low-level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_S – 3.3V	V	A
12	Internal timers								
12.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	50	100	150	µs	A
12.2	Time delay for mode change from fail-safe into normal mode via EN pin	V_{EN} = 5V	EN	t_{norm}	5	15	20	µs	A
12.3	Time delay for mode change from normal mode to sleep mode via EN pin	V_{EN} = 0V	EN	t_{sleep}	5	15	20	µs	A
12.4	Time delay for mode change from sleep mode to normal mode via EN pin	V_{EN} = 5V	EN	t_{s_norm}		150	300	µs	A
12.5	TXD dominant time-out time	V_{TXD} = 0V	TXD	t_{dom}	20	40	60	ms	A
12.7	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_S $TH_{Dom(max)}$ = 0.581 × V_S V_S = 7.0V to 18V t_{Bit} = 50µs D1 = $t_{bus_rec(min)}/(2 \times t_{Bit})$	LIN	D1	0.396				A
12.8	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × V_S $TH_{Dom(min)}$ = 0.284 × V_S V_S = 7.6V to 18V t_{Bit} = 50µs D2 = $t_{bus_rec(max)}/(2 \times t_{Bit})$	LIN	D2			0.581		A
12.9	Duty cycle 3	$TH_{Rec(max)}$ = 0.778 × V_S $TH_{Dom(max)}$ = 0.616 × V_S V_S = 7.0V to 18V t_{Bit} = 96µs D3 = $t_{bus_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
12.10	Duty cycle 4	$TH_{Rec(min)}$ = 0.389 × V_S $TH_{Dom(min)}$ = 0.251 × V_S V_S = 7.6V to 18V t_{Bit} = 96µs D4 = $t_{bus_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

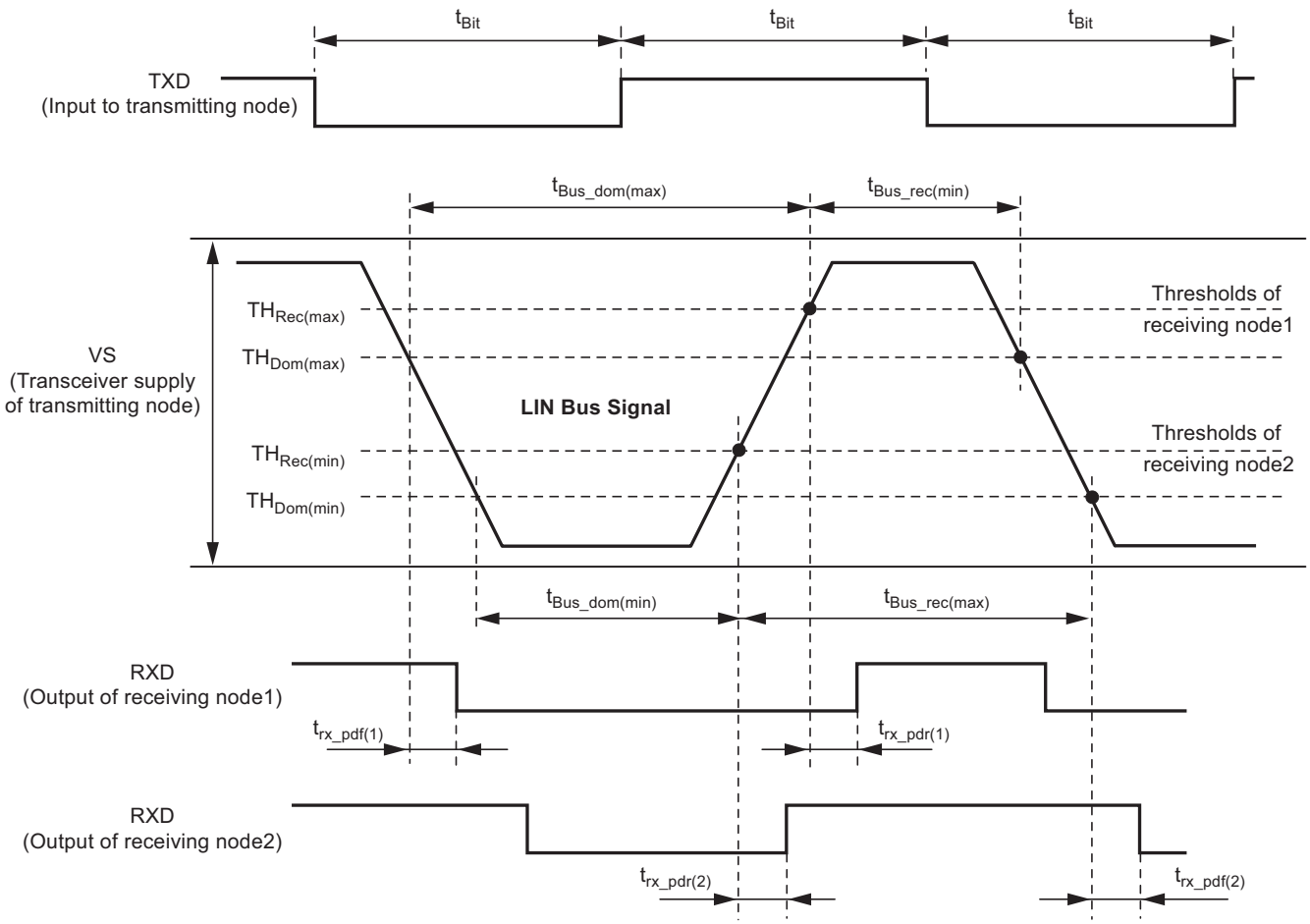
8. Electrical Characteristics (Continued)

5V < V_S < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
12.11	Slope time falling and rising edge at LIN	V_S = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
13	Receiver electrical AC parameters of the LIN physical layer LIN receiver, RXD load conditions: C_{RXD} = 20pF, R_{RXD} = 4.7kΩ								
13.1	Propagation delay of receiver	V_S = 7.0V to 18V t_{rx_pd} = max(t_{rx_pdr} , t_{rx_pdf})	RXD	t_{rx_pd}			6	µs	A
13.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}	RXD	t_{rx_sym}	–2		+2	µs	A

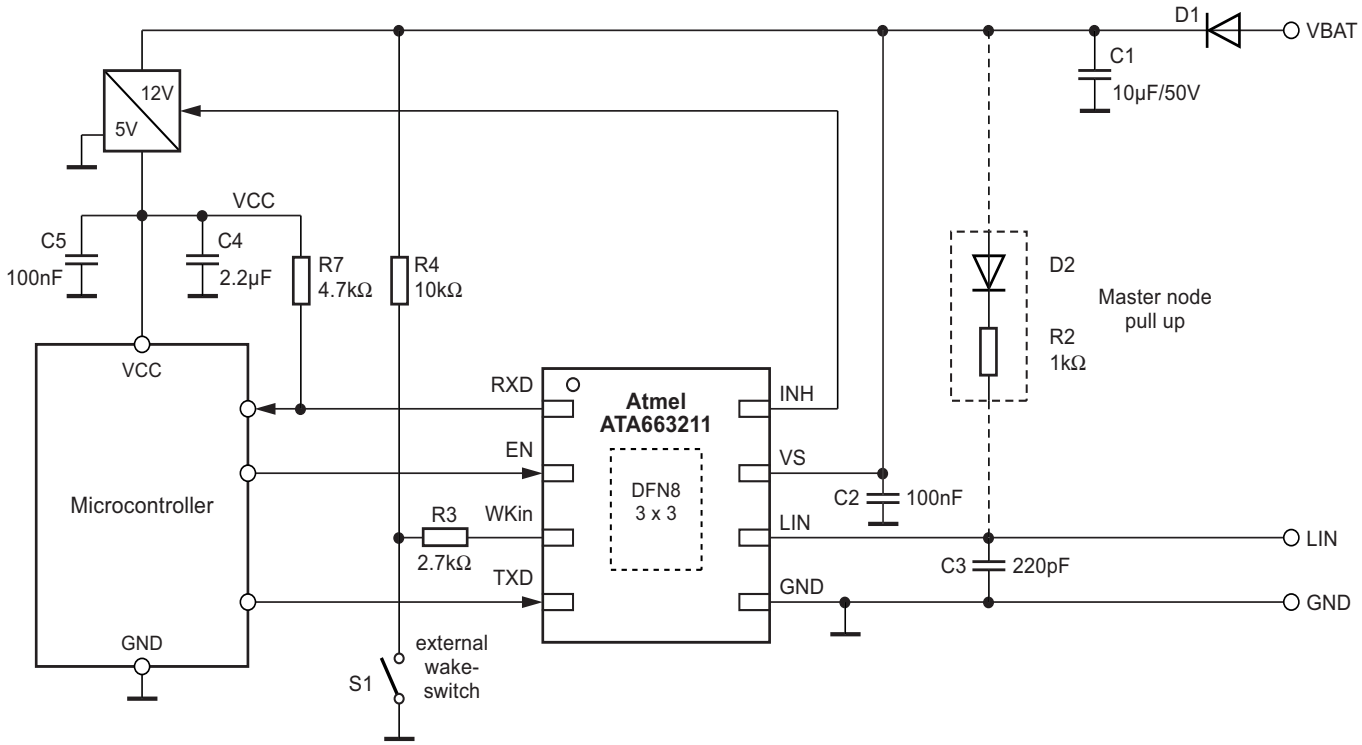
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 8-1. Definition of Bus Timing Characteristics



9. Application Circuits

Figure 9-1. Typical Application Circuit



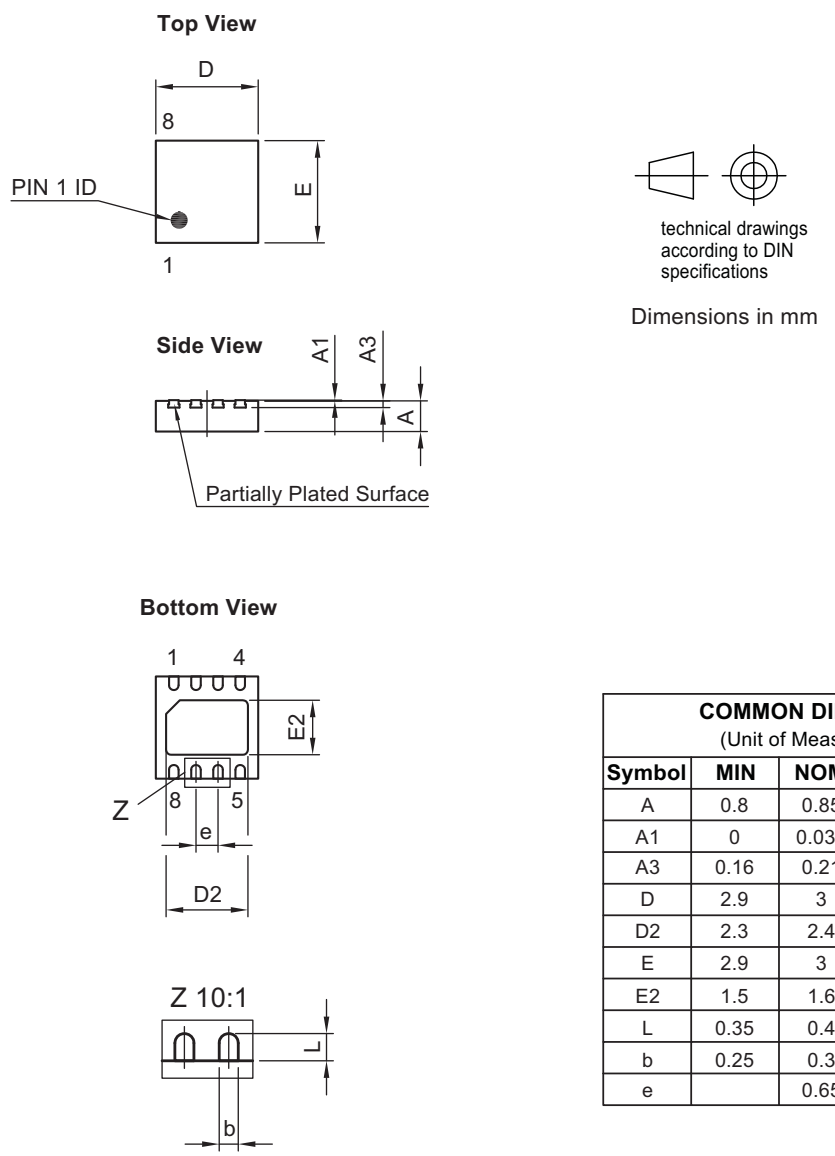
Note: Heat slug must always be connected to GND.

10. Ordering Information

Extended Type Number	Package	Remarks
ATA663211-GBQW	DFN8	LIN transceiver, Pb-free, 6k, taped and reeled
ATA663211-GAQW	SO8	LIN transceiver, Pb-free, 4k, taped and reeled

11. Package Information

Figure 11-1. DFN8

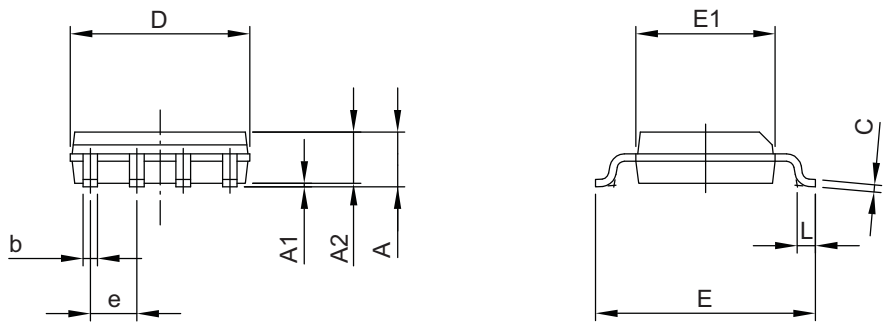


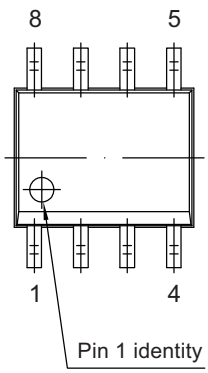
COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	MIN	NOM	MAX	NOTE
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	2.9	3	3.1	
D2	2.3	2.4	2.5	
E	2.9	3	3.1	
E2	1.5	1.6	1.7	
L	0.35	0.4	0.45	
b	0.25	0.3	0.35	
e		0.65		

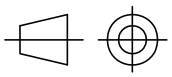
10/11/13

	TITLE	GPC	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	Package: VDFN_3x3_8L Exposed pad 2.4x1.6		6.543-5165.03-4	1

Figure 11-2. SO8







technical drawings
according to DIN
specifications

Dimensions in mm

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	1.5	1.65	1.8	
A1	0.1	0.15	0.25	
A2	1.4	1.47	1.55	
D	4.8	4.9	5	
E	5.8	6	6.2	
E1	3.8	3.9	4	
L	0.4	0.65	0.9	
C	0.15	0.2	0.25	
b	0.3	0.4	0.5	
e		1.27 BSC		

05/08/14

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**Package: SO8**		6.543-5185.01-4	1

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9359C-AUTO-10/14	• SO8 package added • Number 3.5 in Section 8 “Electrical Characteristics” on page 13 update • Section 10 “Ordering Information” on page 18 updated

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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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