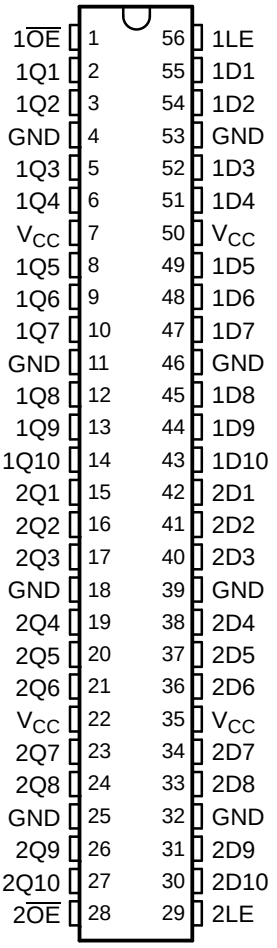
# SN74ALVCH16841
# 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES043E–JULY 1995–REVISED SEPTEMBER 2004

## FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

This 20-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{OE}$ does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16841 is characterized for operation from -40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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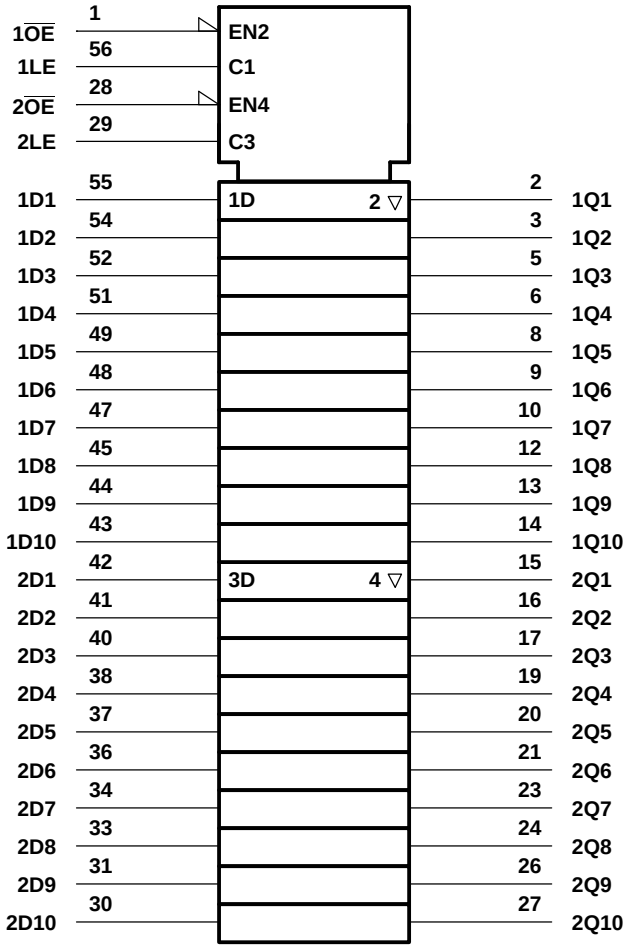
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## FUNCTION TABLE
## (each 10-bit latch)

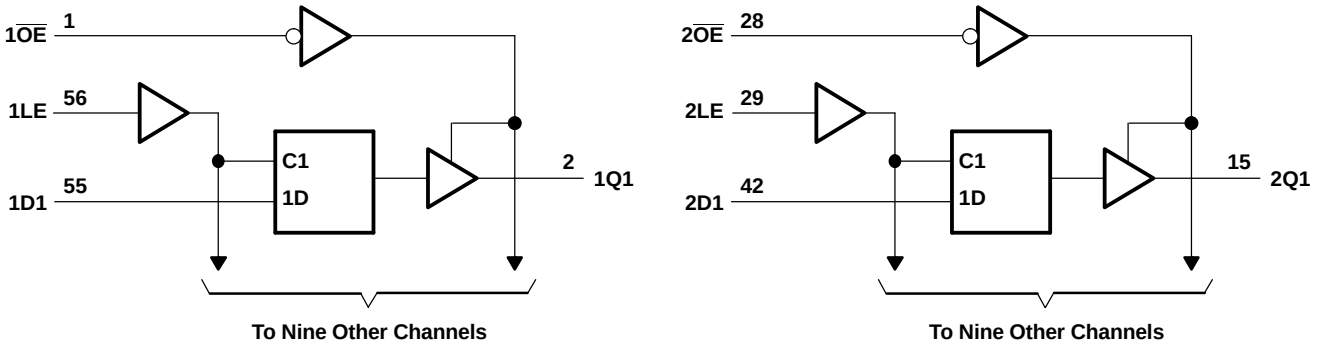
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## LOGIC SYMBOL[1]




[1] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**LOGIC DIAGRAM (POSITIVE LOGIC)**




## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 4.6 | V |
| $V_I$ | Input voltage range(2) | | -0.5 | 4.6 | V |
| $V_O$ | Output voltage range(2)(3) | | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | -50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | -50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DGG package | | 81 | °C/W |
| | | DL package | | 74 | |
| $T_{stg}$ | Storage temperature range | | -65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51.

## RECOMMENDED OPERATING CONDITIONS[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | -4 | mA |
| | | $V_{CC}$ = 2.3 V | | -12 | |
| | | $V_{CC}$ = 2.7 V | | -12 | |
| | | $V_{CC}$ = 3 V | | -24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 12 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = -100 µA | 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | | | V |
| | | $I_{OH}$ = -4 mA | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = -6 mA | 2.3 V | 2 | | | |
| | | $I_{OH}$ = -12 mA | 2.3 V | 1.7 | | | |
| | | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = -24 mA | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 4 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 6 mA | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 12 mA | 2.3 V | | | 0.7 | |
| | | | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3 V | | | 0.55 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | 3.6 V | | | ±5 | µA |
| $I_{I(hold)}$ | | $V_I$ = 0.58 V | 1.65 V | 25 | | | µA |
| | | $V_I$ = 1.07 V | 1.65 V | -25 | | | |
| | | $V_I$ = 0.7 V | 2.3 V | 45 | | | |
| | | $V_I$ = 1.7 V | 2.3 V | -45 | | | |
| | | $V_I$ = 0.8 V | 3 V | 75 | | | |
| | | $V_I$ = 2 V | 3 V | -75 | | | |
| | | $V_I$ = 0 to 3.6 V(2) | 3.6 V | | | ±500 | |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | 3.6 V | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 40 | µA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ - 0.6 V, Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | µA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 4.5 | | pF |
| | Data inputs | | | | 6.5 | | |
| $C_o$ | Outputs | $V_O$ = $V_{CC}$ or GND | 3.3 V | | 7 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| | | $V_{CC}$ = 1.8 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high or low | (1) | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before LE↑ | (1) | | 0.9 | | 0.7 | | 1.1 | | ns |
| $t_h$ | Hold time, data after LE↑ | (1) | | 1.2 | | 1.5 | | 1.1 | | ns |

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | (1) | 1 | 5 | | 4.7 | 1.2 | 3.9 | ns |
| | LE | | (1) | 1 | 5.6 | | 5.1 | 1 | 4.3 | |
| $t_{en}$ | $\overline{OE}$ | Q | (1) | 1 | 6.2 | | 6 | 1 | 4.9 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | (1) | 1.1 | 5.3 | | 4.3 | 1.3 | 4.1 | ns |

(1) This information was not available at the time of publication.

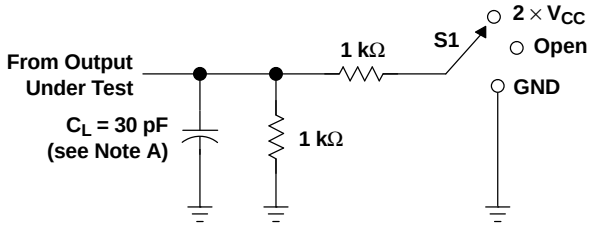
## OPERATING CHARACTERISTICS

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 10 MHz | (1) | 12 | 20 | pF |
| | | Outputs disabled | | (1) | 1 | 3 | |

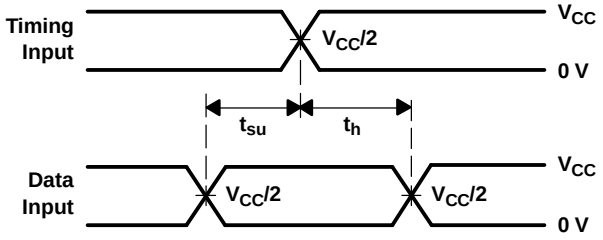
(1) This information was not available at the time of publication.

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V

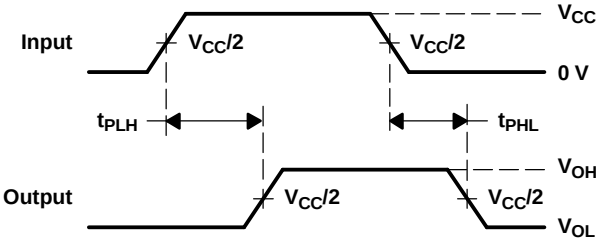



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

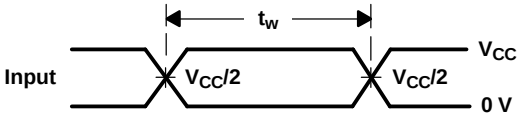
LOAD CIRCUIT



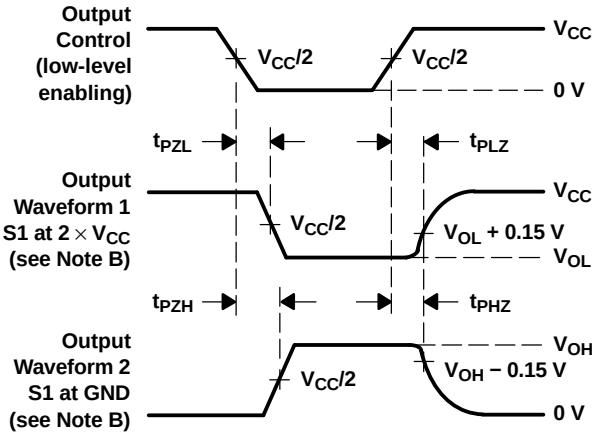

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

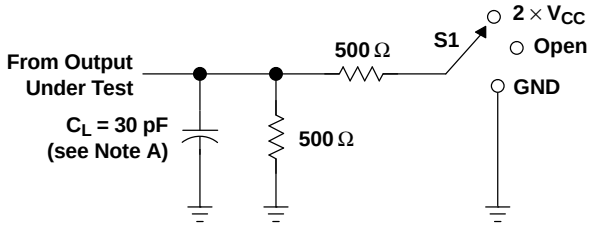



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

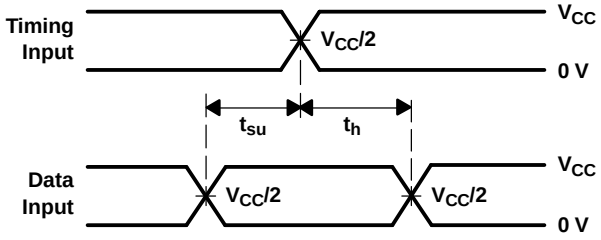
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

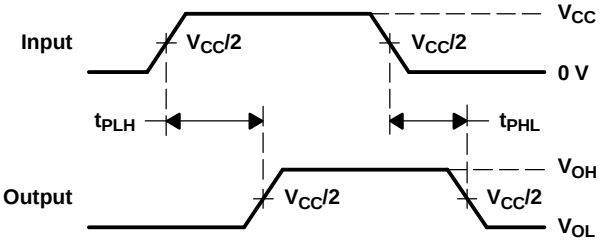



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

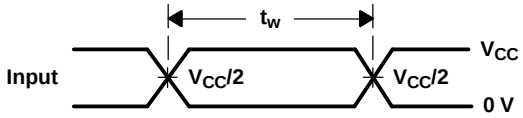
LOAD CIRCUIT



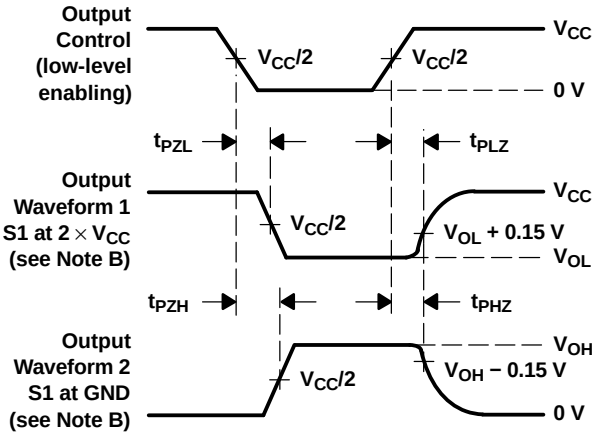

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

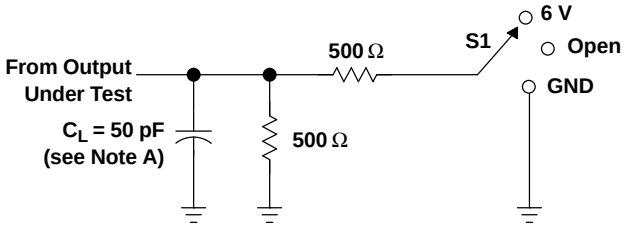



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

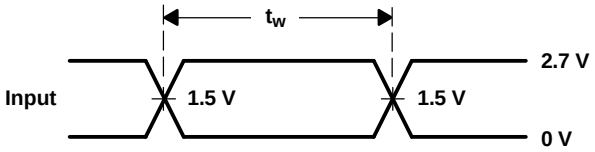
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

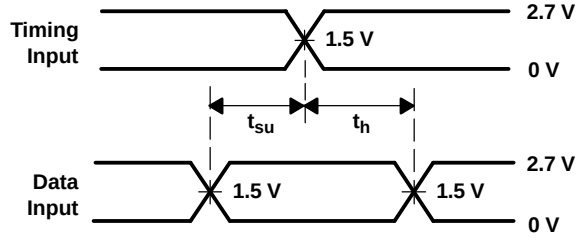



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

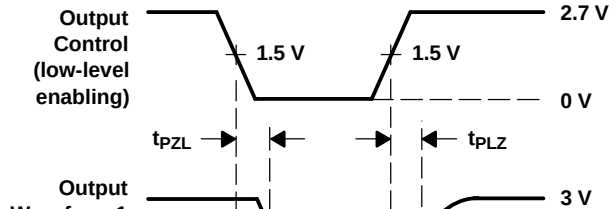
LOAD CIRCUIT



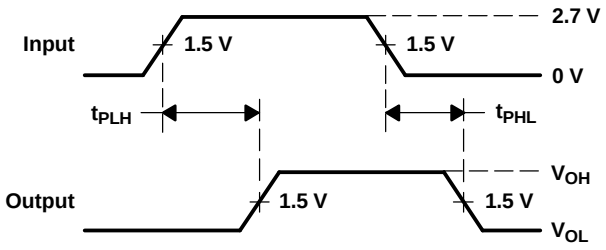

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 74ALVCH16841DGGRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16841DGGRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16841DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16841DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH16841DGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH16841DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH16841DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

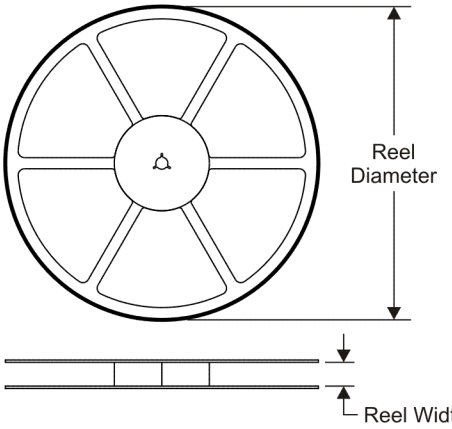
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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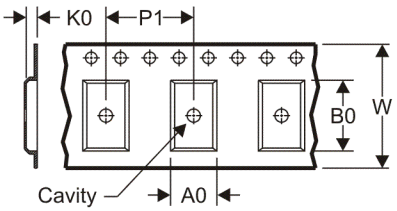
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

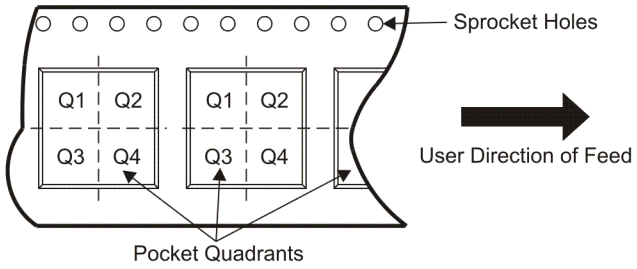



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

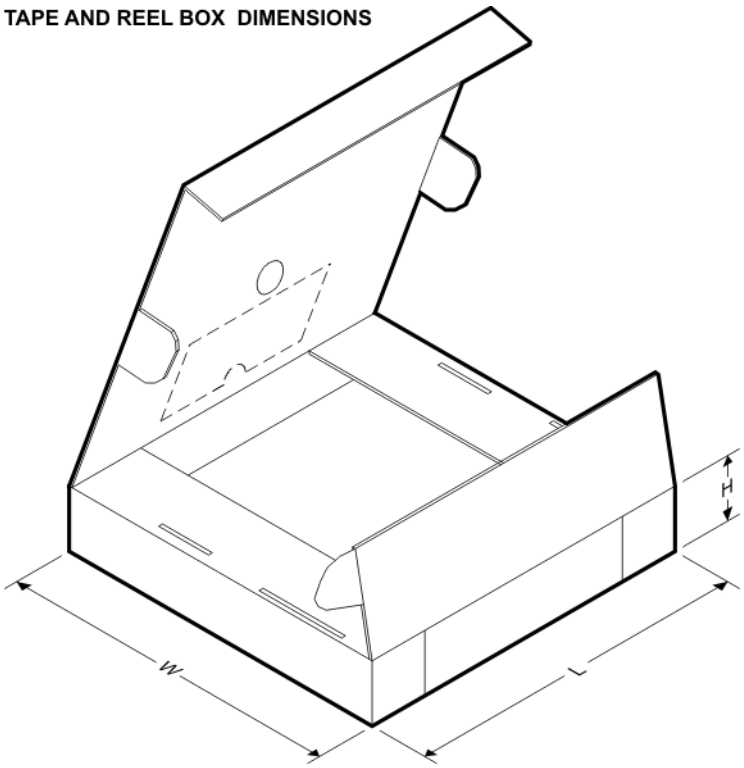
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALVCH16841DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ALVCH16841DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

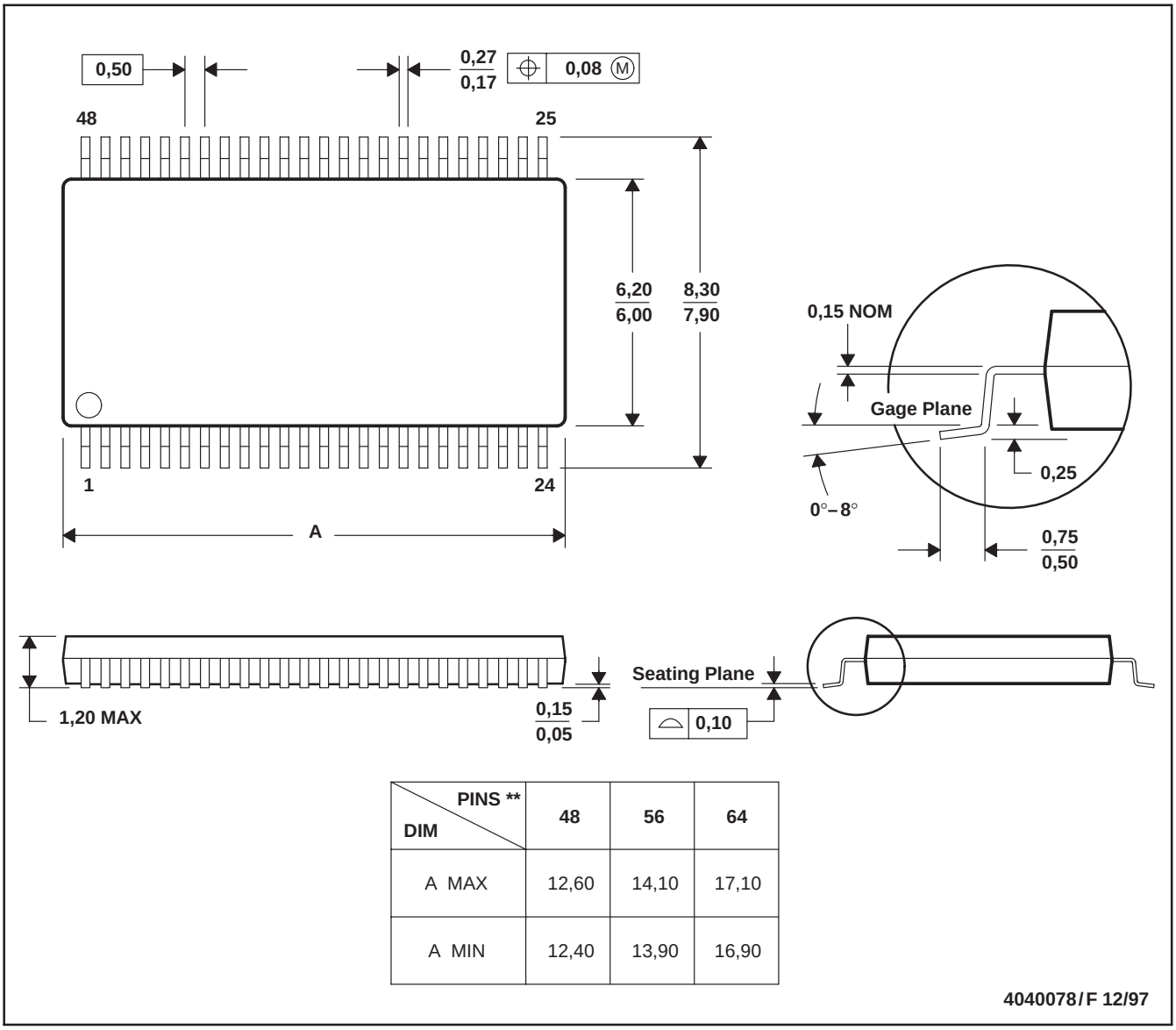



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALVCH16841DGGR | TSSOP | DGG | 56 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ALVCH16841DLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**

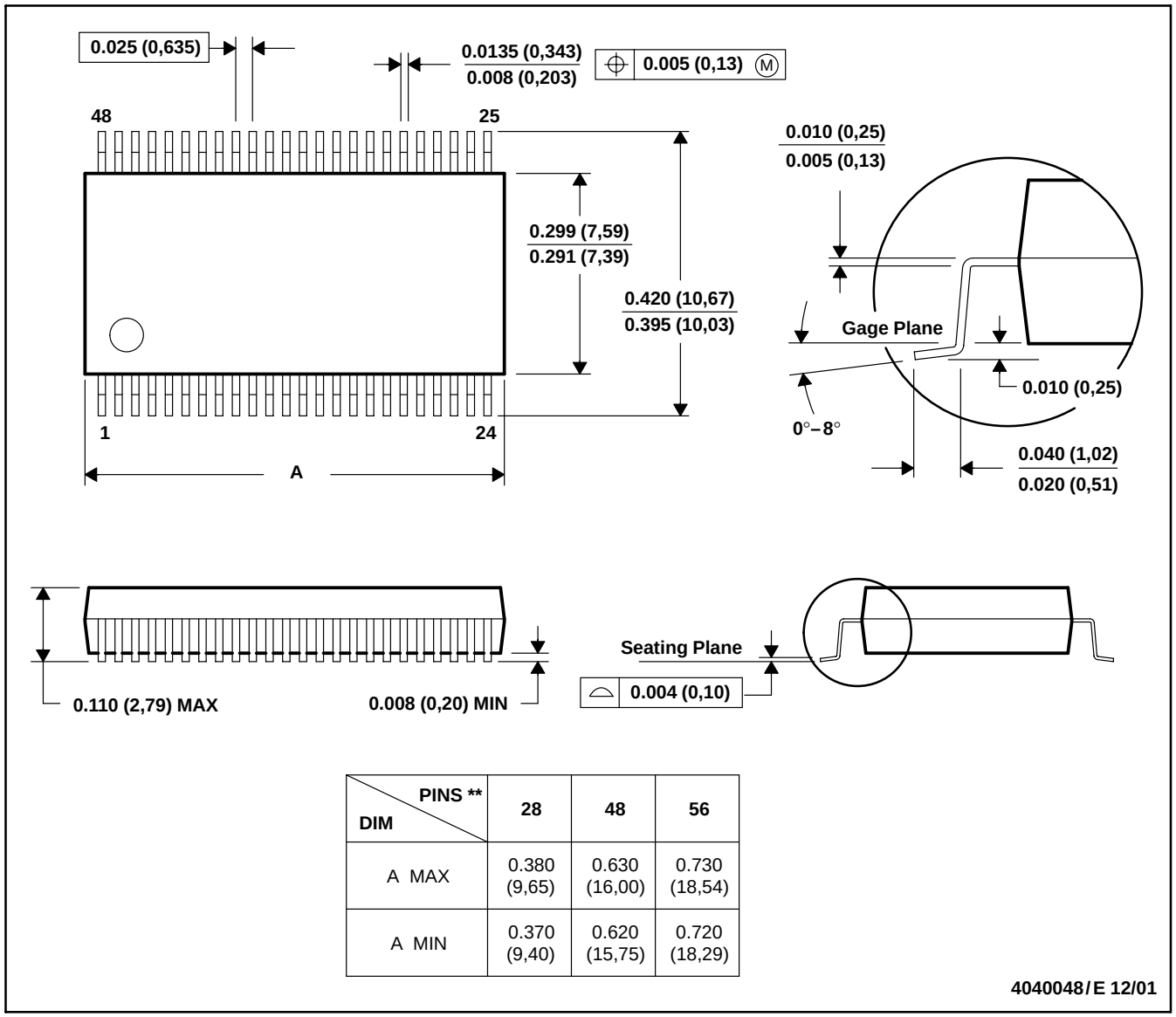



| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

**DL (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |

**4040048/E 12/01**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

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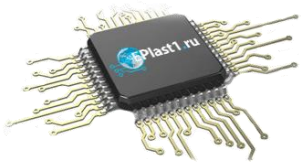
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