NCV47722

High Side Switch with Adjustable Current Limit and Diagnostic Features

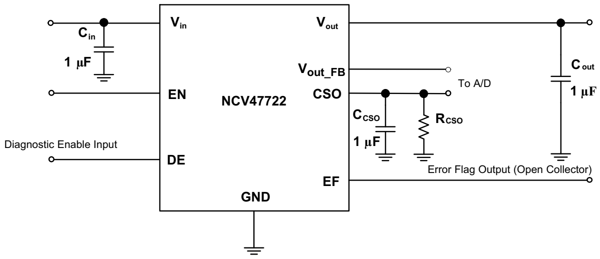
The NCV47722 High Side Switch (HSS) with 250 mA is designed for use in harsh automotive environments. The device has a high peak input voltage tolerance and reverse input voltage, reverse bias, overcurrent and overtemperature protections. The integrated current sense feature (adjustable by resistor connected to CSO pin) provides diagnosis and system protection functionality. The CSO pin output current creates voltage drop across CSO resistor which is proportional to output current. Extended diagnostic features in OFF state are also available and controlled by dedicated input and output pins.

Features

- Output Current: up to 250 mA
- Enable Input (3.3 V Logic Compatible)
- Adjustable Current Limit: up to 350 mA
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage and Reverse Bias Voltage
- Diagnostic Features:
  - Short To Battery (STB) and Open Load (OL) in OFF State
  - Internal Components for OFF State Diagnostics
  - Open Collector Flag Output
  - Output Voltage Monitoring Output (analog)
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Audio and Infotainment System
- Active Safety System



*Vout_FB is sensed Vout output voltage via internal resistor divider

Figure 1. Application Schematic

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

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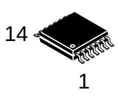
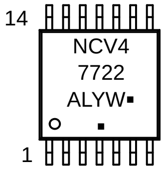
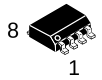
MARKING DIAGRAM

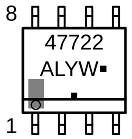


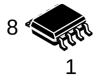
TSSOP−14
Exposed Pad
CASE 948AW



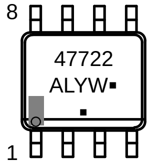


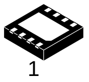
SO−8
D SUFFIX
CASE 751
(In Development)



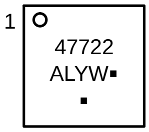


SO−8
Exposed Pad
PD SUFFIX
CASE 751AC
(In Development)





DFN8
MNW SUFFIX
CASE 506BY
(In Development)

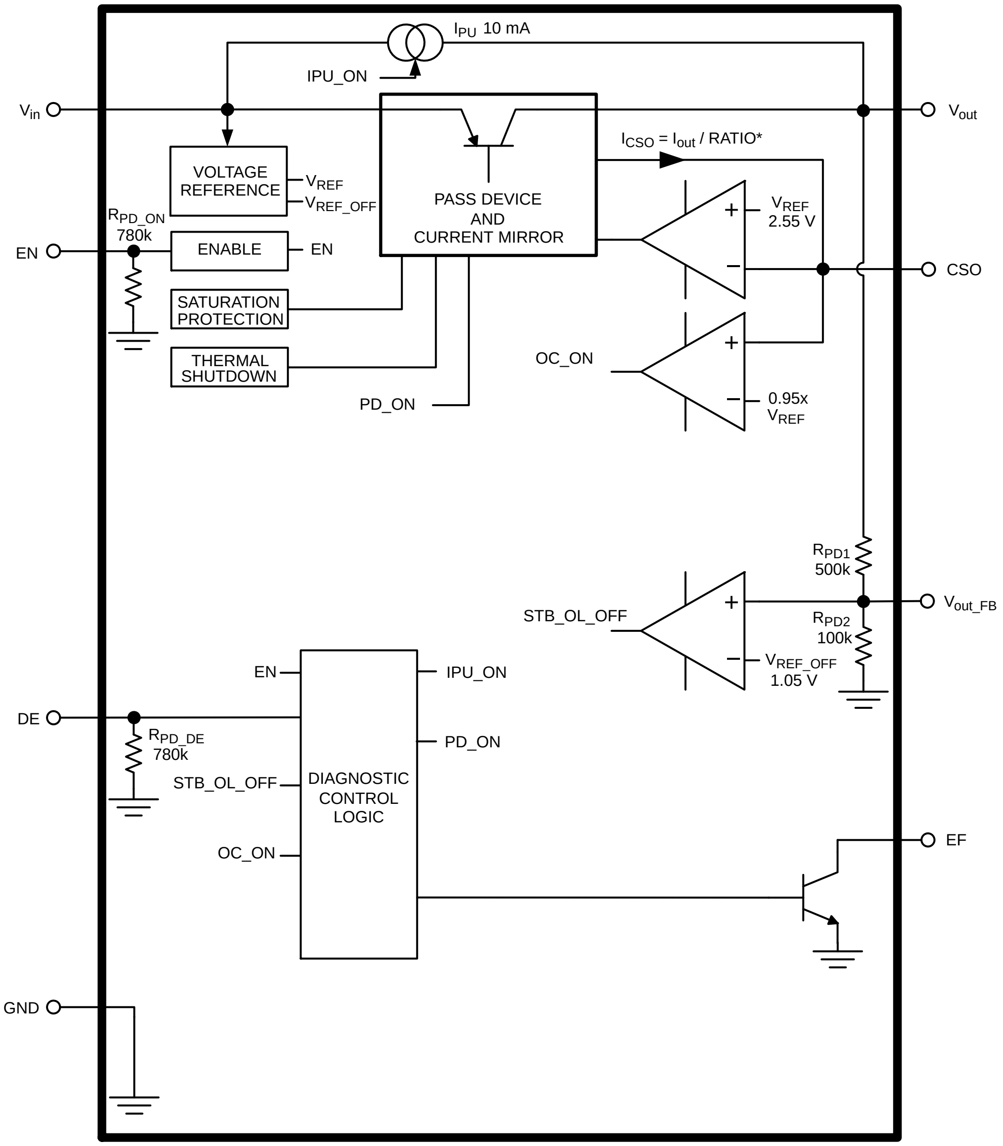


47722 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

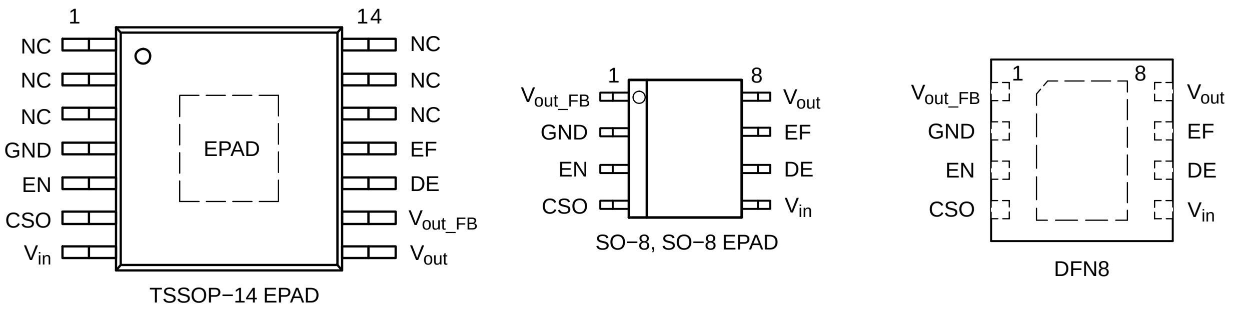
See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

April, 2017 − Rev. 0



*) for current value of RATIO see into Electrical Characteristic Table

Figure 2. Simplified Block Diagram



TSSOP−14 EPAD

SO−8, SO−8 EPAD

DFN8

Figure 3. Pin Connections (Top Views)

Table 1. PIN FUNCTION DESCRIPTION

Pin No. TSSOP−14 EPAD	Pin No. SO−8	Pin No. SO−8 EPAD, DFN8	Pin Name	Description
1	−	−	NC	Not Connected, not internally bonded.
2	−	−	NC	Not Connected, not internally bonded.
3	−	−	NC	Not Connected, not internally bonded.
4	2	2	GND	Power Supply Ground.
5	3	3	EN	Enable Input; low level disables regulator. (Used also for OFF state diagnostics control.
6	4	4	CSO	Current Sense Output, Current Limit setting and Output Current value information. See Application Section for more details.
7	5	5	V_{in}	Power Supply Input.
8	8	8	V_{out}	Regulated Output Voltage.
9	1	1	V_{out_FB}	Output Voltage Analog Monitoring. See Application Section for more details.
10	6	6	DE	Diagnostic Enable Input.
11	7	7	EF	Error Flag (Open Collector) Output. Active Low.
12	−	−	NC	Not Connected, not internally bonded.
13	−	−	NC	Not Connected, not internally bonded.
14	−	−	NC	Not Connected, not internally bonded.
EPAD	−	EPAD	EPAD	Exposed Pad is connected to Ground. Connect to GND plane on PCB.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC	V_{in}	−42	45	V
Input Voltage (Note 1) Load Dump − Suppressed	U_{s*}	 −	 60	V
Enable Input Voltage	V_{EN}	−42	45	V
Output Voltage Monitoring	V_{out_FB}	−0.3	10	V
CSO Voltage	V_{CSO}	−0.3	7	V
DE, CS and EF Voltages	V_{DE}, V_{CS}, V_{EF}	−0.3	7	V
Output Voltage	V_{out}	−1	40	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

Table 3. ESD CAPABILITY (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes < 50 mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS (Note 4)

Rating	Symbol	Value	Unit
Thermal Characteristics (single layer PCB) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead (Note 5)	 $R_{\theta JA}$ $R_{\psi JL}$	 62.6 23.7	°C/W
Thermal Characteristics (4 layers PCB) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead (Note 5)	 $R_{\theta JA}$ $R_{\psi JL}$	 44.1 16.8	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3, 4 layers − according to JEDEC51.7

Table 5. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 6)	V_{in}	4.4	40	V
Output Current Limit (Note 7)	I_{LIM}	10	350	mA
Junction Temperature	T_J	−40	150	°C
Current Sense Output (CSO) Capacitor	C_{CSO}	1	4.7	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Minimum V_{in} = 4.4 V or (V_{out} + 0.5 V), whichever is higher.
7. Corresponding R_{CSO} is in range from 76.5 kΩ down to 2185 Ω.

Table 6. ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3.3 V, R_{CSO} = 0 Ω, C_{CSO} = 1 μF, C_{in} = 1 μF, C_{out} = 1 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTPUTS						
Input to Output Differential Voltage	V_{in} = 8 V to 18 V I_{out} = 200 mA I_{out} = 250 mA	V_{in-out}	 – –	 200 225	 350 400	mV
CURRENT LIMIT PROTECTION						
Current Limit	$V_{out} = V_{in}$ – 1 V	I_{LIM}	350	–	–	mA
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V	I_{DIS}	–	0.002	10	μA
Quiescent Current, $I_q = I_{in} - I_{out}$	I_{out} = 500 μA, V_{in} = 8 V to 18 V	I_q	–	0.5	1.3	mA
Quiescent Current, $I_q = I_{in} - I_{out}$	I_{out} = 200 mA, V_{in} = 8 V to 18 V	I_q	–	8	19	mA
Quiescent Current, $I_q = I_{in} - I_{out}$	I_{out} = 250 mA, V_{in} = 8 V to 18 V	I_q	–	11	25	mA
ENABLE						
Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	 V_{out} ≤ 0.1 V $V_{out} \geq V_{in}$ – 1 V	$V_{th(EN)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Enable Input Current	V_{EN} = 3.3 V	I_{EN}	2	9	20	μA
Turn On Time from Enable ON to $V_{out} = V_{in}$ – 1 V	I_{out} = 100 mA	t_{on}	 –	 25	 –	μs
OUTPUT CURRENT SENSE						
CSO Voltage Level at Current Limit	$V_{out} = V_{in}$ – 1 V R_{CSO} = 3.3 kΩ	V_{CSO_Ilim}	2.448 (−4%)	2.55	2.652 (+4%)	V
CSO Transient Voltage Level	C_{CSO} = 4.7 μF, R_{CSO} = 3.3 kΩ I_{out} pulse from 10 mA to 350 mA, tr = 1 μs	V_{CSO}	–	–	3.3	V
Output Current to CSO Current Ratio	V_{CSO} = 2 V, I_{out} = 10 mA to 50 mA V_{in} = 8 V to 18 V, −40°C ≤ T_J ≤ +150°C	I_{out}/I_{CSO}	– (−15%)	265	– (+15%)	–
Output Current to CSO Current Ratio	V_{CSO} = 2 V, I_{out} = 50 mA to 350 mA V_{in} = 8 V to 18 V, −40°C ≤ T_J ≤ +150°C	I_{out}/I_{CSO}	– (−5%)	285	– (+5%)	–
CSO Current at no Load Current	V_{CSO} = 0 V, I_{out} = 0 mA	I_{CSO_off}	–	–	15	μA
DIAGNOSTICS						
Overcurrent Voltage Level Threshold	$V_{out} = V_{in}$ – 1 V R_{CSO} = 3.3 kΩ	V_{OC}	92	95	98	% of V_{CSO_Ilim}
Short To Battery (STB) Voltage Threshold in OFF state	V_{in} = 4.4 V to 18 V, I_{out} = 0 mA	V_{STB}	2	3	4	V
Open Load (OL) Current Threshold in OFF state	V_{in} = 4.4 V to 18 V	I_{OL}	5	10	25	mA
Output Voltage to Output Feedback Voltage Ratio	V_{in} = 4.4 V to 18 V	V_{out}/V_{outFB}	5.7	6	6.3	–
Diagnostics Enable Threshold Voltage Logic Low (OFF) Logic High (ON)		$V_{th(DE)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Error Flag Low Voltage	I_{EF} = −1 mA	V_{EF_Low}	–	0.04	0.4	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 9)	I_{out} = 90 mA	T_{SD}	150	175	195	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

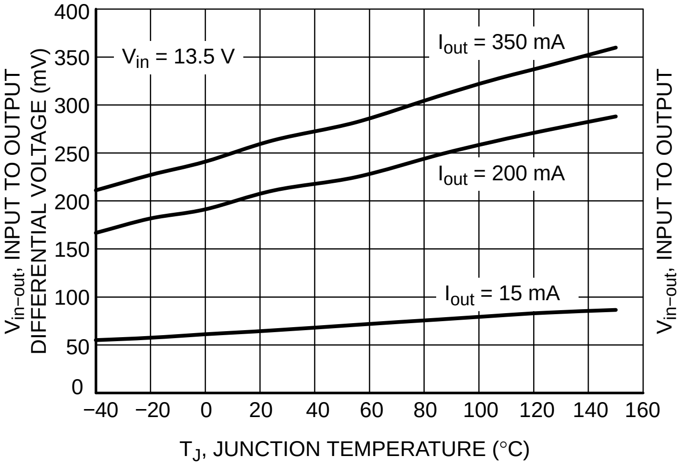


Figure 4. Input to Output Differential Voltage vs. Temperature

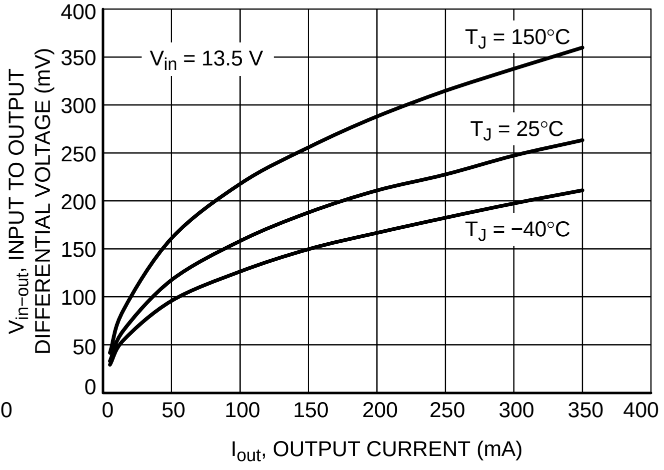


Figure 5. Input to Output Differential Voltage vs. Output Current

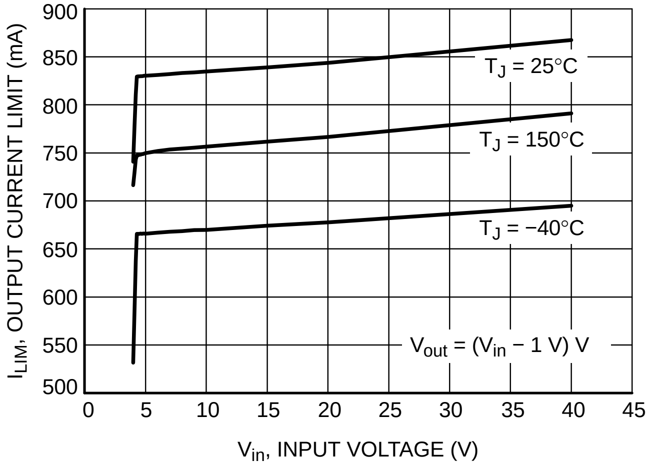


Figure 6. Output Current Limit vs. Input Voltage

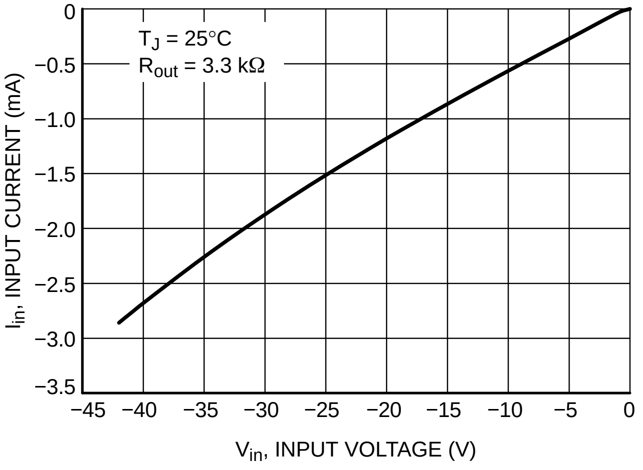


Figure 7. Input Current vs. Input Voltage (Reverse Input Voltage)

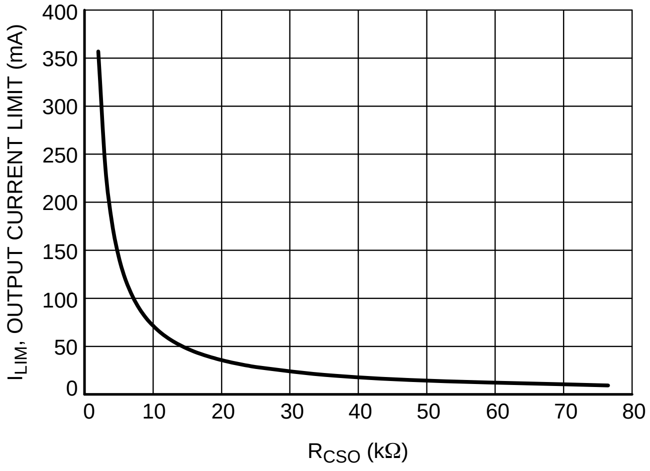


Figure 8. Output Current Limit vs. R_{CSO}

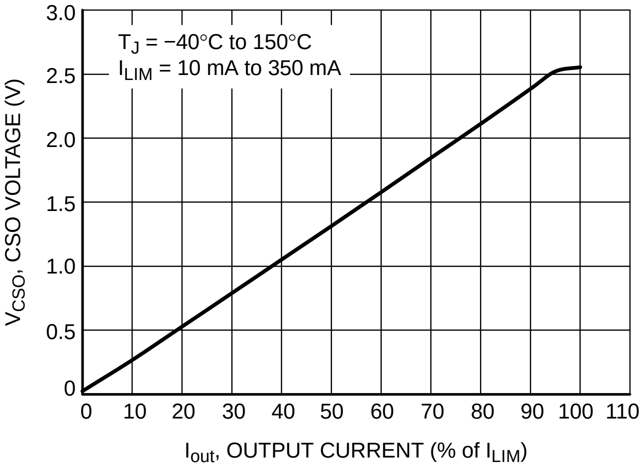


Figure 9. CSO Voltage vs. Output Current (% of I_{LIM})

TYPICAL CHARACTERISTICS

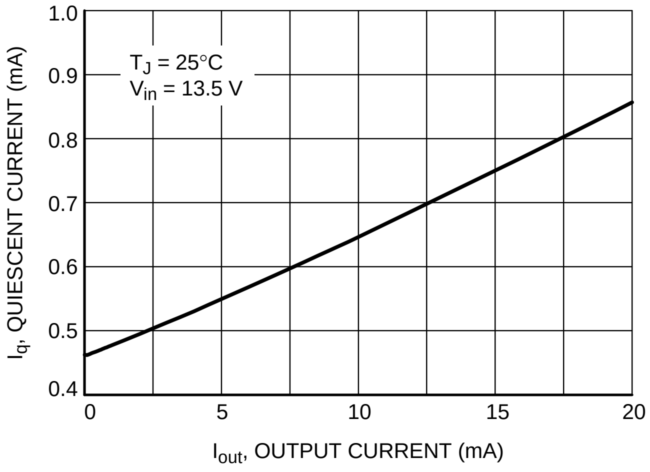


Figure 10. Quiescent Current vs. Output Current (Low Load)

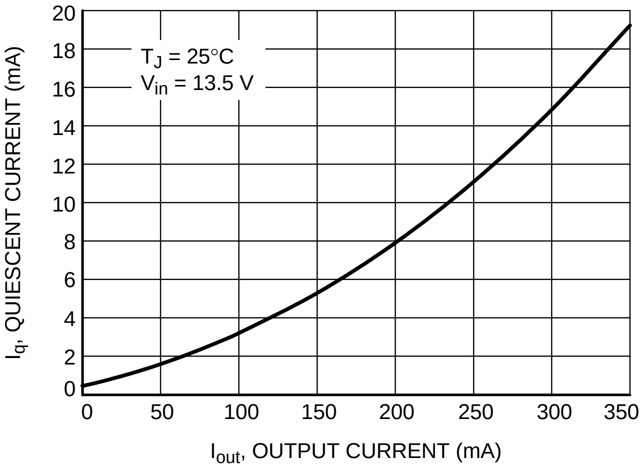


Figure 11. Quiescent Current vs. Output Current (High Load)

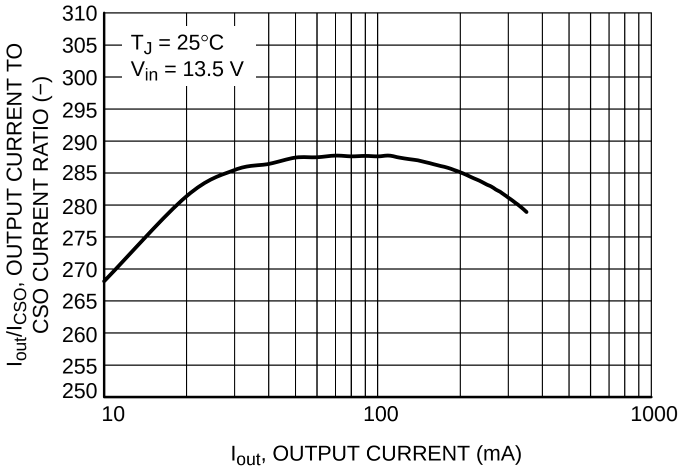


Figure 12. Output Current to CSO Current Ratio vs. Output Current

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Input to Output Differential Voltage

The Input to Output Differential Voltage parameter is defined for specific output current values and specified over Temperature range.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops below 90% of its nominal value.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

Circuit Description

The NCV47722 is an integrated High Side Switch (HSS) with output current capability up to 250 mA to output. It is enabled with an input to the enable pin. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current. The HSS is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.99 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

Setting the Output Current Limit

The output current limit can be set up to 350 mA by external resistor R_{CSO} (see Figure 1). Capacitor C_{CSO} of 1 μF in parallel with R_{CSO} is required for stability of current limit control circuitry (see Figure 1).

$$V_{CSO} = I_{out}\left(R_{CSO} \times \frac{1}{RATIO}\right) \qquad \text{(eq. 1)}$$

$$I_{LIM} = RATIO \times \frac{2.55}{R_{CSO}} \qquad \text{(eq. 2)}$$

$$R_{CSO} = RATIO \times \frac{2.55}{I_{LIM}} \qquad \text{(eq. 3)}$$

where

R_{CSO} − current limit setting resistor
V_{CSO} - voltage at CSO pin proportional to I_{out}
I_{LIM} − current limit value
I_{out} − output current actual value
RATIO − typical value of Output Current to CSO Current Ratio for particular output current range

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to Equation 1.

Once output current reaches its limit value (I_{LIM}) set by external resistor R_{CSO} than voltage at CSO pin is typically 2.55 V. Calculations of I_{LIM} or R_{CSO} values can be done using Equation 2 and Equation 3, respectively. Minimum and maximum value of Output Current Limit can be calculated according to Equations 4 and 5.

$$I_{LIM\_min} = RATIO_{min} \times \frac{V_{CSO\_min}}{R_{CSO\_max}} \qquad \text{(eq. 4)}$$

$$I_{LIM\_max} = RATIO_{max} \times \frac{V_{CSO\_max}}{R_{CSO\_min}} \qquad \text{(eq. 5)}$$

where

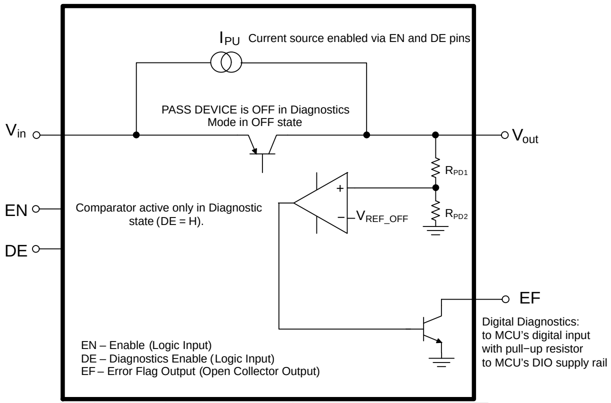
$RATIO_{min}$ − minimum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range
$RATIO_{max}$ − maximum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range
V_{CSO_min} - minimum value of CSO Voltage Level at Current Limit from electrical characteristics table
V_{CSO_max} - maximum value of CSO Voltage Level at Current Limit from electrical characteristics table
R_{CSO_min} − minimum value of R_{CSO} with respect its accuracy
R_{CSO_max} − maximum value of R_{CSO} with respect its accuracy

Designers should consider the tolerance of R_{CSO} during the design phase.

Diagnostic in OFF State

The NCV47722 contains also circuitry for OFF state diagnostics for Short to Battery (STB) and Open Load (OL). There are internal current source and Pull Down resistors which provide additional cost savings for overall application by excluding external components and their assembly cost and saving PCB space and safe control IOs of a Microcontroller Unit (MCU).

Simplified functional schematic and truth table is shown in Figure 13 and related flowchart in Figure 14.



EN	DE	I_{PU}	EF	V_{out}	Diagnostic Status/Action
L	L	OFF	HZ	Unknown	None (Diagnostics OFF)
L	H	OFF	L	$V_{out} > V_{out\_OFF}$	Short to Battery (STB)
L	H	OFF	HZ	$V_{out} < V_{out\_OFF}$	Check for Open Load (OL)
H	H	ON	L	$V_{out} > V_{out\_OFF}$	Open Load (OL)
H	H	ON	HZ	$V_{out} < V_{out\_OFF}$	No Failure (V_{out} close to 0 V)

Figure 13. Simplified Functional Diagram of OFF State Diagnostics (STB and OL)

For diagnostics in OFF state the input DE pin has to be put logic high. Logic level on EN pin determines which failure (STB or OL) is diagnosed. For detailed information see Diagnostic Truth Table 7.

Diagnostic in ON State

Diagnostic in ON State provides information about Overcurrent or Short to Ground failures, during which the EF output is in logic low state. For detailed information see Diagnostic Features Truth Table 7.

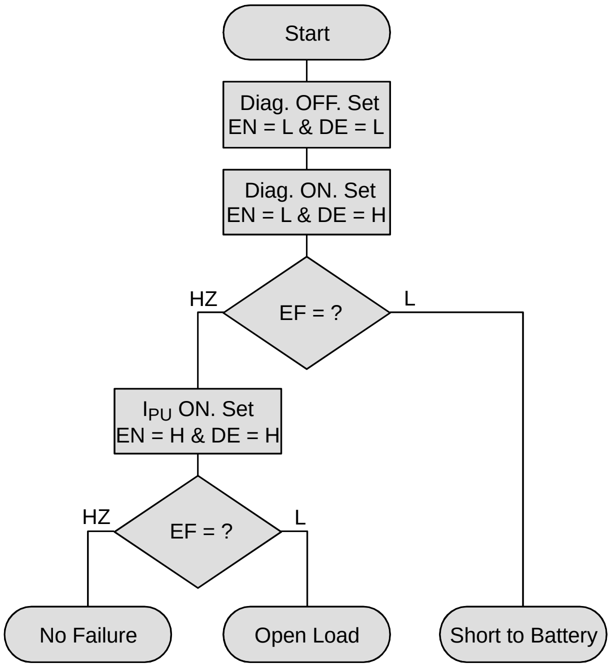


Figure 14. Flowchart for Diagnostics in OFF State

Table 7. DIAGNOSTIC FEATURES TRUTH TABLE

Operational Status	EN	DE	Output Voltage (V_{out})	Diagnostic Output (CSO)	Error Flag (EF)
Disabled	L	L	Low (~0 V)	Low (~0 V)	HZ
Short to Battery	L	H	High ($V_{out} \sim V_{in}$)	Low (~0 V)	L (Note 10)
Open Load (OFF)	H	H	High ($V_{out} \sim V_{in}$)	Low (~0 V)	L (Note 11)
Normal (OFF)	H	H	Low (~0 V)	Low (~0 V)	HZ (Note 11)
Open Load (ON)	H	L	High ($V_{out} \sim V_{in}$)	Low (~0 V)	HZ
Normal (ON)	H	L	High ($V_{out} \sim V_{in}$)	Proportional to I_{out} (±5%) (Note 12)	HZ
Over Current	H	L	$V_{in} - 1$ V	High (~2.55 V)	L
Short to Ground	H	L	Low (~0 V)	High (~2.55 V)	L

10. Internal current source disabled (between V_{out} and V_{in}).
11. Internal current source enabled (between V_{out} and V_{in}).
12. Valid for I_{out} = 50 mA to 350 mA. For I_{out} = 10 mA to 50 mA range proportional to I_{out} (±15%).

Thermal Considerations

As power in the device increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the device can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 6)}$$

Since T_J is not recommended to exceed 150°C, then the device soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2 W when the ambient temperature (T_A) is 25°C. See Figure 15 for $R_{\theta JA}$ versus PCB area. The power dissipated by the device can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 7)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 8)}$$

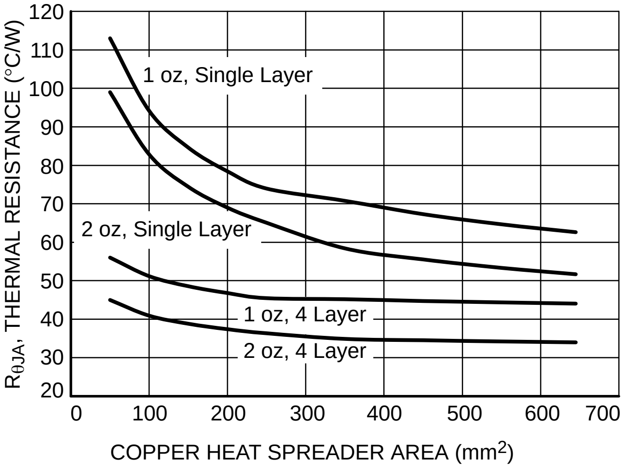


Figure 15. Thermal Resistance vs. PCB Copper Area

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device and make traces as short as possible.

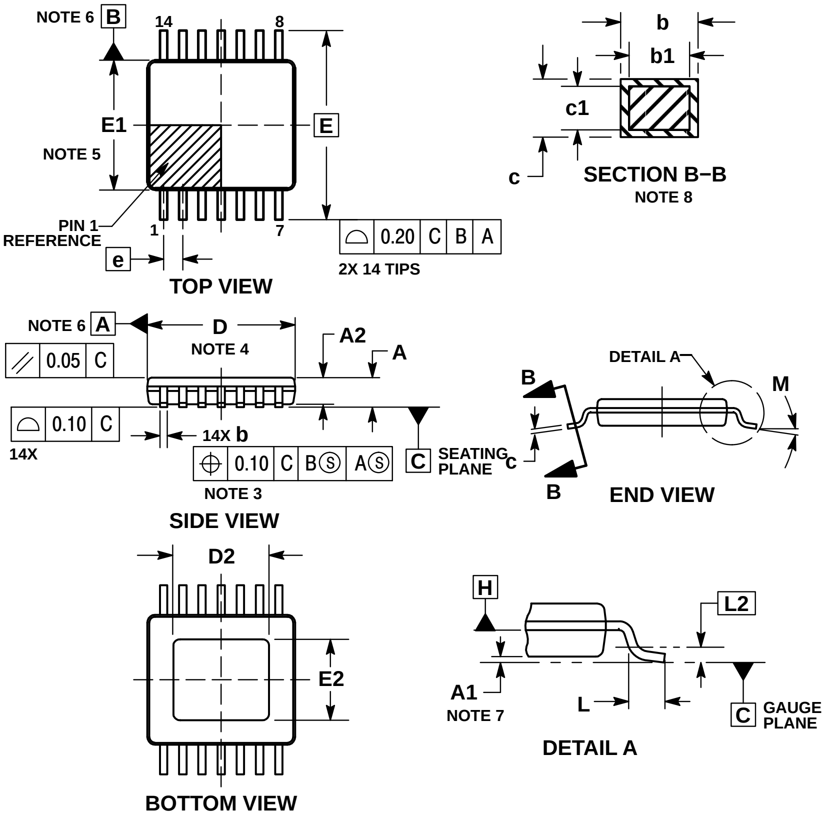
ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCV47722PAAJR2G	Adjustable	Line1: NCV4 Line2: 7722	TSSOP−14 Exposed Pad (Pb−Free)	2500 / Tape & Reel
NCV47722PDAJR2G (In Development)	Adjustable	47722	SOIC−8 EP (Pb−Free)	2500 / Tape & Reel
NCV47722DAJR2G (In Development)	Adjustable	47722	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV47722MNWTXG (In Development)	Adjustable	47722	DFN8 with wettable flanks (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

PACKAGE DIMENSIONS

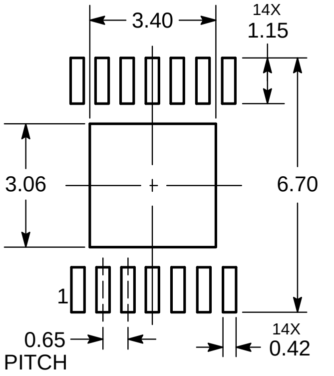
TSSOP−14 EP
CASE 948AW
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−−	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT

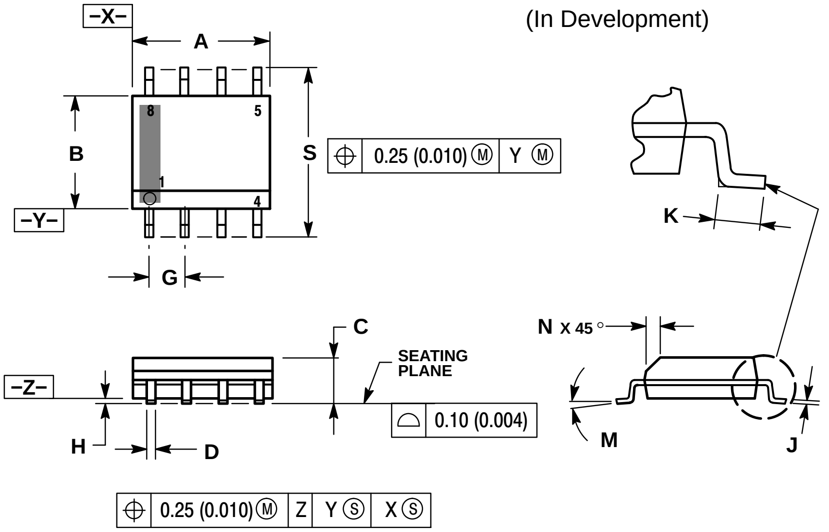


DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

SOIC−8 NB

CASE 751−07
ISSUE AK
(In Development)

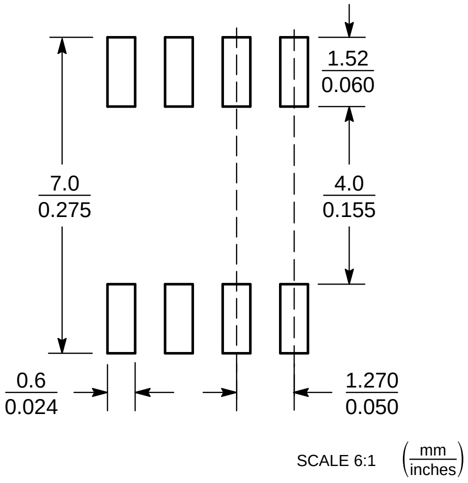


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

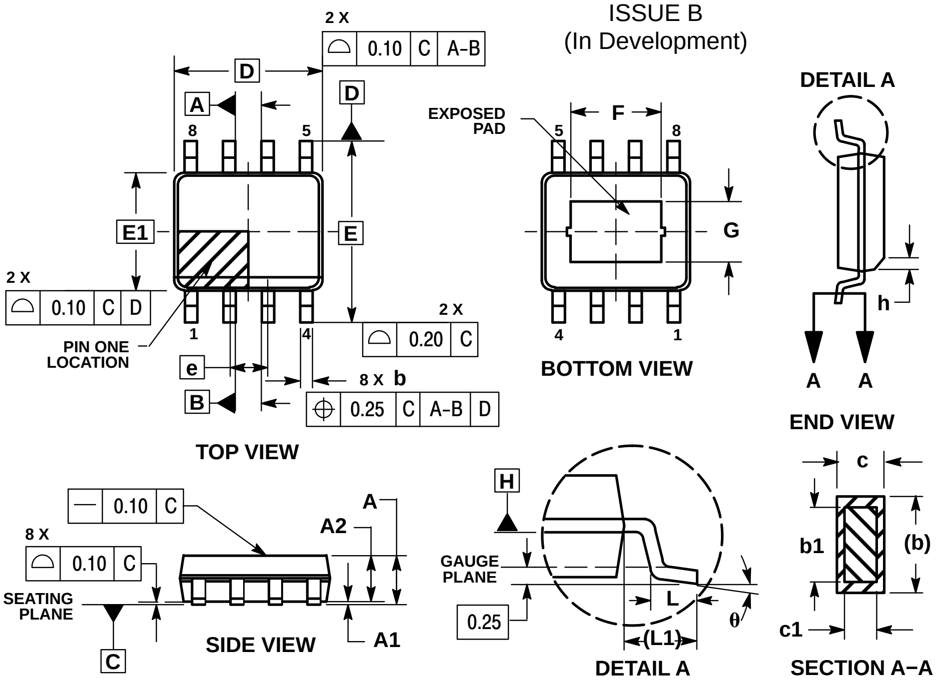
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

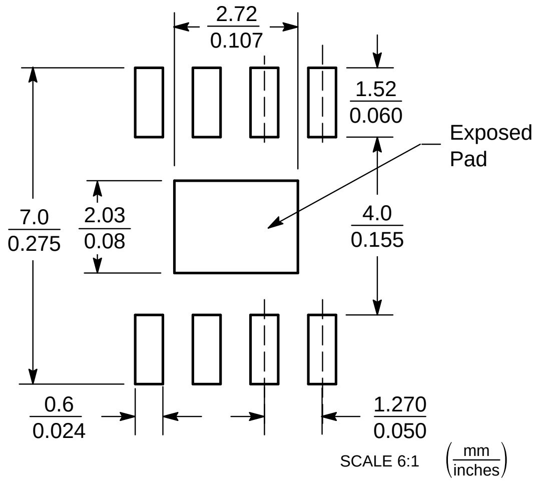
SOIC−8 EP
CASE 751AC
ISSUE B
(In Development)



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE “b” DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0 °	8 °

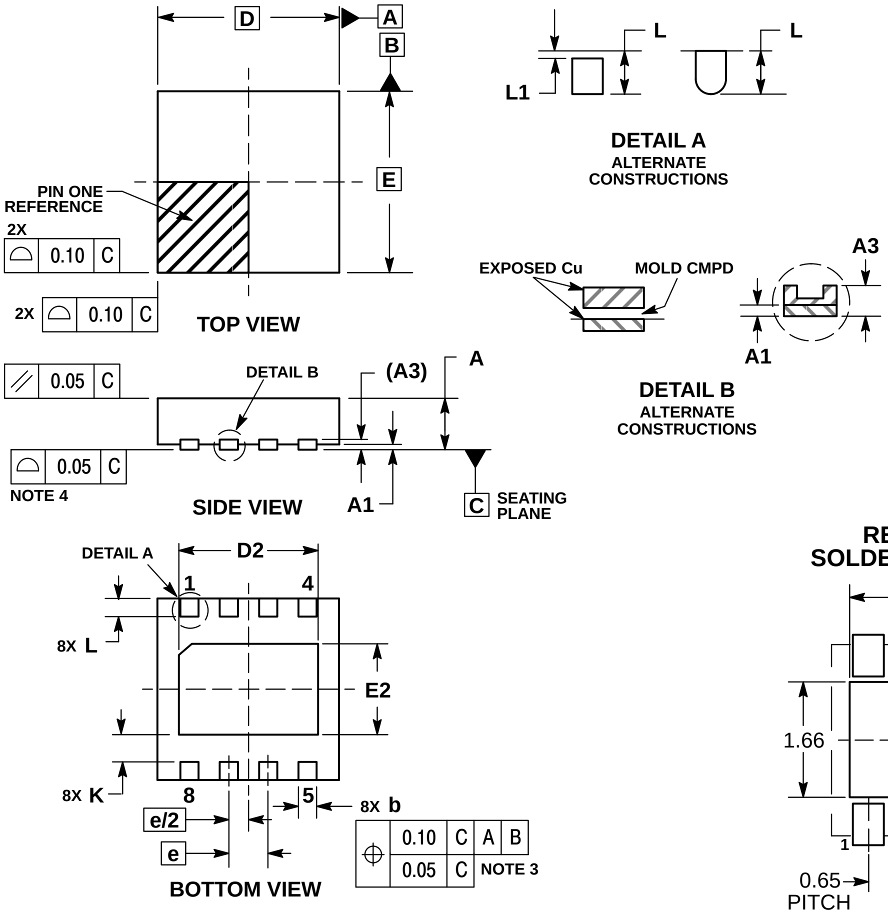
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

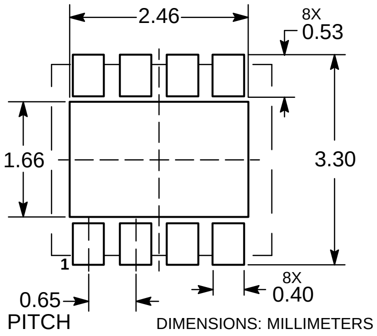
DFN8, 3x3, 0.65P
CASE 506BY
ISSUE A
(In Development)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.20	2.40
E	3.00 BSC	
E2	1.40	1.60
e	0.65 BSC	
K	0.20	−−−
L	0.20	0.40
L1	0.00	0.15

RECOMMENDED SOLDERING FOOTPRINT*



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