

## 512K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

DECEMBER 2010

### FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 12  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 4.5V--5.5V  $V_{DD}$
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Automotive temperature (-40°C to +125°C)
- Lead-free available

### DESCRIPTION

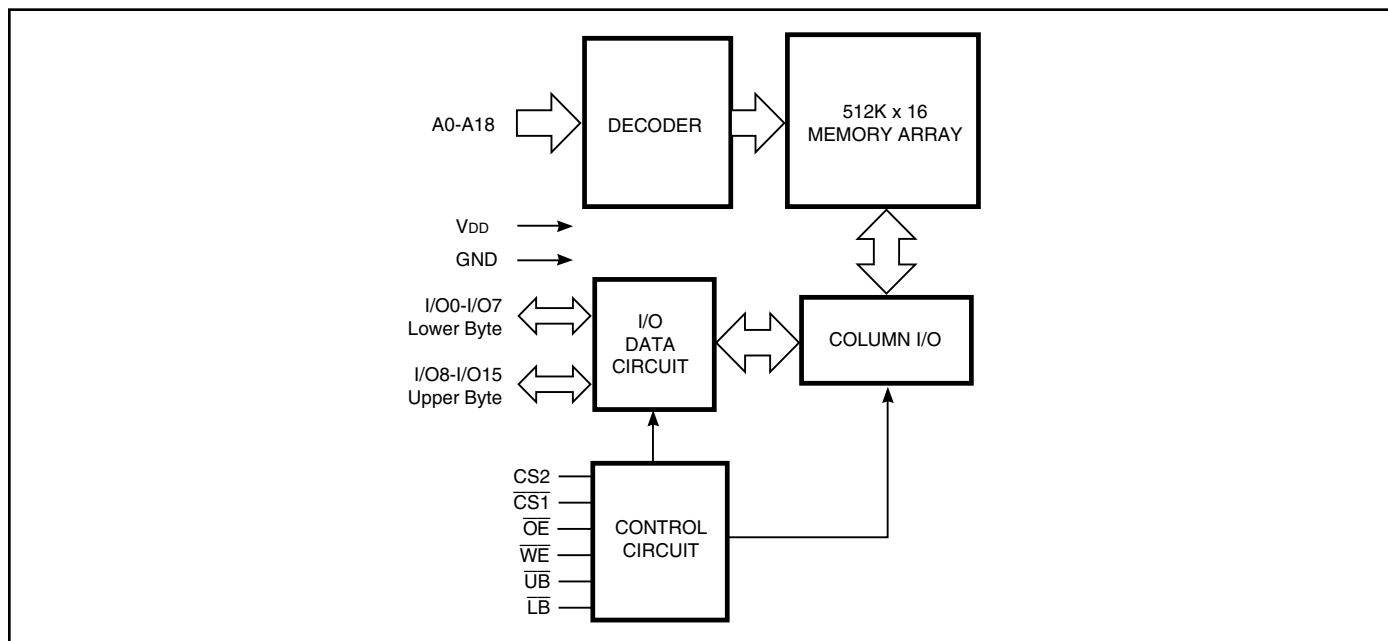
The *ISSI* IS62C51216AL and IS65C51216AL are high-speed, 8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when  $\overline{CS2}$  is LOW (deselected) or when  $\overline{CS1}$  is LOW,  $\overline{CS2}$  is HIGH and both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS62C51216AL and IS65C51216AL are packaged in the JEDEC standard 48-pin mini BGA (9mm x 11mm) and 44-Pin TSOP (TYPE II).

### FUNCTIONAL BLOCK DIAGRAM



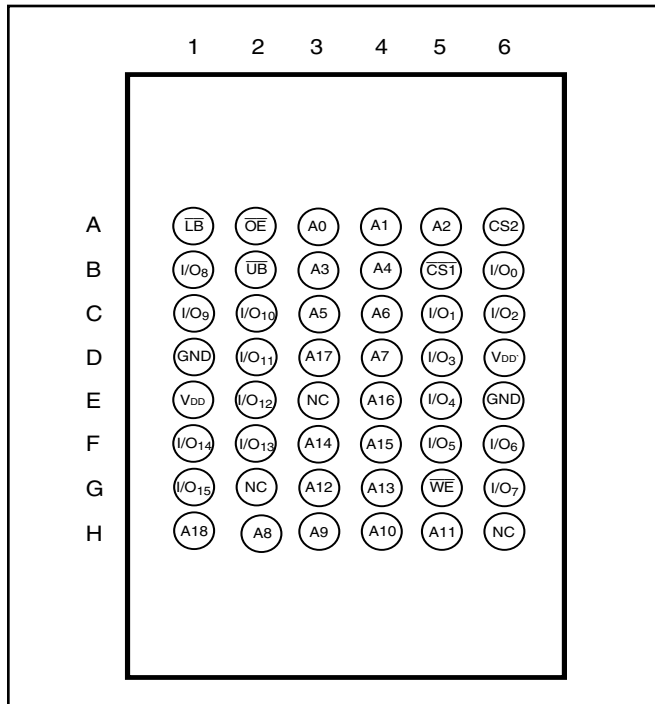
Copyright © 2010 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATIONS**

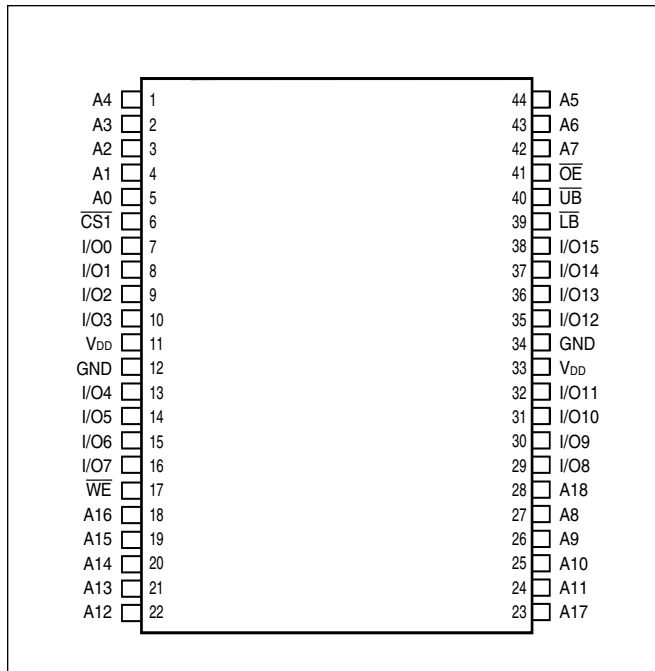
**48-Pin mini BGA (9mmx11mm)**



**PIN DESCRIPTIONS**

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$ , CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V <sub>DD</sub>	Power
GND	Ground

**44-Pin TSOP (Type II)**



**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V <sub>DD</sub> Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	L	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	X	X	H	H	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I <sub>CC</sub>
	H	L	H	H	X	L	High-Z	High-Z	I <sub>CC</sub>
Read	H	L	H	L	L	H	DOUT	High-Z	I <sub>CC</sub>
	H	L	H	L	H	L	High-Z	DOUT	
	H	L	H	L	L	L	DOUT	DOUT	
Write	L	L	H	X	L	H	D <sub>IN</sub>	High-Z	I <sub>CC</sub>
	L	L	H	X	H	L	High-Z	D <sub>IN</sub>	
	L	L	H	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

**OPERATING RANGE (V<sub>DD</sub>)**

Range	Ambient Temperature	V <sub>DD</sub>	Speed
Commercial	0°C to +70°C	4.5V - 5.5V	45ns
Industrial	-40°C to +85°C	4.5V - 5.5V	55ns
Automotive	-40°C to +125°C	4.5V - 5.5V	55ns

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 5.0V.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.5	W
I <sub>OUT</sub>	DC Output Current (LOW)	20	mA

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -1 mA	2.4	—	V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 2.1 mA	—	0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>DD</sub> + 0.5	V	
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V	
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	Com.	-1	1	μA
			Ind.	-2	2	
			Auto.	-5	5	
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> Outputs Disabled	Com.	-1	1	μA
			Ind.	-2	2	
			Auto.	-5	5	

**Note:**

1. V<sub>IL</sub> (min) = -0.3V DC; V<sub>IL</sub> (min) = -2.0V AC (pulse width -2.0 ns). Not 100% tested.  
V<sub>IH</sub> (max) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max) = V<sub>DD</sub> + 2.0V AC (pulse width -2.0 ns). Not 100% tested.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

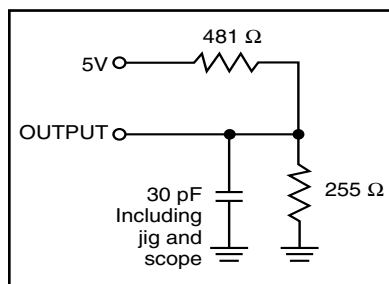
**AC TEST LOADS**


Figure 1

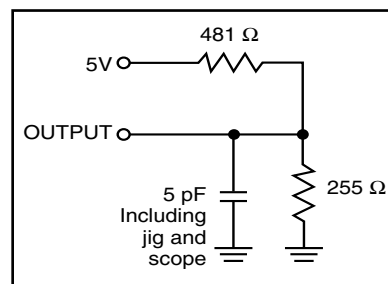


Figure 2

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns		-55 ns		Unit
				Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	Com.	—	25	—	25	mA
			Ind.			—	40	
			Auto. typ. <sup>(2)</sup>	13		12		
I <sub>CC1</sub>	Average operating Current	$\overline{CE} = V_{IL}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA	Com.	—	10	—	10	mA
			Ind.			—	20	
			Auto.					
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CE} \geq V_{IH}$ , f = 0	Com.	—	1	—	1.5	mA
			Ind.			—	2	
			Auto.					
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CE} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> $\geq V_{DD} - 0.2V$ , or V <sub>IN</sub> $\leq V_{SS} + 0.2V$ , f = 0	Com.	—	40	—	60	$\mu A$
			Ind.			—	180	
			Auto. typ. <sup>(2)</sup>	15				

**Note:**

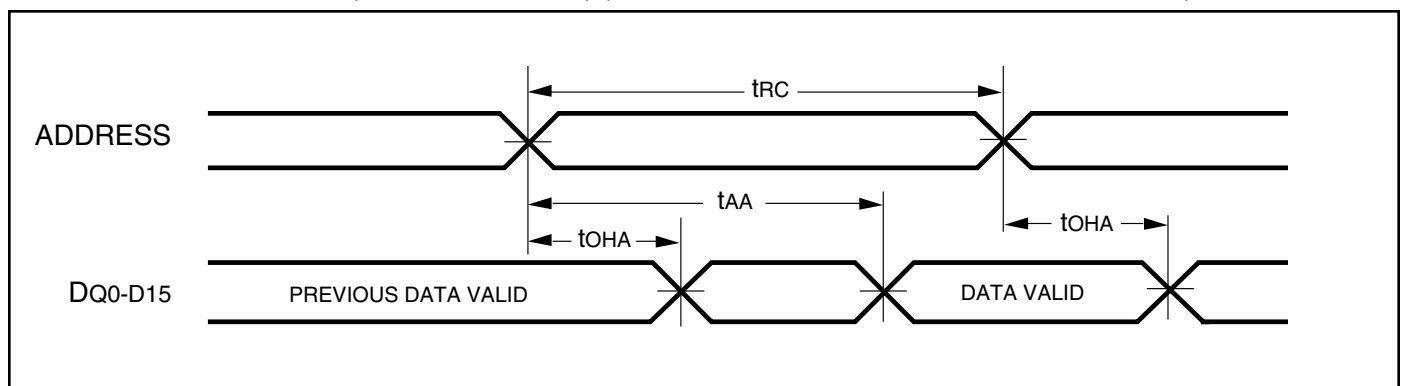
- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical Values are measured at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C and not 100% tested.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	45 ns		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	45	—	55	—	70	—	ns
$t_{AA}$	Address Access Time	—	45	—	55	—	70	ns
$t_{OHA}^3$	Output Hold Time	10	—	10	—	10	—	ns
$t_{ACS1}/t_{ACS2}$	$\overline{CS1}/\overline{CS2}$ Access Time	—	45	—	55	—	70	ns
$t_{DOE}$	$\overline{OE}$ Access Time	—	20	—	25	—	35	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	—	15	—	20	—	25	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
$t_{HZCS1}/t_{HZCS2}^{(2)}$	$\overline{CS1}/\overline{CS2}$ to High-Z Output	0	15	0	20	0	25	ns
$t_{LZCS1}/t_{LZCS2}^{(2)}$	$\overline{CS1}/\overline{CS2}$ to Low-Z Output	10	—	10	—	10	—	ns
$t_{BA}$	$\overline{LB}, \overline{UB}$ Access Time	—	45	—	55	—	70	ns
$t_{HZB}$	$\overline{LB}, \overline{UB}$ to High-Z Output	0	15	0	20	0	25	ns
$t_{LZB}$	$\overline{LB}, \overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns

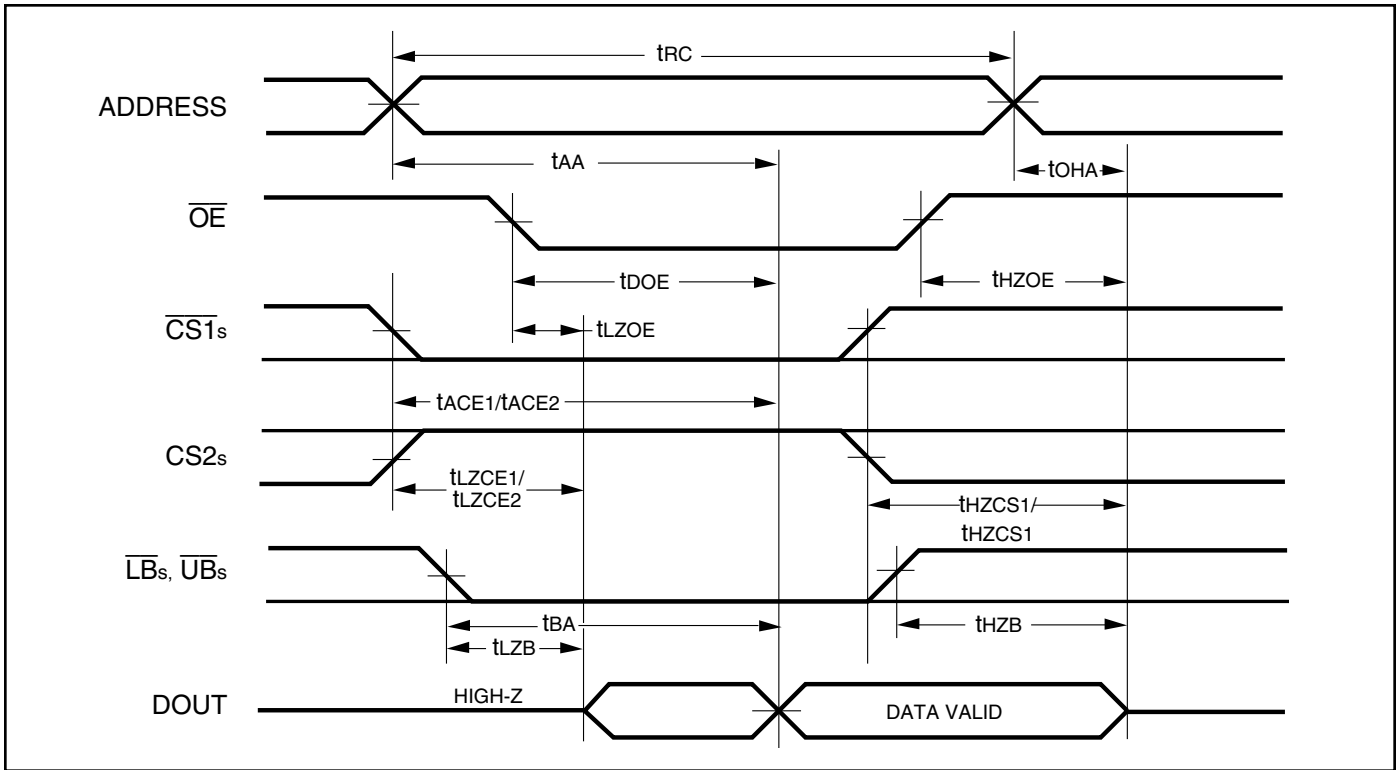
**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. 10ns for CMOS Loading. 8ns @ AC Loading.

**AC WAVEFORMS**
**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $CS2 = \overline{WE} = V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ )


**AC WAVEFORMS**

**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{OE}$ , AND  $\overline{UB}/\overline{LB}$  Controlled)



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

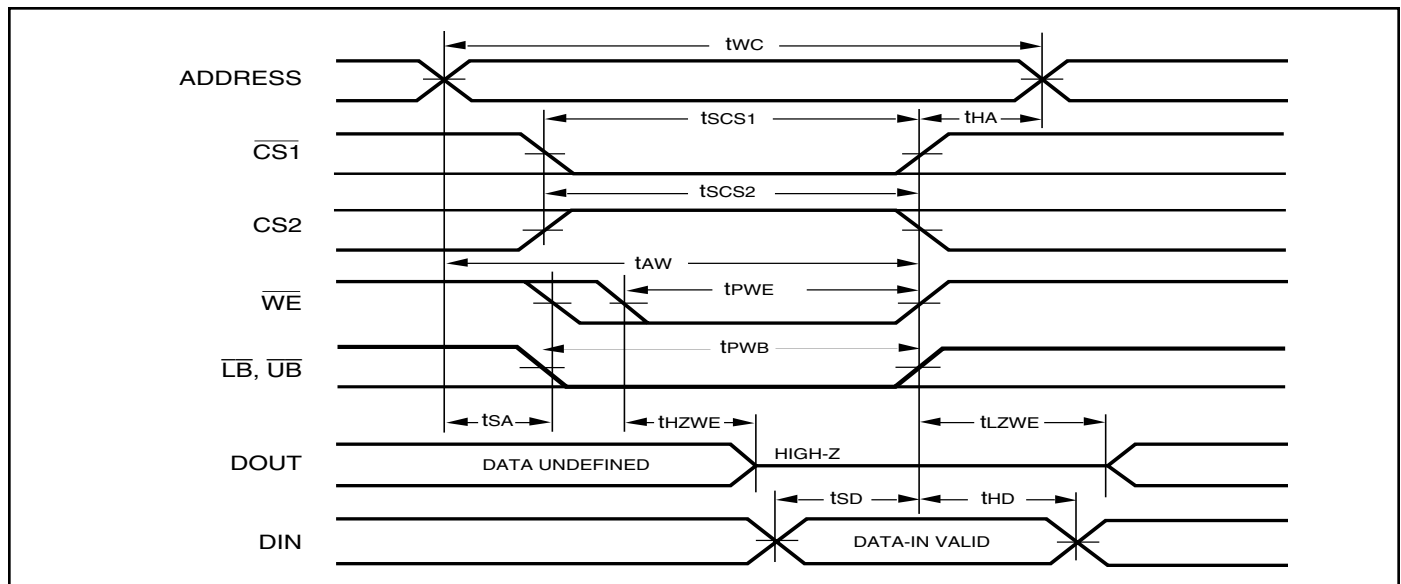


**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)**

Symbol	Parameter	45ns		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	45	—	55	—	70	—	ns
t <sub>SCS1</sub> /t <sub>SCS2</sub>	$\overline{CS1}$ / $\overline{CS2}$ to Write End	35	—	45	—	60	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	35	—	45	—	60	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWB</sub>	$\overline{LB}$ , $\overline{UB}$ Valid to End of Write	35	—	45	—	60	—	ns
t <sub>PWE</sub> <sup>(4)</sup>	$\overline{WE}$ Pulse Width	35	—	40	—	50	—	ns
t <sub>SD</sub>	Data Setup to Write End	25	—	30	—	30	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	30	ns
t <sub>LZWE</sub> <sup>(3)</sup>	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

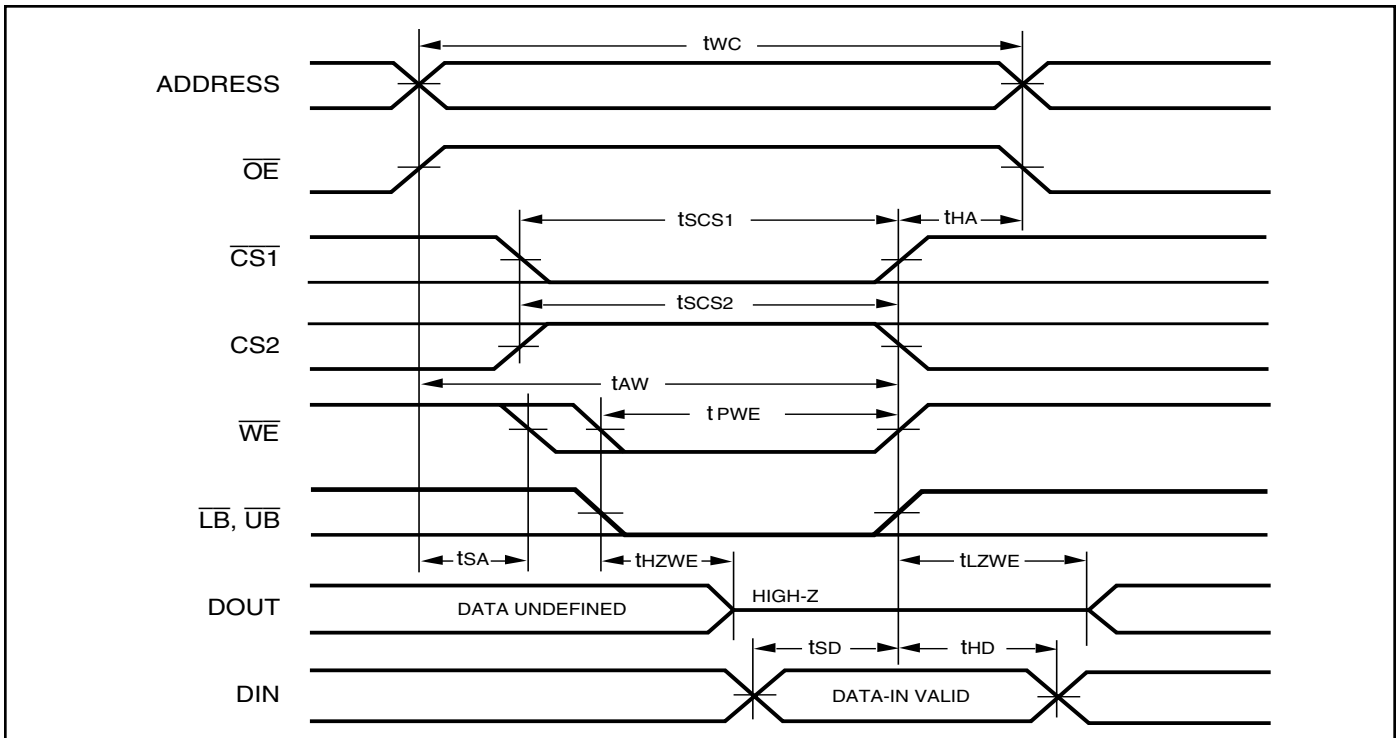
**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW,  $\overline{CS2}$  HIGH and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
4. t<sub>PWE</sub> > t<sub>HZWE</sub> + t<sub>SD</sub> when  $\overline{OE}$  is LOW.

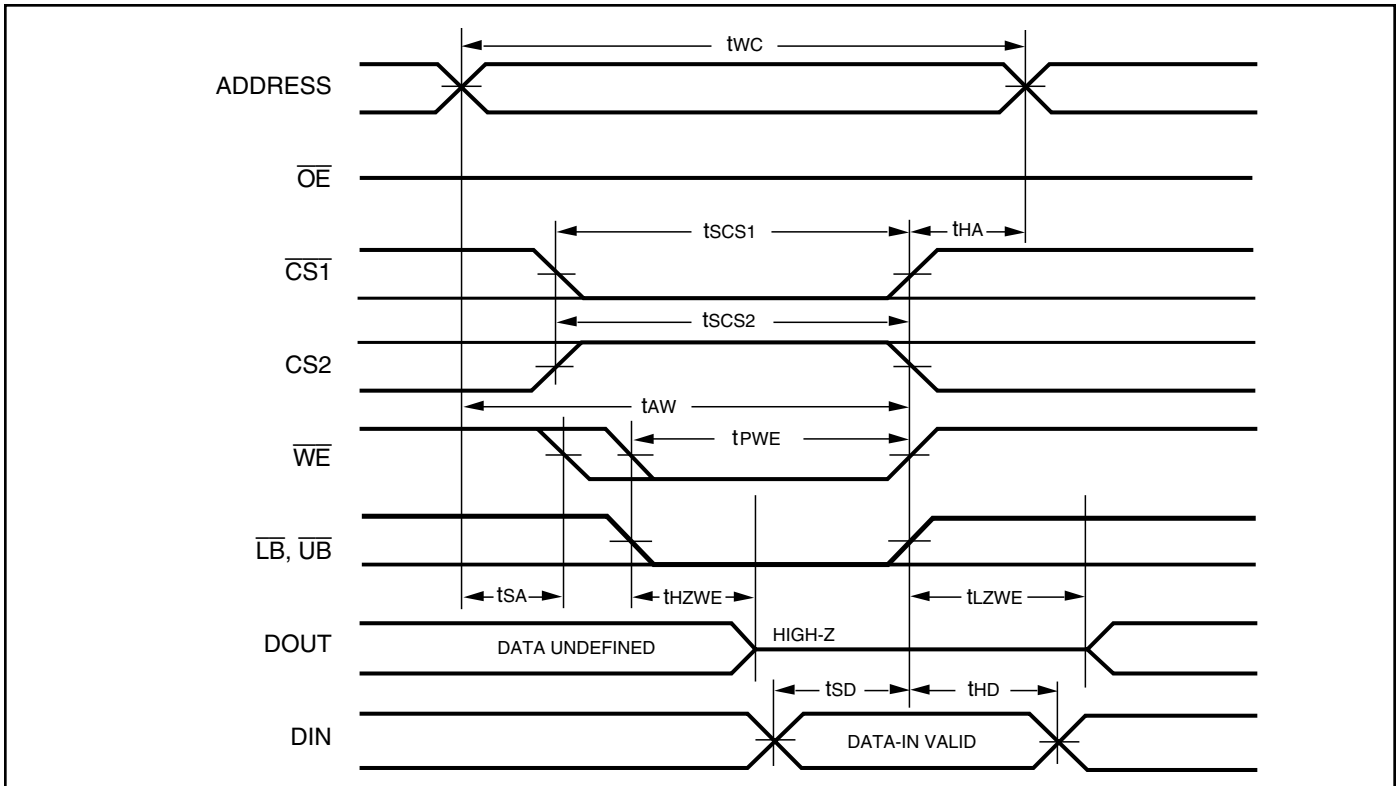
**AC WAVEFORMS**
**WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CS1}$  Controlled,  $\overline{OE}$  = HIGH or LOW)**

**Notes:**

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{WE}$  inputs and at least one of the  $\overline{LB}$  and  $\overline{UB}$  inputs being in the LOW state.
2. WRITE = ( $\overline{CS1}$ ) [ ( $\overline{LB}$ ) = ( $\overline{UB}$ ) ] ( $\overline{WE}$ ).

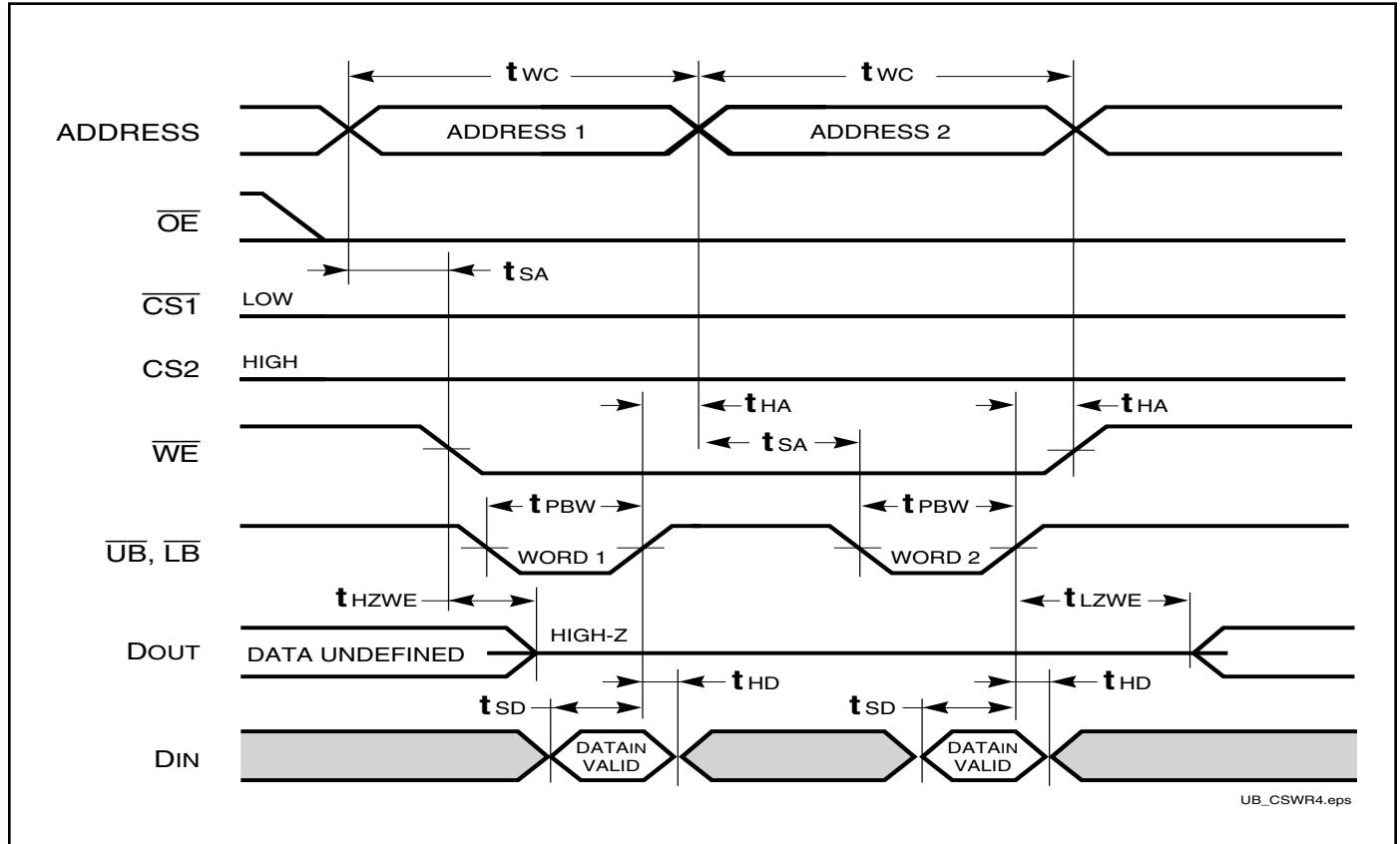
**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



WRITE CYCLE NO. 4 ( $\overline{UB}/\overline{LB}$  Controlled)

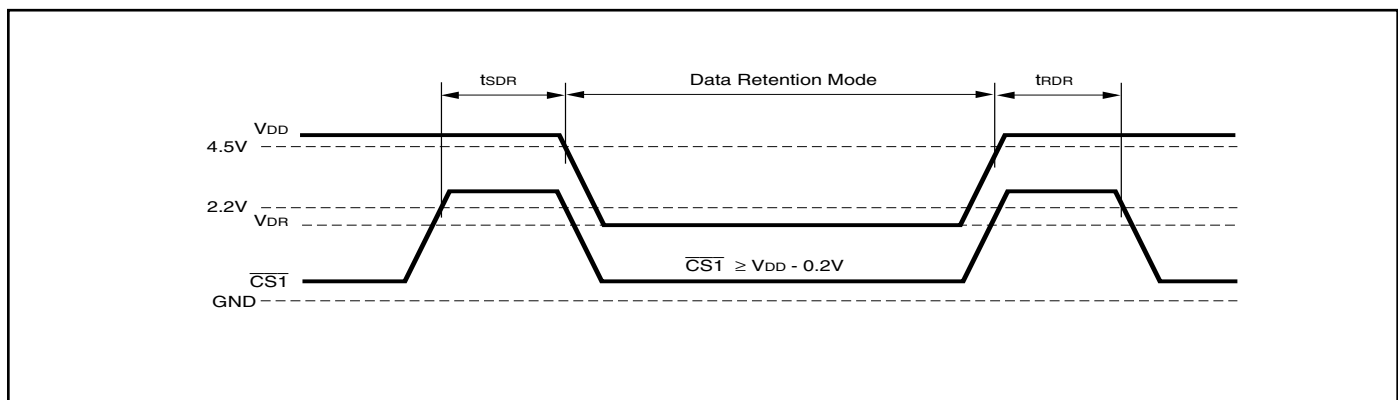
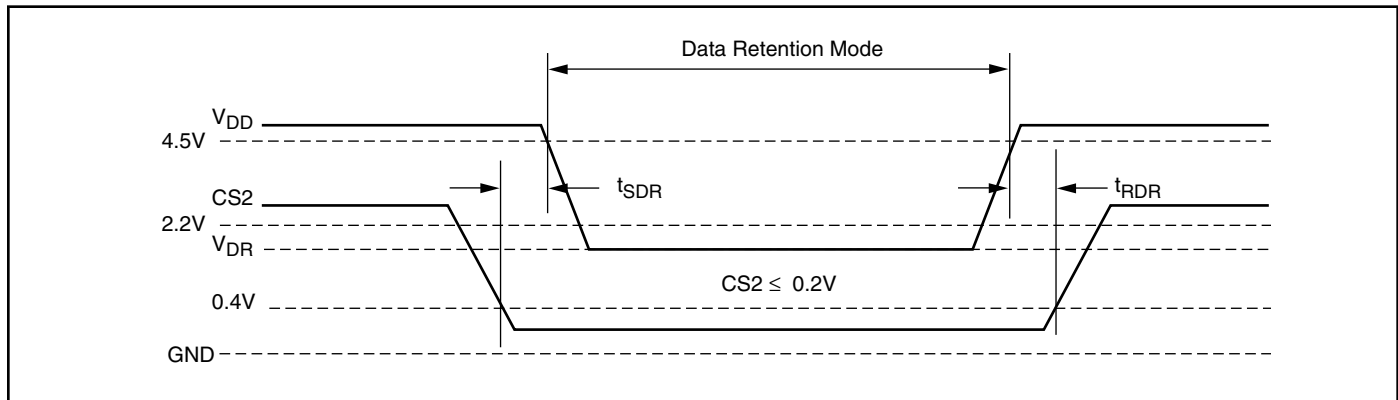


**DATA RETENTION SWITCHING CHARACTERISTICS (4.5V - 5.5V)**

Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{DR}$	$V_{DD}$ for Data Retention	See Data Retention Waveform	2.0		5.5	V
$I_{DR}$	Data Retention Current	$V_{DD} = 2.0V$ and $\overline{CS1} \geq V_{DD} - 0.2V$ and (a) $CS2 \geq V_{DD} - 0.2V$ or (b) $CS2 \leq GND + 0.2V$	—	15	20	$\mu A$
		Com.	—	—	40	
		Ind.	—	—	60	
		Auto.	—	—	180	
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform	0		—	ns
$t_{RDR}$	Recovery Time	See Data Retention Waveform	$t_{RC}$		—	ns

**Note:**

1. Typical Values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$  and not 100% tested.

**DATA RETENTION WAVEFORM ( $\overline{CS1}$  Controlled)**

**DATA RETENTION WAVEFORM (CS2 Controlled)**


## IS62C51216AL, IS65C51216AL

---

### IS62C51216AL (4.5V - 5.5V)

**Industrial Range: -40°C to +85°C**

---

Speed (ns)	Order Part No.*	Package
55	IS62C51216AL-55TLI	TSOP-II, Lead-free
	IS62C51216AL-55MLI	mini BGA, Lead-free (9mmx11mm)

---

\*Devices will meet 45ns when used in 0°C to +70°C temperature range.

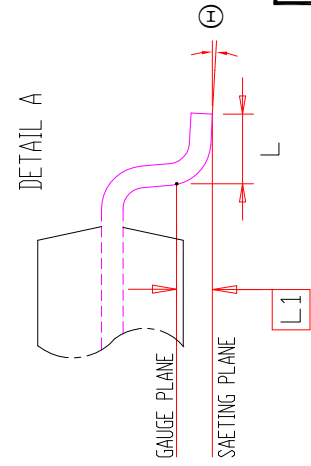
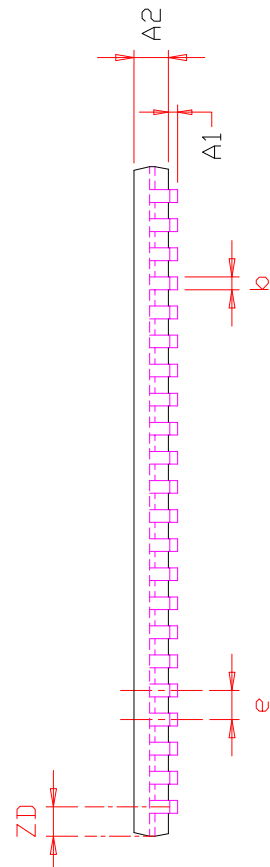
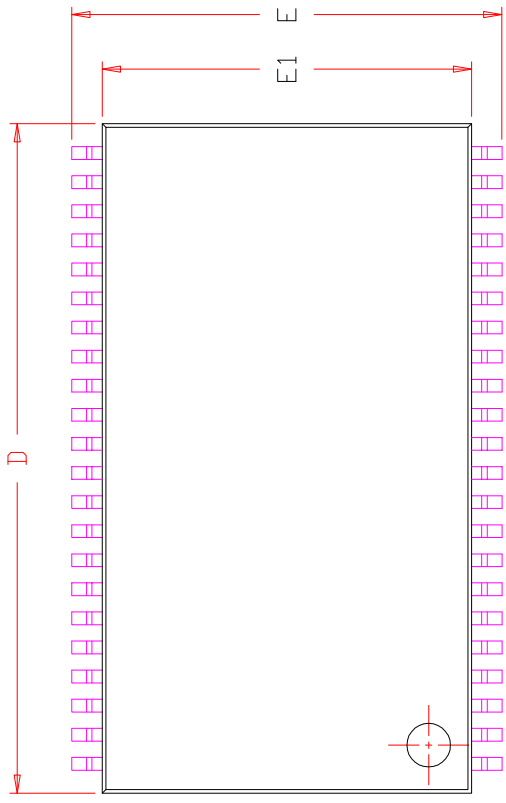
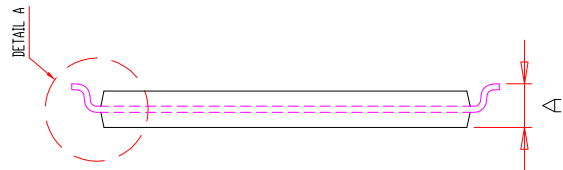
### IS65C51216AL (4.5V - 5.5V)

**Automotive Range: -40°C to +125°C**

---

Speed (ns)	Order Part No.	Package
55	IS65C51216AL-55CTLA3	TSOP-II, Lead-free, Copper Lead-frame
	IS65C51216AL-55MLA3	mini BGA, Lead-free (9mmx11mm)

---



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40		0.69	0.016		0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
⊖	0		8°	0		8°

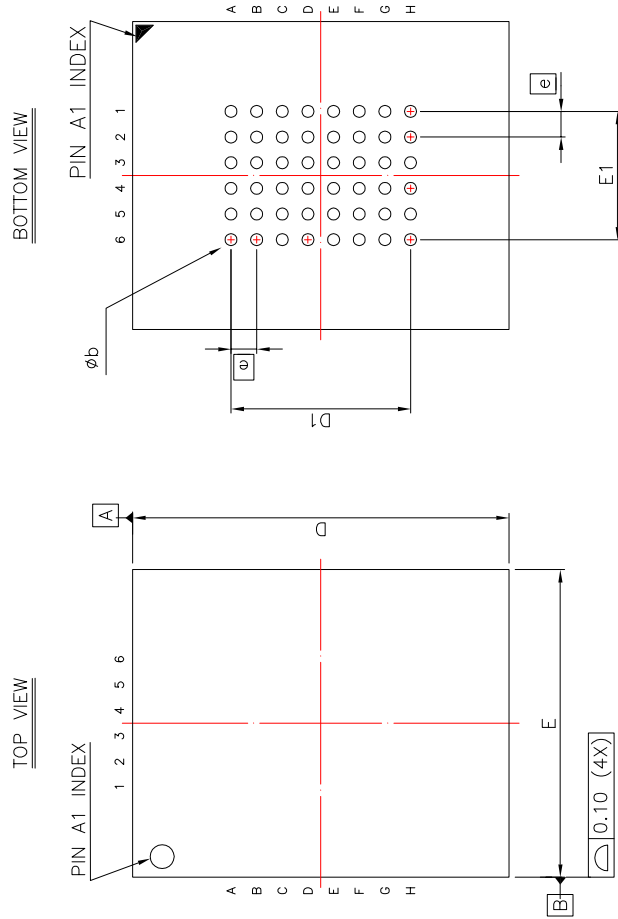
**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



**44L 400mil TSOP-2**  
Package Outline

**REV. F**      **DATE** 06/04/2008



SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
$\phi b$	0.75 BSC			0.030 BSC		

**NOTE :**

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

	TITLE	REV.	DATE
	48L 9x11mm TF-BGA Package Outline	B	08/21/2008



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.