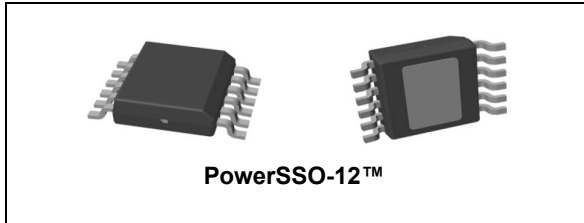


Dual high side smart power solid state relay

Datasheet - production data



Features

- Nominal current: 0.5 A per channel
- Shorted-load protections
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shutdown restart not simultaneous for the various channels
- Protection against loss of ground
- Current limitation 1 A per channel
- Undervoltage shutdown
- Open-load in off-state and short to V_{CC} detection
- Open-drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2

Description

The VNI2140J is a monolithic device designed using STMicroelectronics' VIPower technology. The device drives two independent resistive or inductive loads with one side connected to ground. Active current limitation prevents a drop in system power supply in cases of shorted-load, and built-in thermal shutdown protects the chip from damage due to overtemperature and short-circuit. In overload conditions, channel turns OFF and ON automatically to maintain the junction temperature between TTSD and TR. If the case temperature reaches TCSD, the overloaded channel is turned OFF and restarts only when case temperature decreases down to TCR. In order to avoid high-peak current from the supply, when more than one channel is overloaded the TCSD restart is not simultaneous. Non overloaded channels continue to operate normally. The open-drain diagnostics output indicates overtemperature conditions and open-load in off state.

Table 1. Device summary

| Order codes | Package | Packaging |
|-------------|--------------|---------------|
| VNI2140J | PowerSSO-12™ | Tube |
| VNI2140JTR | | Tape and reel |

Table 2. Main features

| Type | $V_{\text{demag}}^{(1)}$ | $R_{\text{Dson}}^{(1)}$ | $I_{\text{out}}^{(1)}$ | V_{CC} |
|----------|--------------------------------|-------------------------|------------------------|-----------------|
| VNI2140J | $V_{\text{CC}} - 45 \text{ V}$ | 0.08Ω | $1 \text{ A}^{(2)}$ | 45 V |

1. Per channel.

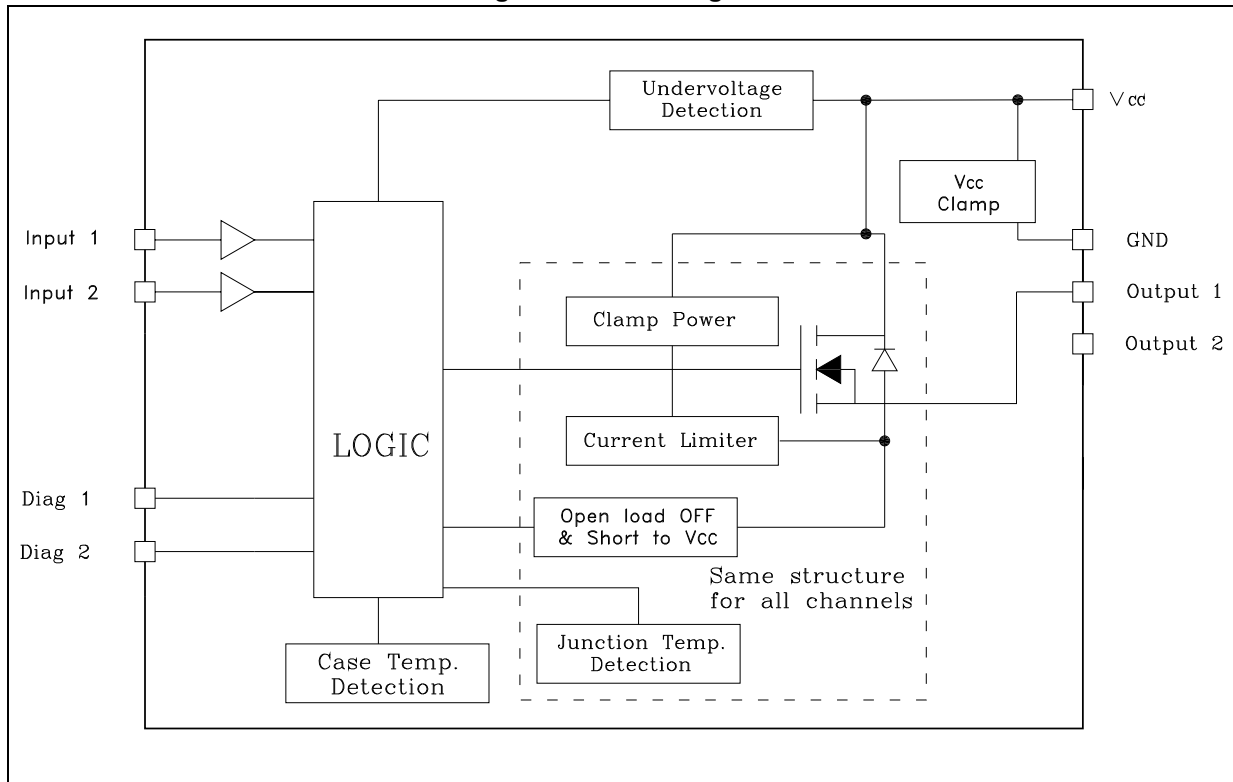
2. Current limitation.

Contents

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1 Block diagram

Figure 1. Block diagram



2 Pin connections

Figure 2. Pin connections (top view)

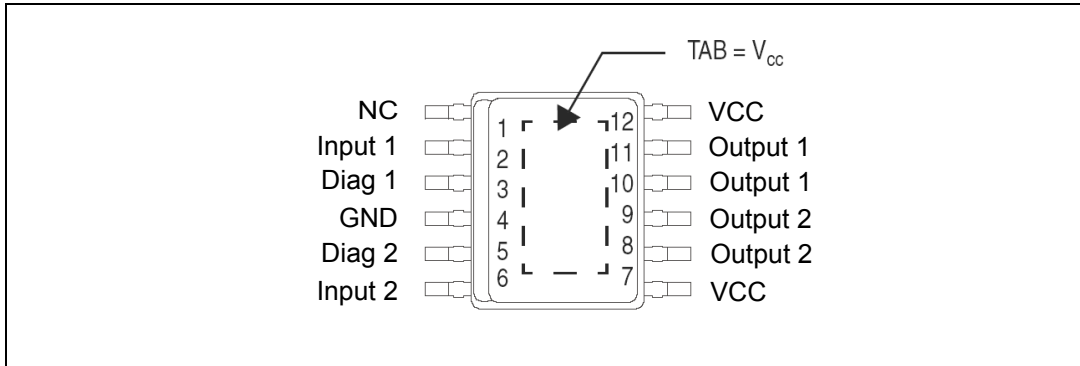


Table 3. Pin description

| No. | Name | Description |
|-----|----------|--|
| 1 | NC | Not connected |
| 2 | Input 1 | Channel 1 input 3.3 V CMOS/TTL compatible |
| 3 | Diag 1 | Channel 1 diagnostic in open-drain configuration |
| 4 | GND | Device ground connection |
| 5 | Diag 2 | Channel 2 diagnostic in open-drain configuration |
| 6 | Input 2 | Channel 2 input 3.3 V CMOS/TTL compatible |
| 7 | VCC | Supply voltage |
| 8 | Output 2 | Channel 2 power stage output, internally protected |
| 9 | Output 2 | Channel 2 power stage output, internally protected |
| 10 | Output 1 | Channel 1 power stage output, internally protected |
| 11 | Output 1 | Channel 1 power stage output, internally protected |
| 12 | VCC | Supply voltage |
| TAB | TAB | Supply voltage |

3 Maximum ratings

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------|---|--------------------|--------------------|
| V_{CC} | Power supply voltage | 45 | V |
| $-V_{CC}$ | Reverse supply voltage | -0.3 | V |
| I_{GND} | DC ground reverse current | -250 | mA |
| I_{OUT} | Output current (continuous) | Internally limited | A |
| I_R | Reverse output current (per channel) | -5 | A |
| I_{IN} | Input current (per channel) | ± 10 | mA |
| V_{IN} | Input voltage | $+V_{CC}$ | V |
| V_{DIAG} | Diag pin voltage | $+V_{CC}$ | V |
| I_{DIAG} | Diag pin current | ± 10 | mA |
| V_{ESD} | Electrostatic discharge (R = 1.5 k Ω ; C = 100 pF) | 2000 | V |
| E_{AS} | Single pulse avalanche energy per channel, all channels driven simultaneously at $T_{amb} = 125\text{ }^{\circ}\text{C}$, $I_{OUT} = 1\text{ A}$ | 300 | mJ |
| P_{TOT} | Power dissipation at $T_c = 25\text{ }^{\circ}\text{C}$ | Internally limited | W |
| T_J | Junction operating temperature | Internally limited | $^{\circ}\text{C}$ |
| T_{STG} | Storage temperature | -55 to 150 | $^{\circ}\text{C}$ |

Thermal data

Table 5. Thermal data

| Symbol | Parameter | Value | Unit |
|--------------|---|---|-----------------------------|
| $R_{th(JC)}$ | Thermal resistance junction to case ⁽¹⁾ | Max. 1 | $^{\circ}\text{C}/\text{W}$ |
| $R_{th(JA)}$ | Thermal resistance junction to ambient ⁽²⁾ | Max. See Figure 11 on page 15 | $^{\circ}\text{C}/\text{W}$ |

1. Per channel.

2. When mounted using minimum recommended pad size on FR-4 board.

4 Electrical characteristics

9 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 6. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------|----------------------------|--|------|------------|-------|----------|
| V _{CC} | Supply voltage | | 9 | - | 45 | V |
| R _{DS(ON)} | On-state resistance | I _{OUT} = 0.5 A at T _J = 25 °C I _{OUT} = 0.5 A | - | 0.080 | 0.150 | Ω Ω |
| V _{CLAMP} | Clamp voltage | I _S = 20 mA | 45 | - | 52 | V |
| I _S | Supply current | All channel in off-state On-state with V _{IN} = 5 V (T _J = 125 °C) | - | 300 1.9 | 4 | μA mA |
| I _{LGND} | Output current at turn-off | V _{CC} = V _{DIAG} = V _{IN} = V _{GND} = 24 V, V _{OUT} = 0 V | - | - | 1 | mA |
| V _{OUT(OFF)} | Off-state output voltage | V _{IN} = 0 V and I _{OUT} = 0 A | - | - | 3 | V |
| I _{OUT(OFF)} | OFF-state output current | V _{IN} = V _{OUT} = 0 V | 0 | - | 5 | μA |
| I _{OUT(OFF1)} | | V _{IN} = 0 V; V _{OUT} = 4 V | -35 | - | 0 | μA |

Table 7. Timing (V_{CC} = 24 V, R_{LOAD} = 48 Ω)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------------------|---------------------------------------|---|------|------|------|------|
| t _{d(ON)} | Turn-on delay time of output current | I _{OUT} = 0.5 A, resistive load Input rise time < 0.1 μs, T _J = 25 °C | - | 8 | - | μs |
| t _r | Rise time of output current | I _{OUT} = 0.5 A, resistive load Input rise time < 0.1 μs, T _J = 25 °C | - | 15 | - | μs |
| t _{d(ON)} + t _r | Turn-on response | I _{OUT} = 0.5 A, resistive load Input rise time < 0.1 μs, T _J = 25 °C | - | - | 35 | μs |
| t _{d(OFF)} | Turn-off delay time of output current | I _{OUT} = 0.5 A, resistive load Input rise time < 0.1 μs, T _J = 25 °C | - | 10 | - | μs |
| t _f | Fall time of output current | I _{OUT} = 0.5 A, resistive load Input rise time < 0.1 μs, T _J = 25 °C | - | 7 | - | μs |
| t _{d(OFF)} + t _f | Turn-off response | I _{OUT} = 0.5 A, resistive load Input rise time < 0.1 μs, T _J = 25 °C | - | - | 40 | μs |
| t _{DOL} | Delay time for open-load detection | - | - | 500 | - | μs |
| dV/dt _(ON) | Turn ON voltage slope | - | - | 3 | - | V/μs |
| dV/dt _(off) | Turn OFF voltage slope | - | - | 4 | - | V/μs |

Table 8. Logical input

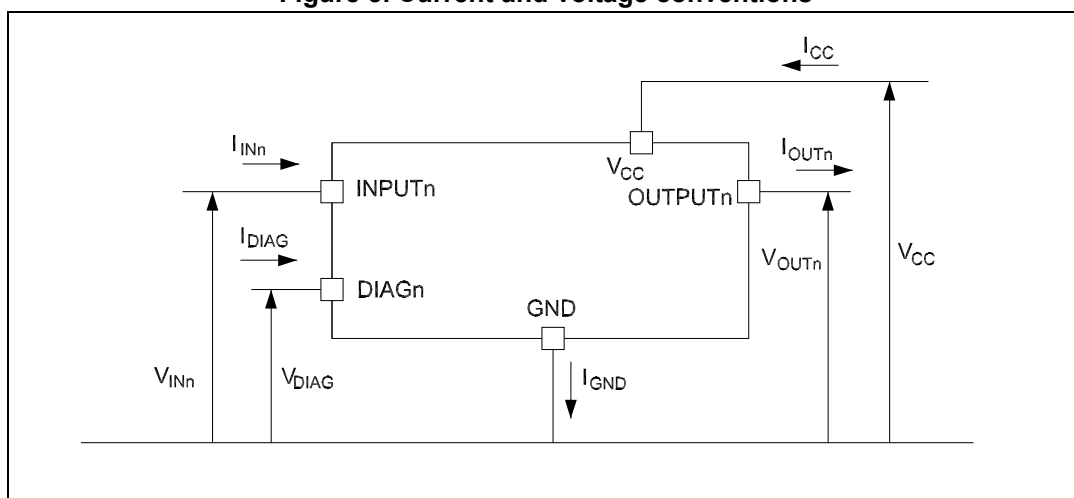
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--------------------------|------------------------|------|------|------|---------------|
| V_{IL} | Input low level voltage | - | - | - | 0.8 | V |
| V_{IH} | Input high level voltage | - | 2.20 | - | - | V |
| $V_{I(HYST)}$ | Input hysteresis voltage | - | - | 0.15 | - | V |
| I_{IN} | Input current | $V_{IN} = 15\text{ V}$ | - | - | 10 | μA |
| | | $V_{IN} = 36\text{ V}$ | - | - | 210 | |

Table 9. Protection and diagnostic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|---|--|---------------|---------------|---------------|--------------------|
| $V_{DIAG}^{(1)}$ | Diag voltage output low | $I_{DIAG} = 1.5\text{ mA}$ (fault condition) | - | - | 0.6 | V |
| V_{USD} | Undervoltage protection | - | 7 | - | 9 | V |
| V_{USDHYS} | Undervoltage hysteresis | - | 0.4 | 0.5 | - | V |
| I_{LIM} | DC short-circuit current | $V_{CC} = 24\text{ V}; R_{LOAD} < 10\text{ m}\Omega$ | 1 | - | 2 | A |
| I_{LDIAG} | Diag leakage current | $V_{CC} = 32\text{ V}$ | - | 30 | - | μA |
| V_{OL} | Open-load off-state voltage detection threshold | $V_{IN} = 0\text{ V}$ | 2 | 3 | 4 | V |
| T_{TSD} | Junction shutdown temperature | - | 150 | 170 | - | $^{\circ}\text{C}$ |
| T_R | Junction reset temperature | - | 135 | 155 | 200 | $^{\circ}\text{C}$ |
| T_{HIST} | Junction thermal hysteresis | - | 7 | 15 | - | $^{\circ}\text{C}$ |
| T_{CSD} | Case shutdown temperature | - | 125 | 130 | 135 | $^{\circ}\text{C}$ |
| T_{CR} | Case reset temperature | - | 110 | - | - | $^{\circ}\text{C}$ |
| T_{CHYST} | Case thermal hysteresis | - | 7 | 15 | - | $^{\circ}\text{C}$ |
| V_{demag} | Output voltage at turn-OFF | $I_{OUT} = 0.5\text{ A}; L_{LOAD} \geq 1\text{ mH}$ | $V_{CC} - 45$ | $V_{CC} - 50$ | $V_{CC} - 52$ | V |

1. Diag determination > 100 ms after the switching edge.

Figure 3. Current and voltage conventions



5 Truth table

Table 10. Truth table

| IC condition | INPUTn | OUTPUTn | DIAGn |
|--------------------------------------|--------|------------------|-------|
| Normal operation | L | L | H |
| | H | H | H |
| Overtemperature | L | L | H |
| | H | L | L |
| Undervoltage | L | L | X |
| | H | L | X |
| Shorted-load (current limitation) | L | L | H |
| | H | X | H |
| Output voltage > V_{OL} | L | Z ⁽¹⁾ | L |
| | H | H | H |
| Short to V_{CC} | L | H | L |
| | H | H | H |

1. Z = depending on the external circuit.

6 Switching waveforms

Figure 4. Switching waveforms

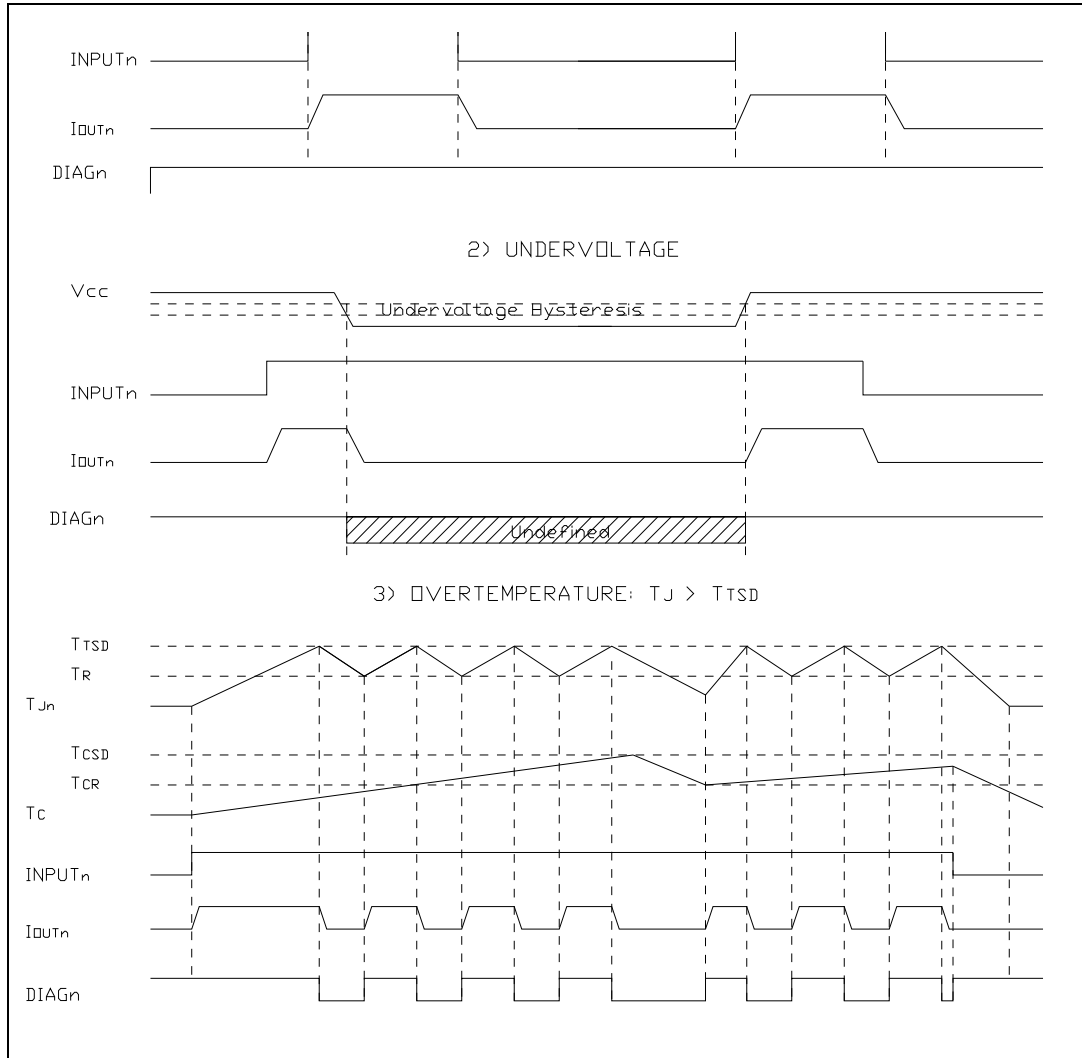


Figure 5. Switching waveforms (continued)

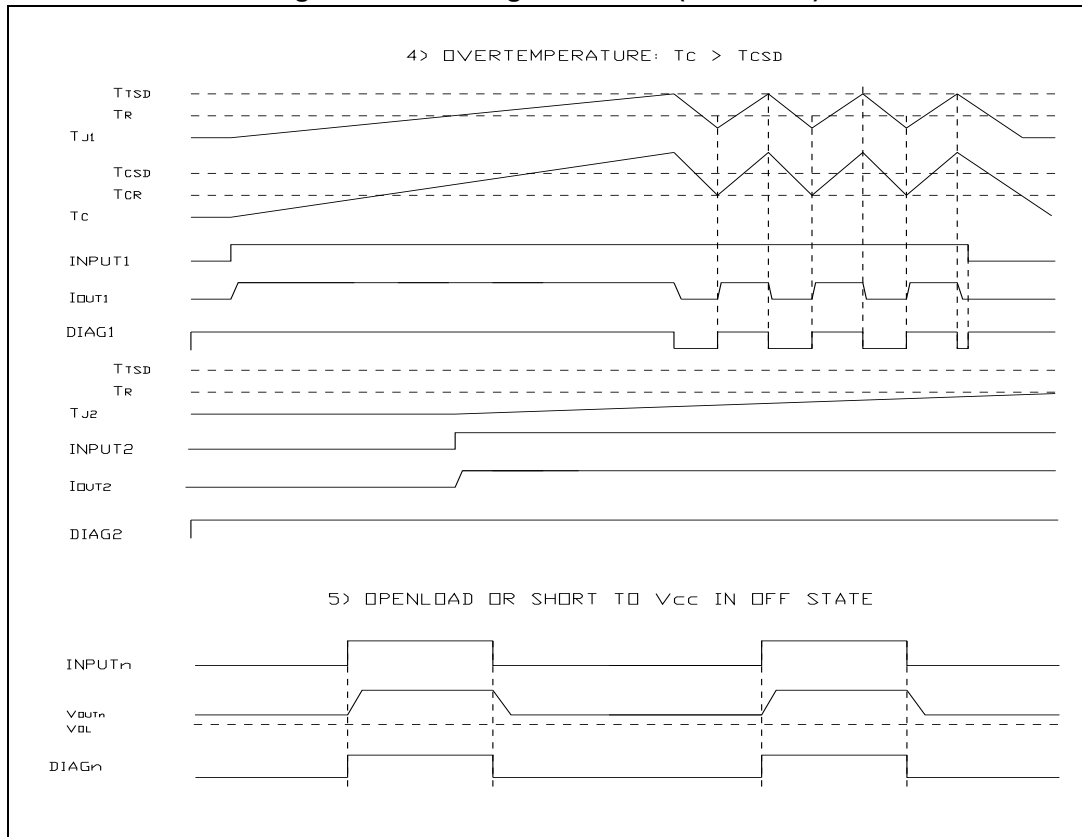


Figure 6. Switching parameter test conditions

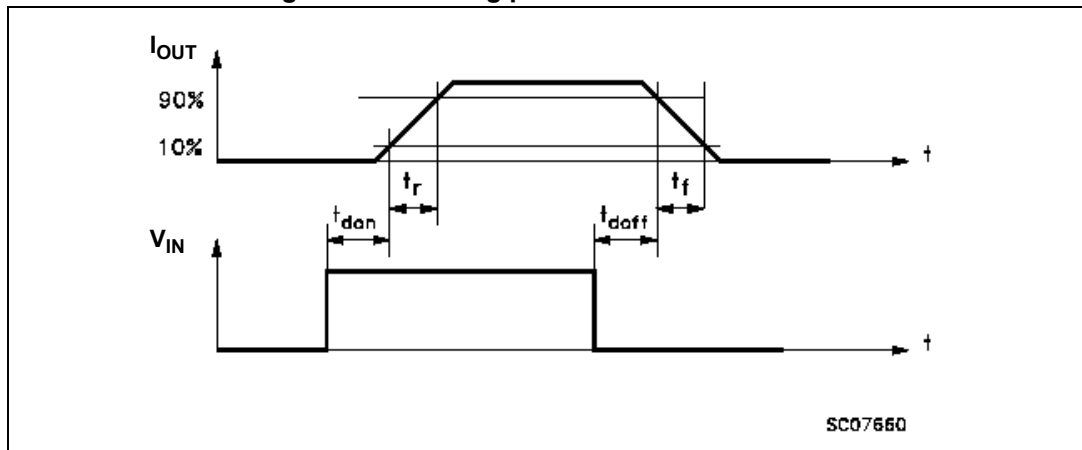
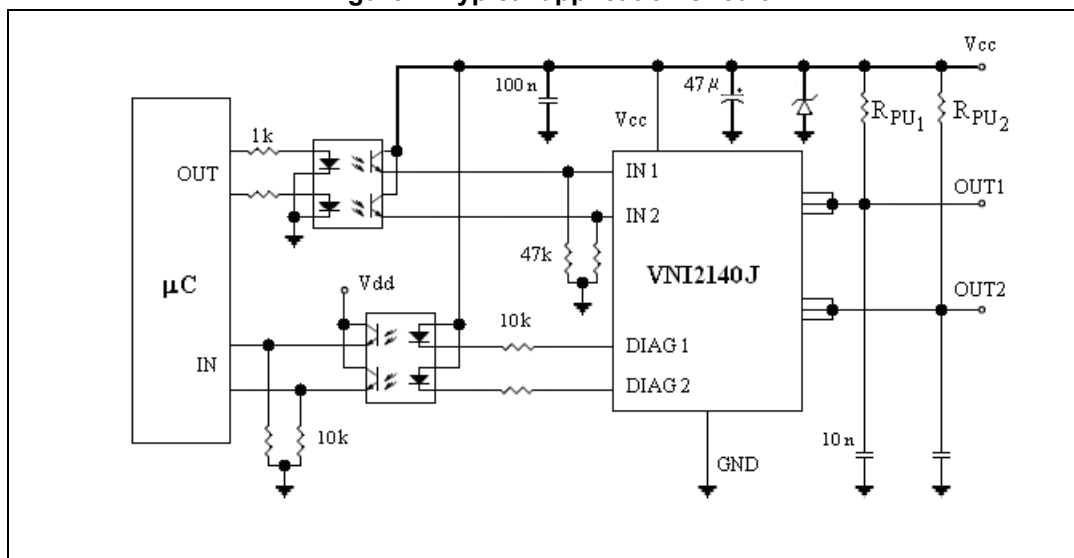


Figure 7. Typical application circuit



7 Open-load

In order to detect the open-load fault a pull-up resistor must be connected between the V_{CC} line and the output pin.

In a normal condition a current flows through the network made up of a pull-up resistor and a load. The voltage across the load is less than V_{OLMIN} ; so the diag pin is kept high.

This is the result in the condition:

Equation 1

$$V_{CC} \frac{R_{LOAD}}{R_{LOAD} + R_{PU}} < V_{OLMIN}$$

or

Equation 2

$$\left(\frac{V_{CC}}{V_{OLMIN}} - 1 \right) \cdot R_{LOAD} < R_{PU}$$

When a open-load event occurs the voltage on the output pin rises to a value higher than V_{OLMAX} (depending on the pull-up resistor). The diag pin will go down.

This result in the condition:

Equation 3

$$R_{PU} < \frac{V_{CC} - V_{OLMAX}}{|I_{OUT(OFF1)MIN}|}$$

Figure 8. Open-load detection

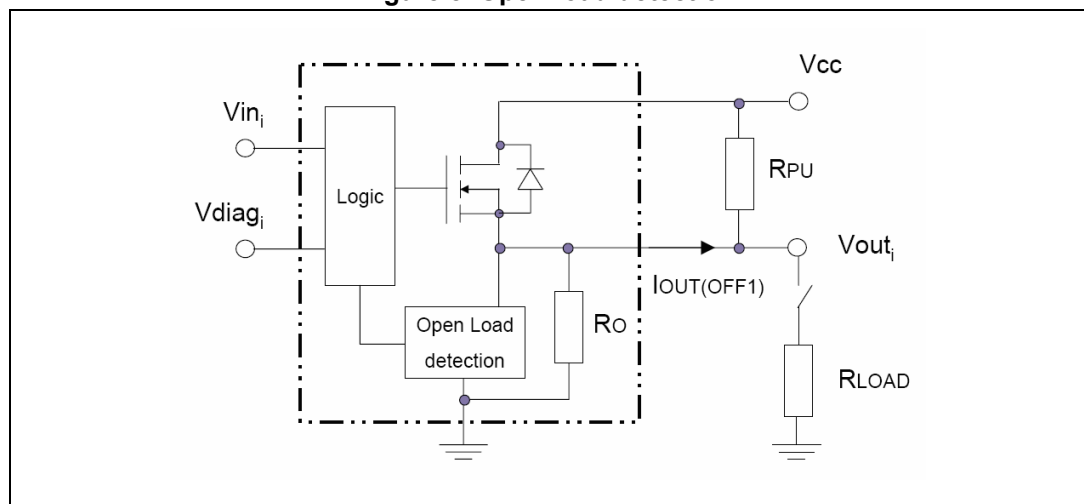
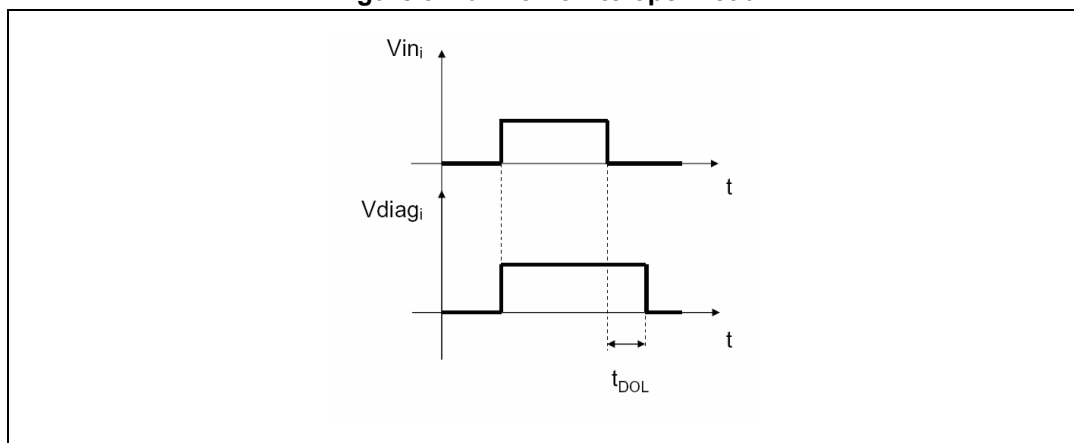


Figure 9. Turn-on/off to open-load



8 Package and PCB thermal data

Figure 10. PowerSSO-12 PC board

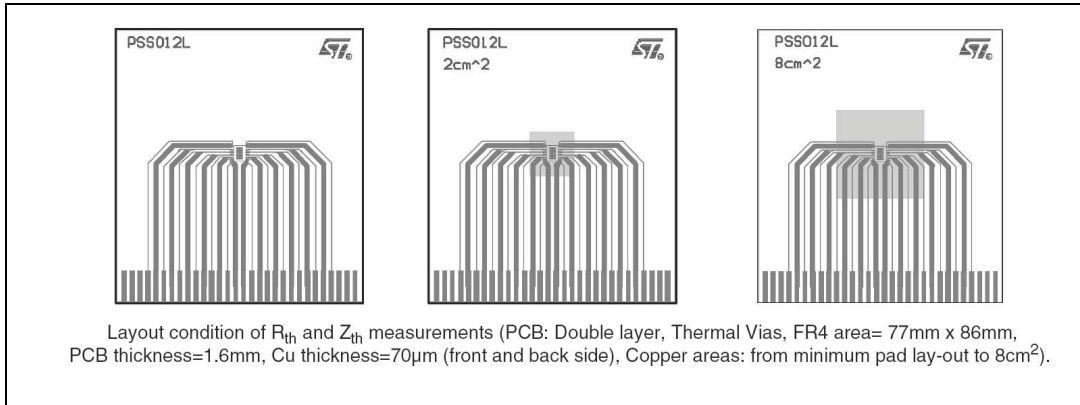


Figure 11. R_{thJA} vs PCB copper area in open box free air condition

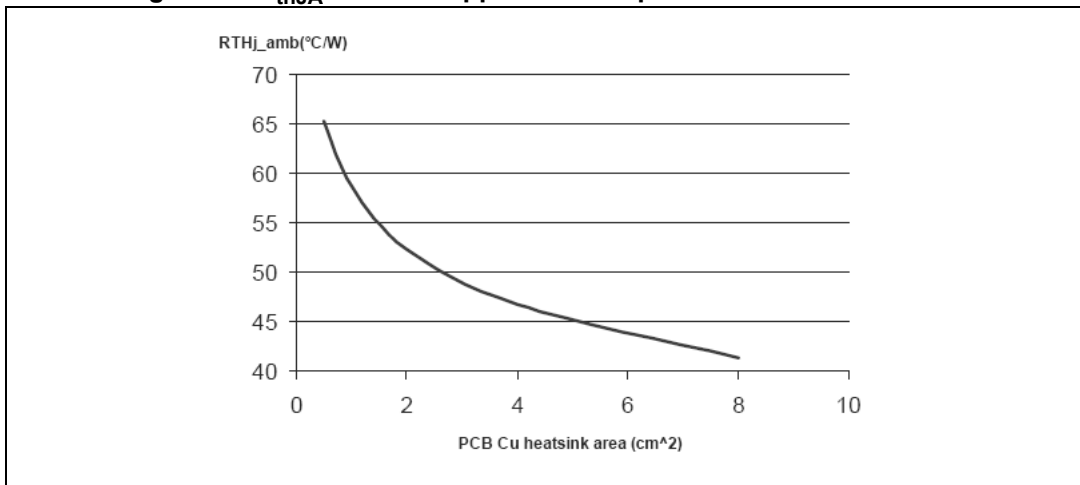
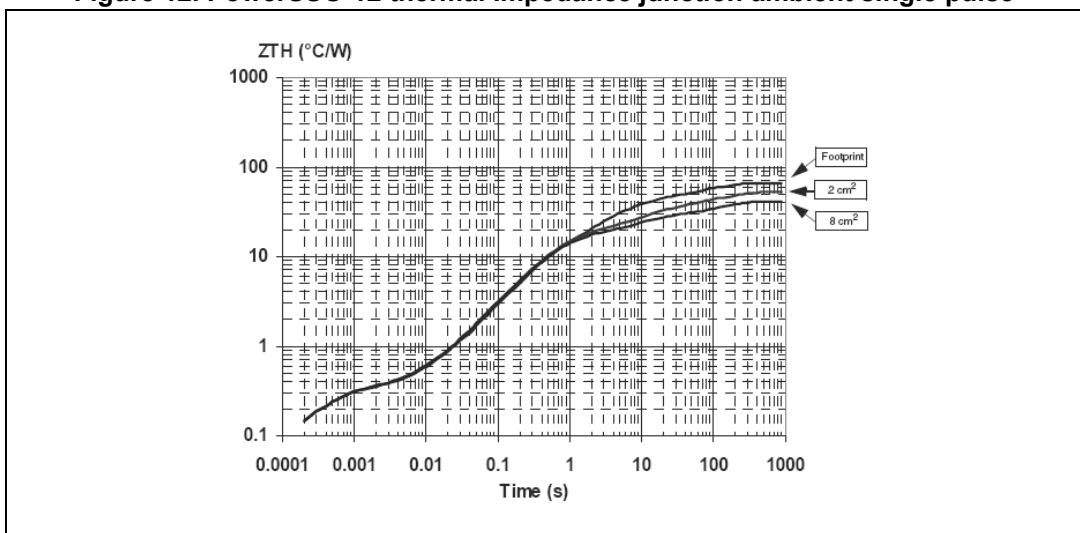


Figure 12. PowerSSO-12 thermal Impedance junction ambient single pulse



Pulse calculation formula

Equation 4

$$Z_{TH\delta} = R_{TH} \times \delta + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 13. Thermal fitting model of a double channel HSD in PowerSSO-12

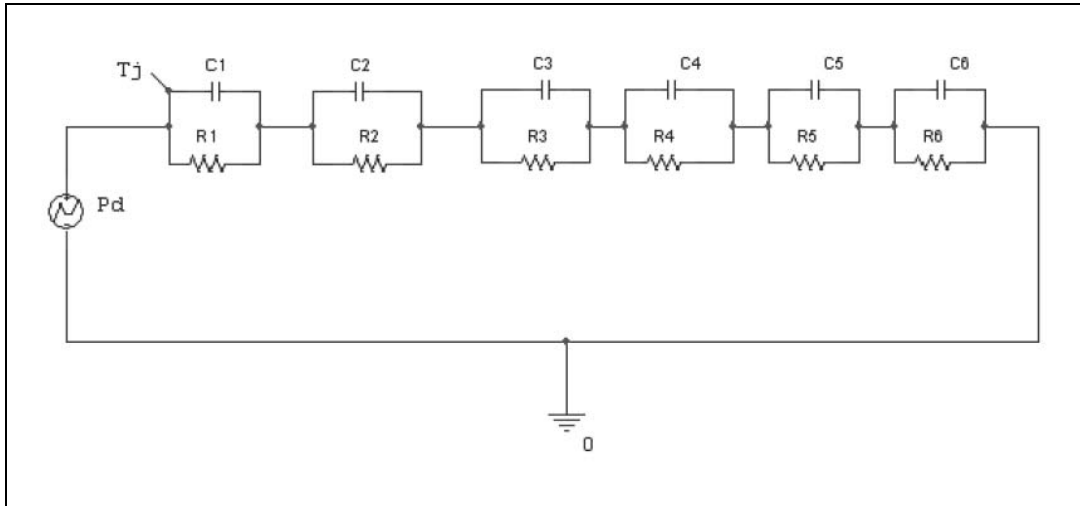


Table 11. Thermal parameter

| Area/island (cm ²) | Footprint | 2 | 8 |
|--------------------------------|-----------|-----|-----|
| R1 (°C/W) | 0.1 | - | - |
| R2 (°C/W) | 0.2 | - | - |
| R3 (°C/W) | 7 | - | - |
| R4 (°C/W) | 10 | 10 | 9 |
| R5 (°C/W) | 22 | 15 | 10 |
| R6 (°C/W) | 26 | 20 | 15 |
| C1 (W.s/°C) | 0.0001 | - | - |
| C2 (W.s/°C) | 0.002 | - | - |
| C3 (W.s/°C) | 0.05 | - | - |
| C4 (W.s/°C) | 0.2 | 0.1 | 0.1 |
| C5 (W.s/°C) | 0.27 | 0.8 | 1 |
| C6 (W.s/°C) | 3 | 6 | 9 |

9 Reverse polarity protection

This schematic in [Figure 14](#) can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

Equation 5

$$R_{GND} = (-V_{CC}) / (-I_{GND})$$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

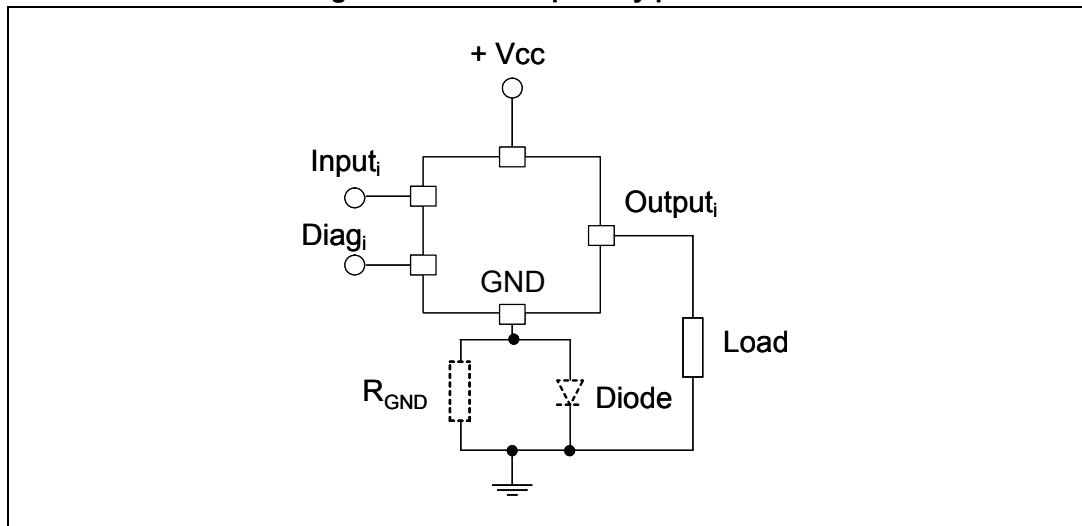
Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse polarity situations) is:

Equation 6

$$PD = (-V_{CC})^2 / R_{GND}$$

Note: In normal condition (no reverse polarity) due to the diode there will be a voltage drop between GND of the device and GND of the system.

Figure 14. Reverse polarity protection



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 PowerSSO-12™ package information

Figure 15. PowerSSO-12™ package outline

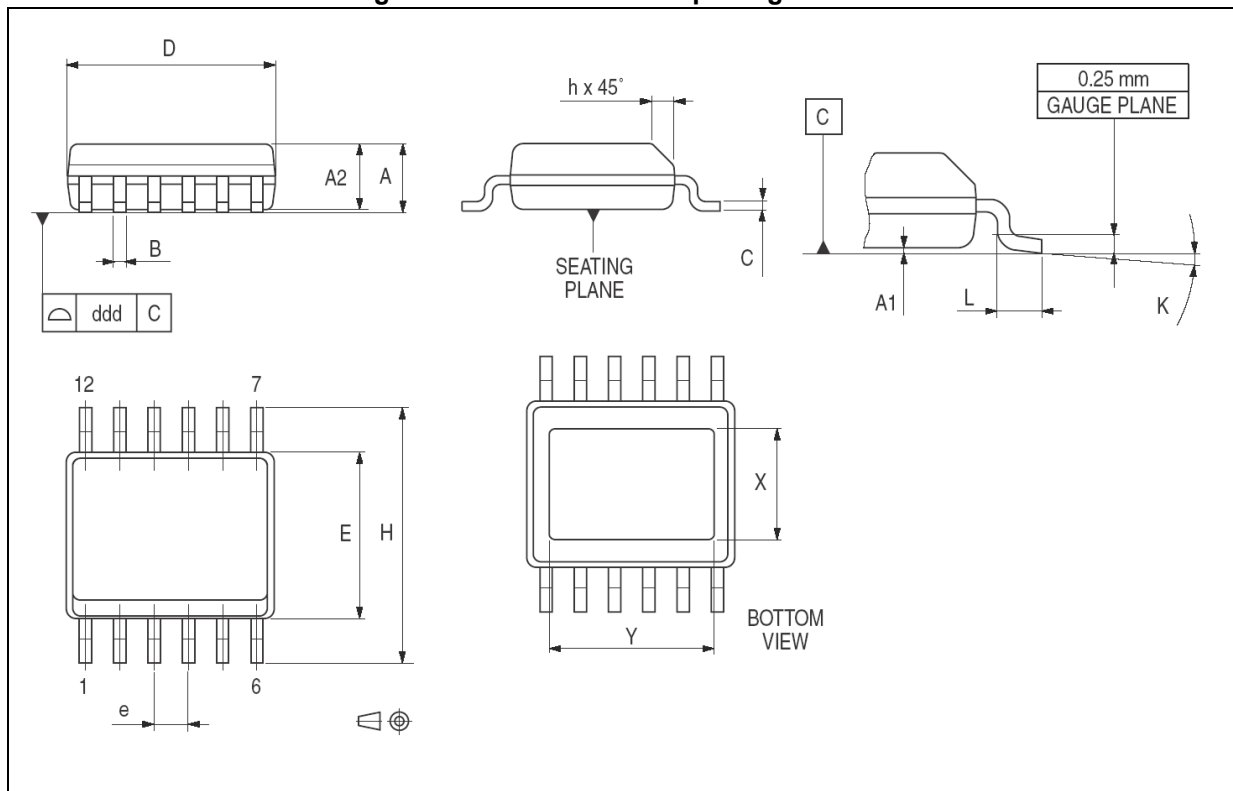


Table 12. PowerSSO-12™ mechanical data

| Symbol | Dimensions (mm) | | |
|--------|-----------------|-------|-------|
| | Min. | Typ. | Max. |
| A | 1.250 | - | 1.620 |
| A1 | 0.000 | - | 0.100 |
| A2 | 1.100 | - | 1.650 |
| B | 0.230 | - | 0.410 |
| C | 0.190 | - | 0.250 |
| D | 4.800 | - | 5.000 |
| E | 3.800 | - | 4.000 |
| e | - | 0.800 | - |
| H | 5.800 | - | 6.200 |
| h | 0.250 | - | 0.500 |
| L | 0.400 | - | 1.270 |
| k | 0° | - | 8° |
| X | 1.900 | - | 2.500 |
| Y | 3.600 | - | 4.200 |
| ddd | - | - | 0.100 |

Figure 16. PowerSSO-12™ tube shipment (no suffix)

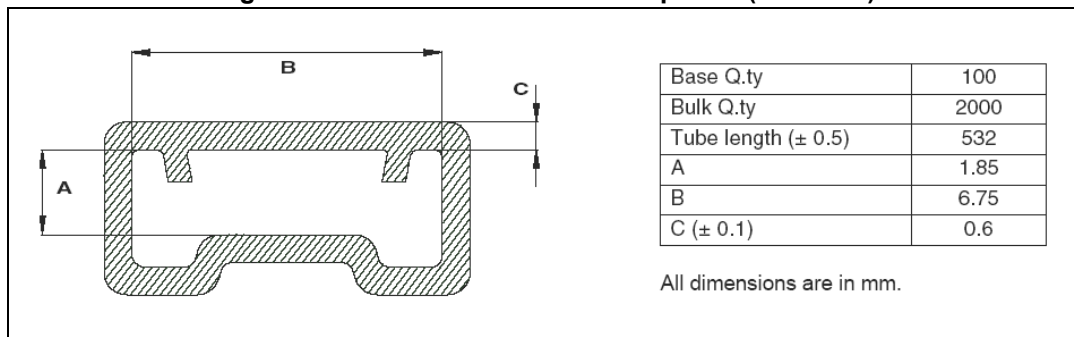


Figure 17. PowerSSO-12™ tape and reel shipment (suffix “TR”)

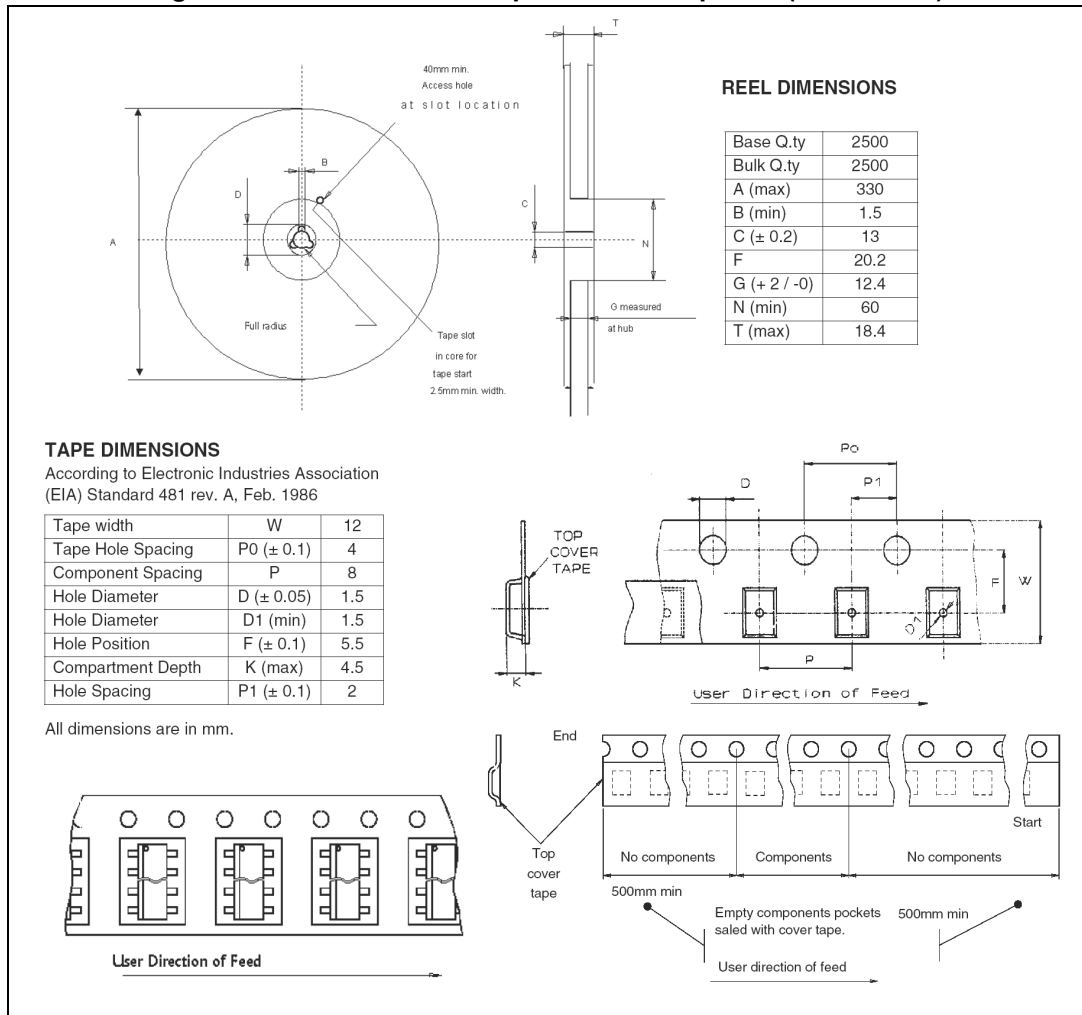
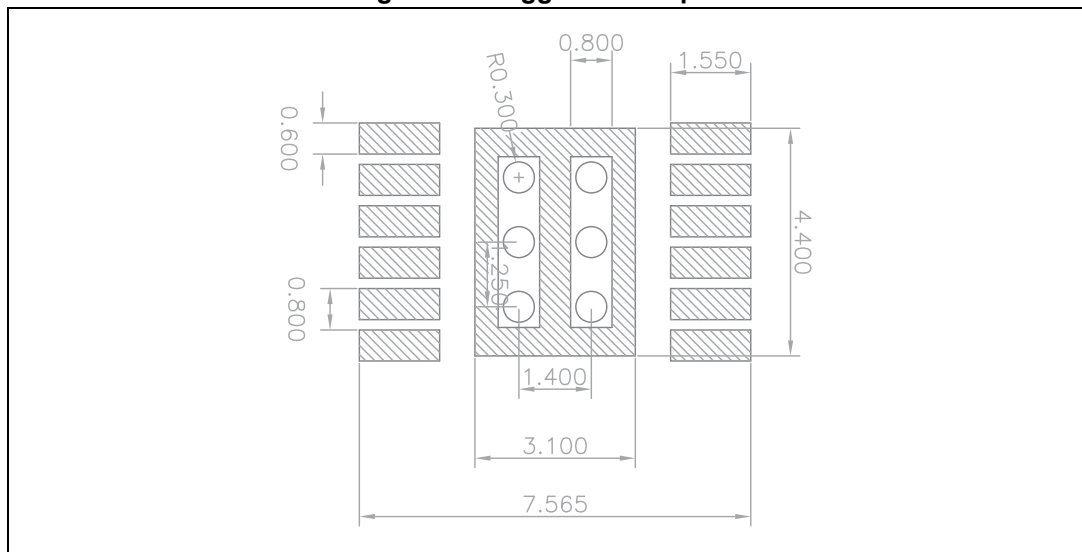


Figure 18. Suggested footprint



11 Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 16-Dec-2008 | 1 | Initial release |
| 29-Apr-2009 | 2 | Updated <i>Table 5 on page 6</i> |
| 03-Jul-2009 | 3 | Updated features in coverpage and <i>Table 5 on page 6</i> |
| 27-Aug-2009 | 4 | Updated <i>Section 9: Reverse polarity protection</i> |
| 25-Mar-2010 | 5 | Updated Coverpage and <i>Table 4 on page 5</i> |
| 26-Apr-2010 | 6 | Updated <i>Table 5 on page 6</i> |
| 21-Jul-2010 | 7 | Updated <i>Table 8 on page 7</i> |
| 15-Nov-2011 | 8 | Updated <i>Figure 18 on page 21</i> |
| 09-Nov-2017 | 9 | Updated <i>Table 4 on page 5</i> and <i>Table 7 on page 6</i> . Minor modifications throughout document. |

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