



LC75811E, 75811W

1/8 to 1/10 Duty Dot Matrix LCD Display Controller/Driver



Overview

The LC75811E and LC75811W are 1/8 to 1/10 duty dot matrix LCD display controller/drivers that supports the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75811E and LC75811W also provide on-chip character display ROM and RAM to allow display systems to be implemented easily.

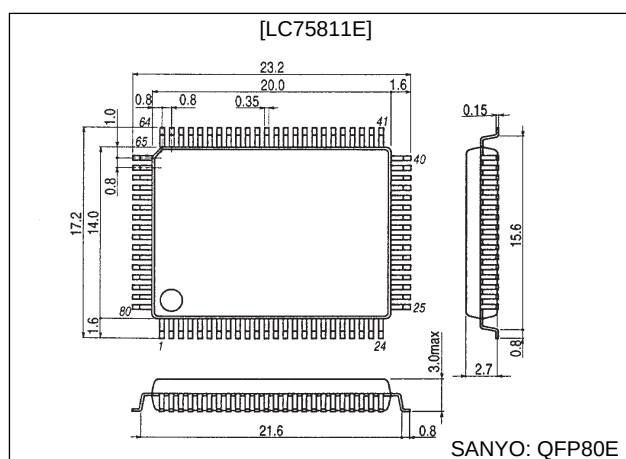
Features

- Controls and drives a 5×7 , 5×8 , or 5×9 dot matrix LCD.
- Supports accessory display segment drive (up to 60 segments)
- Display technique: 1/8 duty 1/4 bias drive (5×7 dots)
1/9 duty 1/4 bias drive (5×8 dots)
1/10 duty 1/4 bias drive (5×9 dots)
- Display digits: 12 digits $\times$ 1 line (5×7 dots),
11 digits $\times$ 1 line (5×8 or 5×9 dots)
- Display control memory
CGROM: 240 characters (5×7 , 5×8 , or 5×9 dots)
CGRAM: 16 characters (5×7 , 5×8 , or 5×9 dots)
ADRAM: 12×5 bits
DCRAM: 48×8 bits
- Instruction function
Display on/off control
Display shift function
- Provides a backup function based on low power modes.
- Serial data input supports CCB format communication with the system controller.
- Independent LCD drive block power supply VLCD
- Provides a RES pin for LSI internal initialization
- RC oscillator circuit

Package Dimensions

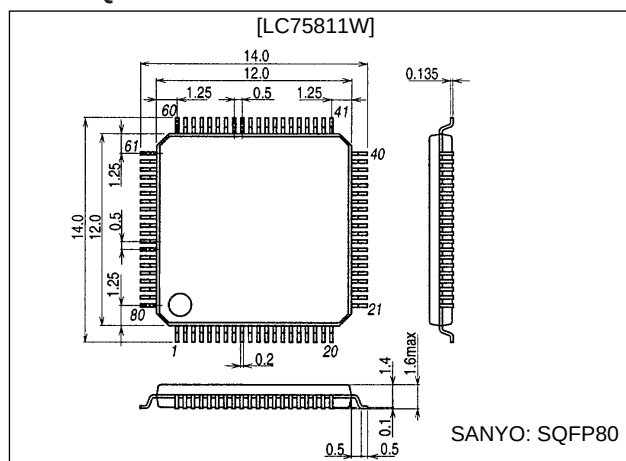
unit: mm

3174-QFP80E



unit: mm

3220-SQFP80



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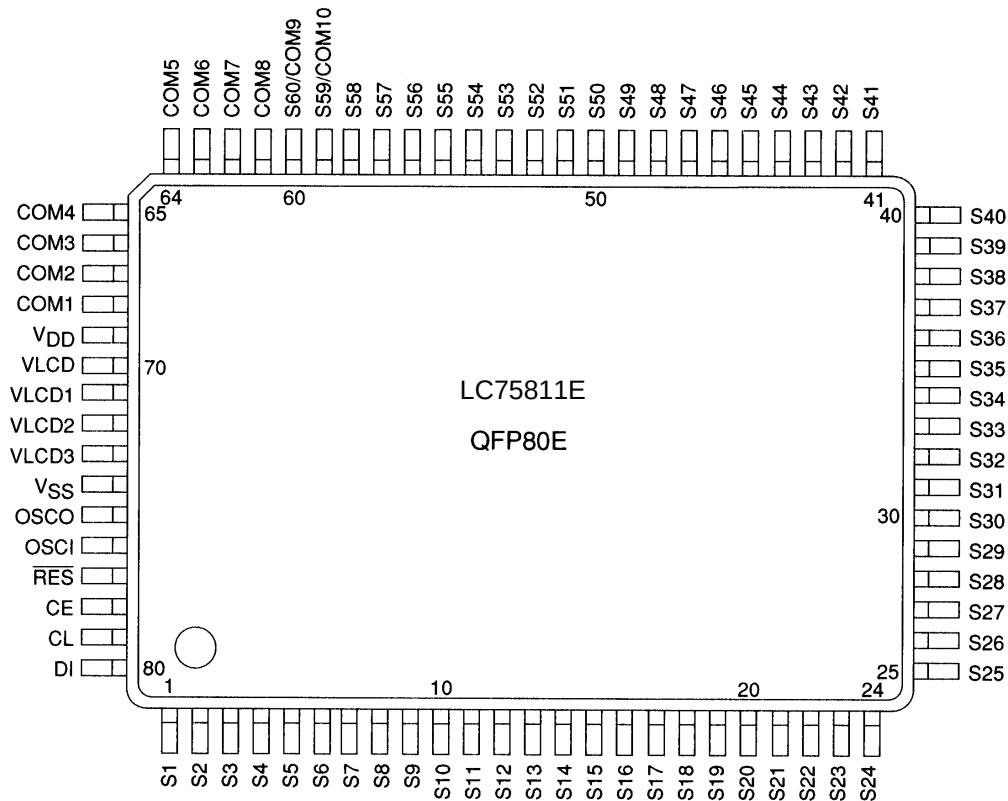
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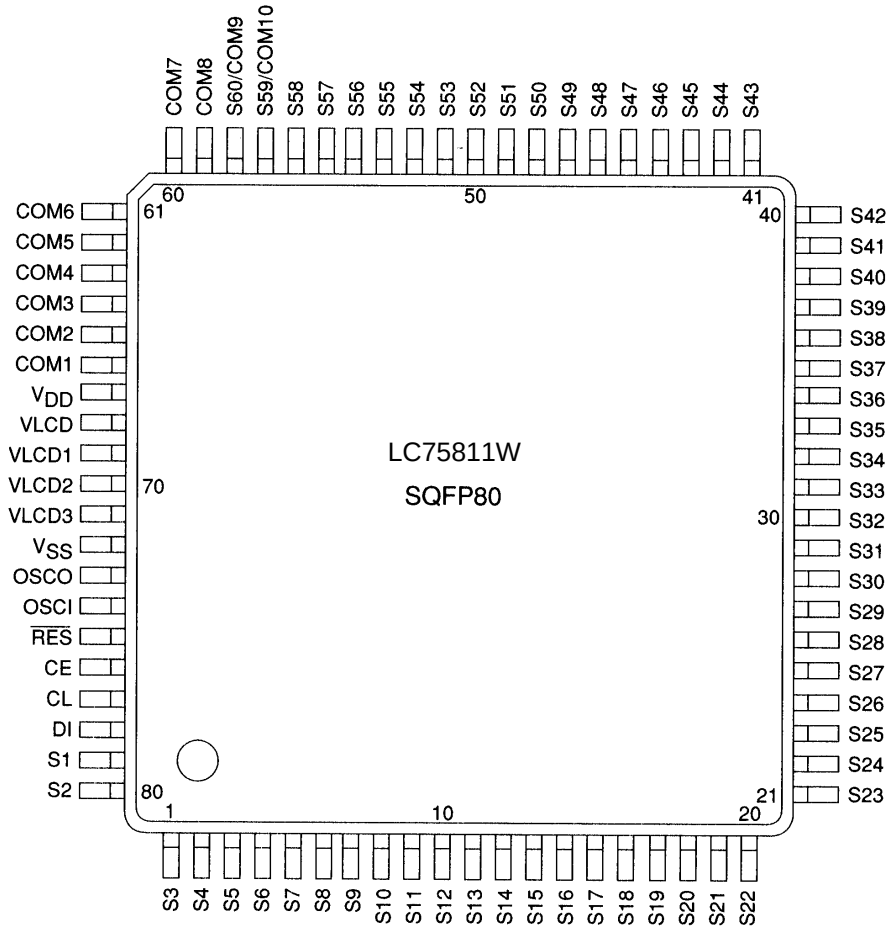
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LC75811E, 75811W

Pin Assignments (Top View)



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD}	-0.3 to +7.0	V
	$V_{LCD\text{ max}}$	V_{LCD}	-0.3 to +11.0	V
Input voltage	V_{IN1}	CE, CL, DI, $\overline{\text{RES}}$	-0.3 to +7.0	V
	V_{IN2}	OSCI	-0.3 to $V_{DD} + 0.3$	V
	V_{IN3}	V_{LCD1} , V_{LCD2} , V_{LCD3}	-0.3 to $V_{LCD} + 0.3$	V
Output voltage	V_{OUT1}	OSCO	-0.3 to $V_{DD} + 0.3$	V
	V_{OUT2}	S1 to S60, COM1 to COM10	-0.3 to $V_{LCD} + 0.3$	V
Output current	I_{OUT1}	S1 to S60	300	μA
	I_{OUT2}	COM1 to COM10	3	mA
Allowable power dissipation	$P_{d\text{ max}}$	$T_a = 85^\circ\text{C}$	200	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$

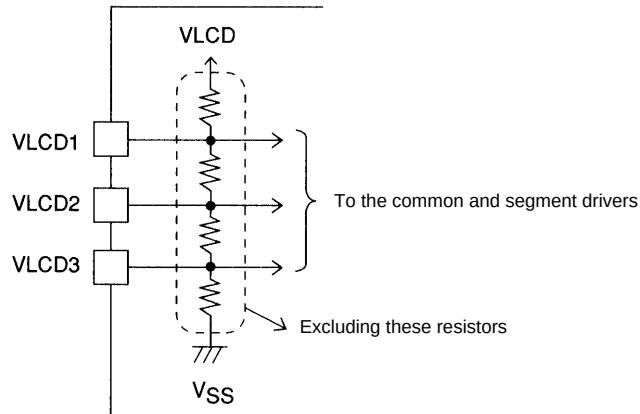
Allowable Operating Ranges at $T_a = -40$ to 85°C , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}	4.5		10.0	V
Input voltage	V_{LCD1}	V_{LCD1}		$3/4 V_{LCD}$	V_{LCD}	V
	V_{LCD2}	V_{LCD2}		$2/4 V_{LCD}$	V_{LCD}	V
	V_{LCD3}	V_{LCD3}		$1/4 V_{LCD}$	V_{LCD}	V
Input high level voltage	V_{IH1}	CE, CL, DI, $\overline{\text{RES}}$	$0.8 V_{DD}$		6.0	V
	V_{IH2}	OSCI	$0.7 V_{DD}$		V_{DD}	V
Input low level voltage	V_{IL1}	CE, CL, DI, $\overline{\text{RES}}$	0		$0.2 V_{DD}$	V
	V_{IL2}	OSCI	0		$0.3 V_{DD}$	V
Recommended external resistance	R_{OSC}	OSCI, OSCO		33		$\text{k}\Omega$
Recommended external capacitance	C_{OSC}	OSCI, OSCO		220		pF
Guaranteed oscillation range	f_{OSC}	OSC	150	300	600	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2	160			ns
High level clock pulse width	$t_{\theta H}$	CL: Figure 2	160			ns
Low level clock pulse width	$t_{\theta L}$	CL: Figure 2	160			ns
Minimum reset pulse width	t_{WRES}	$\overline{\text{RES}}$: Figure 3	1			μs

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{RES}$		$0.1 V_{DD}$		V
Input high level current	I_{IH}	CE, CL, DI, $\overline{RES}$, OSCI: $V_I = 6.0$ V			5.0	μA
Input low level current	I_{IL}	CE, CL, DI, $\overline{RES}$, OSCI: $V_I = 0$ V	-5.0			μA
Output high level voltage	V_{OH1}	S1 to S60: $I_O = -20 \mu A$	$V_{LCD} - 0.6$			V
	V_{OH2}	COM1 to COM10: $I_O = -100 \mu A$	$V_{LCD} - 0.6$			V
	V_{OH3}	OSCO: $I_O = -500 \mu A$	$V_{DD} - 1.0$			V
Output low level voltage	V_{OL1}	S1 to S60: $I_O = 20 \mu A$			0.6	V
	V_{OL2}	COM1 to COM10: $I_O = 100 \mu A$			0.6	V
	V_{OL3}	OSCO: $I_O = 500 \mu A$			1.0	V
Output middle level voltage*1	V_{MID1}	S1 to S60: $I_O = \pm 20 \mu A$	$2/4 V_{LCD} - 0.6$		$2/4 V_{LCD} + 0.6$	V
	V_{MID2}	COM1 to COM10: $I_O = \pm 100 \mu A$	$3/4 V_{LCD} - 0.6$		$3/4 V_{LCD} + 0.6$	V
	V_{MID3}	COM1 to COM10: $I_O = \pm 100 \mu A$	$1/4 V_{LCD} - 0.6$		$1/4 V_{LCD} + 0.6$	V
Oscillator frequency	f_{OSC}	OSCI, OSCO: $R_{OSC} = 33 k\Omega$, $C_{OSC} = 220 pF$	210	300	390	kHz
Current drain	I_{DD1}	V_{DD} : power saving mode			5	μA
	I_{DD2}	V_{DD} : $V_{DD} = 6.0$ V, output open, $f_{OSC} = 300$ kHz		450	900	μA
	I_{LCD1}	V_{LCD} : power saving mode			5	μA
	I_{LCD2}	V_{LCD} : $V_{LCD} = 10.0$ V, output open, $f_{OSC} = 300$ kHz		200	400	μA

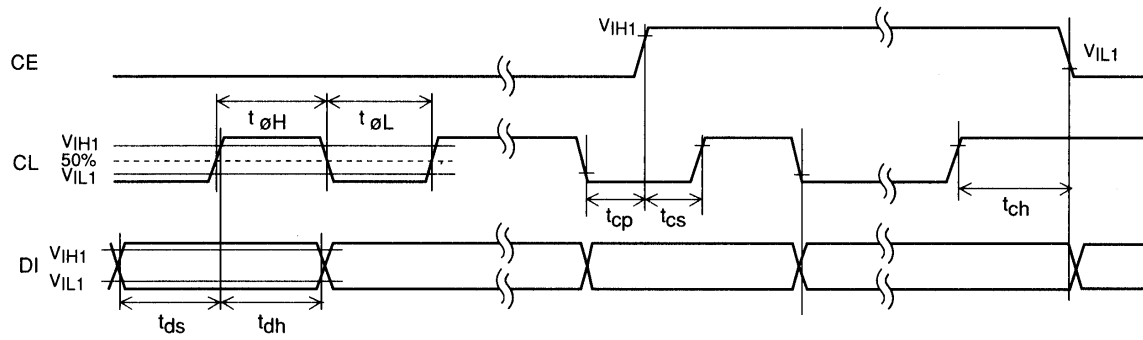
Note *1: Excluding the bias voltage generation divider resistor built into the V_{LCD1} , V_{LCD2} , and V_{LCD3} . (See figure 1.)



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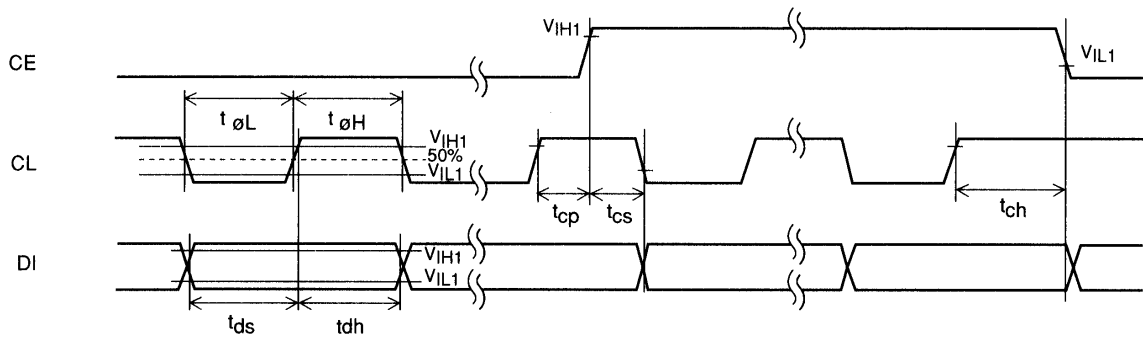
Figure 1

- When CL is stopped at the low level



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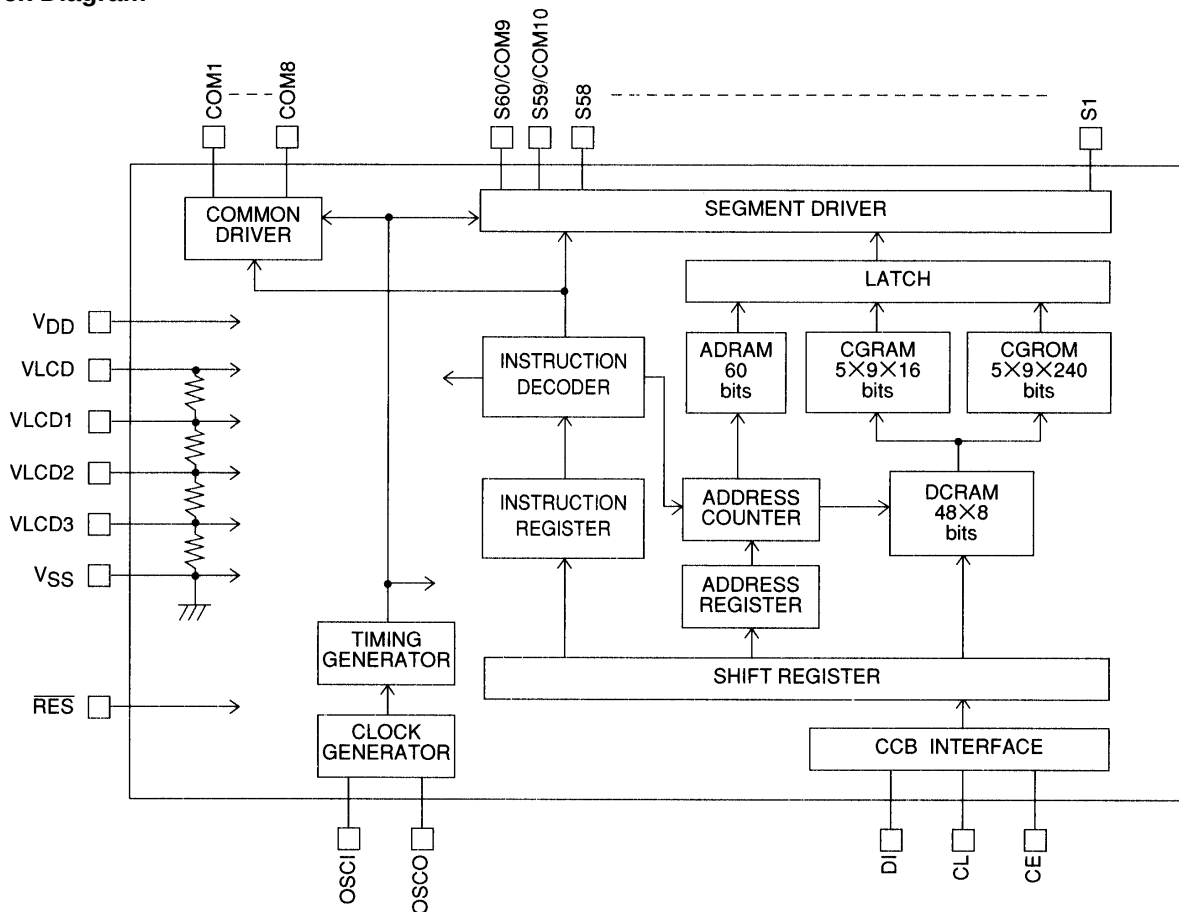
- When CL is stopped at the high level



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Figure 2

Block Diagram



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LC75811E, 75811W

Pin Functions

Pin	Pin No.		Function	Active	I/O	Handling when unused
	LC75811E	LC75811W				
S1 to S58 S59/COM10 S60/COM9	1 to 58 59 60	79, 80 1 to 56 57 58	Segment driver outputs. The S59/COM10 and S60/COM9 pins can be used as common driver outputs under the "set display technique" instruction.	—	O	OPEN
COM1 to COM8	68 to 61	66 to 59	Common driver outputs.	—	O	OPEN
OSCI	76	74	Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor at these pins.	—	I	GND
OSCO	75	73		—	O	OPEN
CE	78	76	Serial data transfer inputs. These pins are connected to the microcontroller. CE: Chip enable CL: Synchronization clock DI: Transfer data	H	I	GND
CL	79	77			I	
DI	80	78		—	I	
$\overline{\text{RES}}$	77	75	Reset signal input. • When $\overline{\text{RES}}$ is low (V_{SS}): • Display off S1 to S58 = "L" (V_{SS}). S59/COM10 and S60/COM9 = "L" (V_{SS}). COM1 to COM8 = "L" (V_{SS}). • Serial data transfer is disabled. • The OSCI/OSCO pin oscillator is stopped. • When $\overline{\text{RES}}$ is high (V_{DD}): • Display on after a "display on/off control" (display on state setting) instruction is executed. • Serial data transfers are enabled. • The OSCI/OSCO pin oscillator operates.	L	I	GND
V_{LCD1}	71	69	Used for applying the LCD drive 3/4 bias voltage externally.	—	I	OPEN
V_{LCD2}	72	70	Used for applying the LCD drive 2/4 bias voltage externally.	—	I	OPEN
V_{LCD3}	73	71	Used for applying the LCD drive 1/4 bias voltage externally.	—	I	OPEN
V_{DD}	69	67	Logic block power supply connection. Provide a voltage of between 2.7 and 6.0 V.	—	—	—
V_{LCD}	70	68	LCD driver block power supply connection. Provide a voltage of between 4.5 and 10.0 V.	—	—	—
V_{SS}	74	72	Power supply connection. Connect to ground.	—	—	—

- ADRAM (Additional data RAM)

ADRAM is RAM used to store the ADATA display data. ADRAM has a capacity of 12×5 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM. The table below lists the correspondence between the 4-bit ADRAM address loaded into AC and the display position on the LCD panel.

- When the ADRAM address loaded into AC is 0_H . (Number of digit displayed: 12)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12
ADRAM address (hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B

However, when the display shift is performed by specifying ADATA, the ADRAM address shifts as shown below.

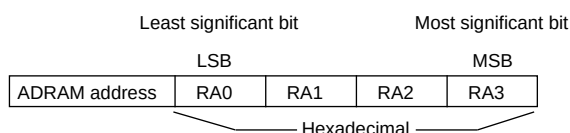
Display digit	1	2	3	4	5	6	7	8	9	10	11	12
ADRAM address (hexadecimal)	1	2	3	4	5	6	7	8	9	A	B	0

(Left shift)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12
ADRAM address (hexadecimal)	B	0	1	2	3	4	5	6	7	8	9	A

(Right shift)

Note: *4. The ADRAM addresses are expressed in hexadecimal.



Example: When the ADRAM address is A_H

RA0	RA1	RA2	RA3
0	1	0	1

Note: *5. 5×7 dots ... 12-digit display 5 dots
 5×8 dots ... 12-digit display 4 dots
 5×9 dots ... 12-digit display 3 dots

- CGROM (Character generator ROM)

CGROM is ROM used to generate the 240 kinds of 5×7 , 5×8 , or 5×9 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240×45 bits. When a character code is written to DCRAM, the character pattern stored in CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.

- CGRAM (Character generator RAM)

CGRAM is RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5×7 , 5×8 , or 5×9 dot matrix character patterns can be stored. CGRAM has a capacity of 16×45 bits.

Reset Function

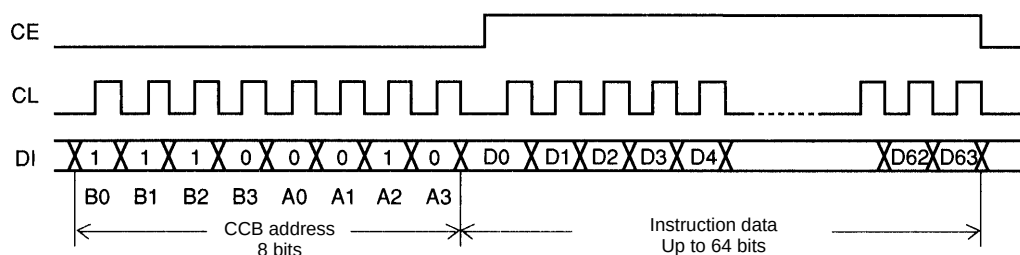
The LC75811E and LC75811W are reset when a low level is applied to the $\overline{\text{RES}}$ pin at power on and, in normal mode. On a reset the LC75811E and LC75811W create a display with all LCD panels turned off. However, after a reset applications must set the contents of DCRAM, ADRAM, and CGRAM before turning on display with a “display on/off control” instruction since the contents of these memories are undefined. That is, applications must execute the following instructions.

- Set display technique
- DCRAM data write
- ADRAM data write (If ADRAM is used.)
- CGRAM data write (If CGRAM is used.)
- Set AC address

After executing the above instructions, applications must turn on the display with a “display on/off control” instruction. Note that when applications turn off in the normal mode, applications must turn off the display with a “display on/off control” instruction. (See the detailed instruction descriptions.)

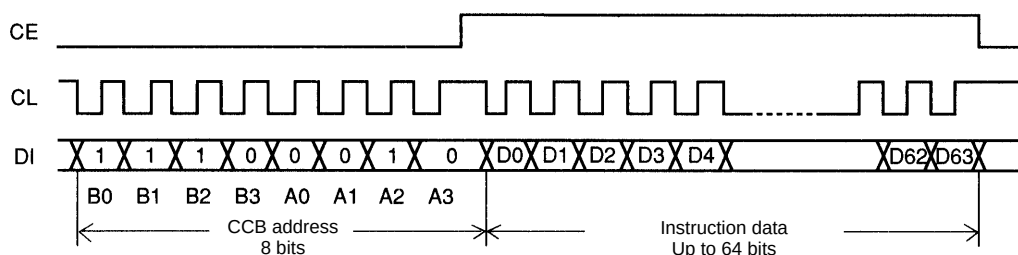
Serial Data Transfer Format

- When CL is stopped at the low level



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- When CL is stopped at the high level



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- CCB address: 47H
- D0 to D63: Instruction data

The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

Instruction	D0 D1...D39	D40 D41 D42 D43 D44 D45 D46 D47	D48 D49 D50 D51 D52 D53 D54 D55	D56 D57 D58 D59	D60 D61 D62 D63	Execution time *8
Set display technique				DT1 DT2 X X	0 0 0 1	0 µs
Display on/off control		DG1 DG2 DG3 DG4 DG5 DG6 DG7 DG8	DG9 DG10DG11DG12 X X X X	M A SC BU	0 0 1 0	0 µs/27 µs *9
Display shift				M A R/L X	0 0 1 1	27 µs
Set AC address			DA0 DA1 DA2 DA3 DA4 DA5 X X	RA0 RA1 RA2 RA3	0 1 0 0	27 µs
DCRAM data write *6		AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7	DA0 DA1 DA2 DA3 DA4 DA5 X X	IM X X X	0 1 0 1	27 µs
ADRAM data write *7		AD1 AD2 AD3 AD4 AD5 X X X	RA0 RA1 RA2 RA3 X X X X	IM X X X	0 1 1 0	27 µs
CGRAM data write	CD1 CD2...CD40	CD41 CD42 CD43 CD44 CD45 X X X	CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7	X X X X	0 1 1 1	27 µs

X: don't care

Notes: *6. The data format differs when the "DCRAM data write" instruction is executed in the increment mode (IM = 1).

(See detailed instruction descriptions.)

*7. The data format differs when the "ADRAM data write" instruction is executed in the increment mode (IM = 1).

(See detailed instruction descriptions.)

*8. The execution times listed here apply when fosc = 300 kHz. The execution times differ when the oscillator frequency fosc differs.

Example: When fosc = 210 kHz

$$27 \mu s \times \frac{300}{210} = 39 \mu s$$

*9. When the power saving mode (BU = 1) is set, the execution time is 27 µs (when fosc = 300 kHz).

Detailed Instruction Descriptions

- Set display technique ... <Sets the display technique>

Code						
D56	D57	D58	D59	D60	D61	D62 D63
DT1	DT2	X	X	0	0	0 1

X: don't care

DT1, DT2: Setting the display technique

DT1	DT2	Display technique	Output pins	
			S60/COM9	S59/COM10
0	0	1/8 duty, 1/4 bias drive	S60	S59
1	0	1/9 duty, 1/4 bias drive	COM9	S59
0	1	1/10 duty, 1/4 bias drive	COM9	COM10

Note: *10. Sn (n = 59, 60): Segment outputs
COMn (n = 9, 10): Common outputs

- Display on/off control ... <Turns the display on or off>

Code																						
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62 D63
DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	X	X	X	X	M	A	SC	BU	0	0	1 0

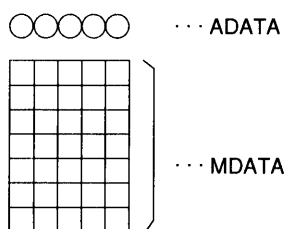
X: don't care

M, A: Specifies the data to be turned on or off.

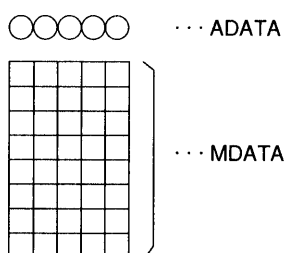
M	A	Display operating state
0	0	Both MDATA and ADATA are turned off (The display is forcibly turned off regardless of the DG1 to DG12 data.)
0	1	Only ADATA is turned on (The ADATA of display digits specified by the DG1 to DG12 data are turned on.)
1	0	Only MDATA is turned on (The MDATA of display digits specified by the DG1 to DG12 data are turned on.)
1	1	Both MDATA and ADATA are turned on (The MDATA and ADATA of display digits specified by the DG1 to DG12 data are turned on.)

Note: *11. MDATA, ADATA

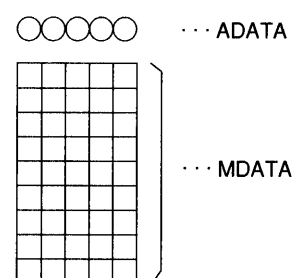
5 × 7 dot matrix display



5 × 8 dot matrix display



5 × 9 dot matrix display



A10719

DG1 to DG12: Specifies the display digit

Display digit	1	2	3	4	5	6	7	8	9	10	11	12
Display digit data	DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12

For example, if DG1 to DG6 are 1, and DG7 to DG12 are 0, then display digits 1 to 6 will be turned on, and display digits 7 to 12 will be turned off (blanked).

SC: Controls the common and segment output pins.

SC	Common and segment output pin states
0	Output of LCD drive waveforms
1	Fixed at the V _{SS} level (all segments off)

Note: *12. When SC is 1, the S1 to S60 and COM1 to COM10 output pins are set to the V_{SS} level, regardless of the M, A, and DG1 to DG12 data.

BU: Controls the normal mode and power saving mode.

BU	Mode
0	Normal mode
1	Power saving mode (In this mode, the OSCI and OSCO pins oscillator is stopped, and the common and segment pins are set to the V _{SS} level. In this mode, instructions other than the "display on/off control" instruction cannot be executed. Thus applications must set the LSI to normal mode before executing any of the other instructions.)

• Display shift ... <Shifts the display>

Code							
D56	D57	D58	D59	D60	D61	D62	D63
M	A	R/L	X	0	0	1	1

X: don't care

M, A: Specifies the data to be shifted

M	A	Shift operating state
0	0	Neither MDATA nor ADATA is shifted
0	1	Only ADATA is shifted
1	0	Only MDATA is shifted
1	1	Both MDATA and ADATA are shifted

R/L: Shift direction specification

R/L	Shift direction
0	Left shift
1	Right shift

• Set AC address... <Specifies the DCRAM and ADRAM address for AC>

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
DA0	DA1	DA2	DA3	DA4	DA5	X	X	RA0	RA1	RA2	RA3	0	1	0	0

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5
LSB					MSB
Least significant bit			Most significant bit		

RA0 to RA3: ADRAM address

RA0	RA1	RA2	RA3
LSB			MSB
Least significant bit		Most significant bit	

This instruction loads the 6-bit DCRAM address DA0 to DA5 and the 4-bit ADRAM address RA0 to RA3 into the AC.

- DCRAM data write ... <Specifies the DCRAM address and stores data at that address>

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM	X	X	X	0	1	0	1

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5
LSB			MSB		
Least significant bit			Most significant bit		

AC0 to AC7: DCRAM data (character code)

AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7
LSB				MSB			
Least significant bit				Most significant bit			

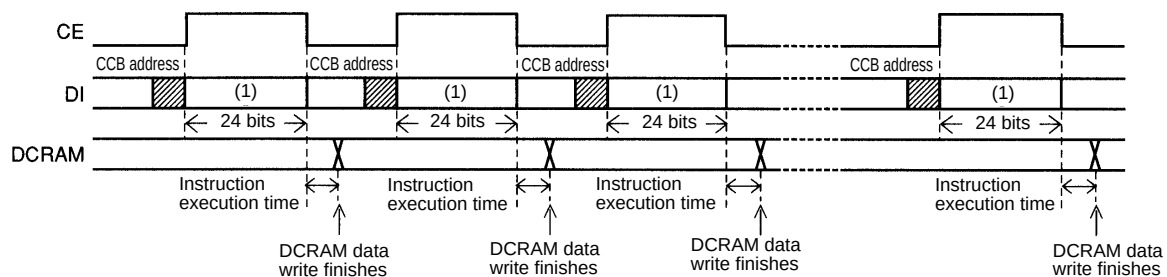
This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5×7 , 5×8 , or 5×9 dot matrix display data using CGROM or CGRAM.

IM: Setting the method of writing data to DCRAM

IM	DCRAM data write method
0	Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)
1	Increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.)

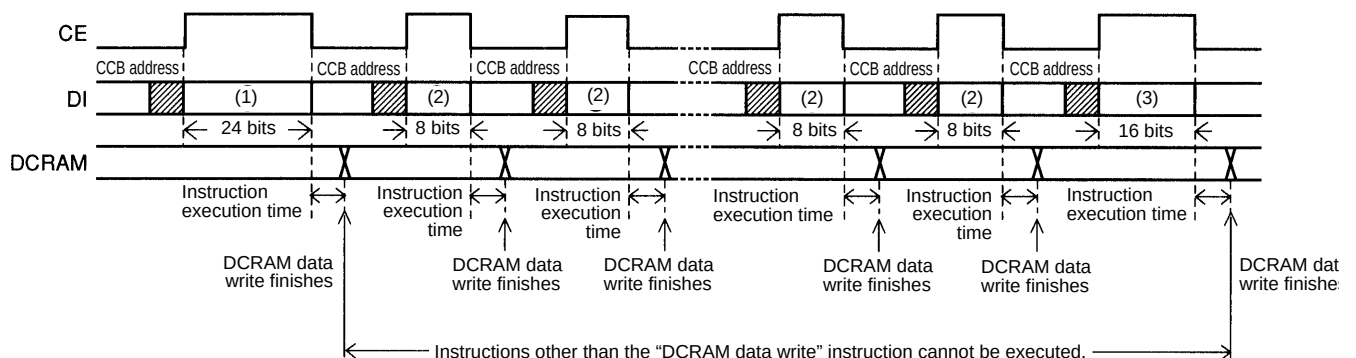
Notes: *13.

- DCRAM data write method when IM = 0



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- DCRAM data write method when IM = 1 (Instructions other than the "DCRAM data write" instruction cannot be executed.)



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Data format at (1) (24 bits)

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM	X	X	X	0	1	0	1

X: don't care

Data format at (2) (8 bits)

Code							
D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

Data format at (3) (16 bits)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	0	X	X	X	0	1	0	1

X: don't care

- ADAM data write ... <Specifies the ADAM address and stores data at that address>

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM	X	X	X	0	1	1	0

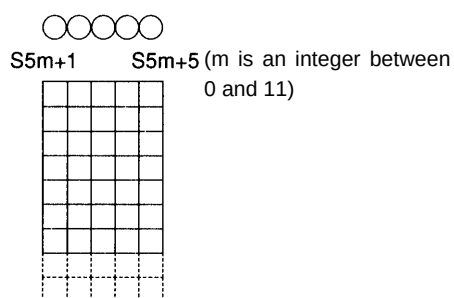
X: don't care

RA0 to RA3: ADAM address

RA0	RA1	RA2	RA3
LSB			MSB
Least significant bit			Most significant bit

AD1 to AD5: ADATA display data

In addition to the 5×7 , 5×8 , or 5×9 dot matrix display data (MDATA), this LSI supports direct display of the five accessory display segments provided in each digit as ADATA. This display function does not use CGROM or CGRAM. The figure below shows the correspondence between the data and the display. When $AD_n = 1$ (where n is an integer between 1 and 5) the segment corresponding to that data will be turned on.



ADATA	Corresponding output pin
AD1	S5m + 1 (m is an integer between 0 and 11)
AD2	S5m + 2
AD3	S5m + 3
AD4	S5m + 4
AD5	S5m + 5

LC75811E, 75811W

- CGRAM data write ... <Specifies the CGRAM address and stores data at that address>

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
CD1	CD2	CD3	CD4	CD5	CD6	CD7	CD8	CD9	CD10	CD11	CD12	CD13	CD14	CD15	CD16

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
CD17	CD18	CD19	CD20	CD21	CD22	CD23	CD24	CD25	CD26	CD27	CD28	CD29	CD30	CD31	CD32

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
CD33	CD34	CD35	CD36	CD37	CD38	CD39	CD40	CD41	CD42	CD43	CD44	CD45	X	X	X

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	X	X	X	X	0	1	1	1

X: don't care

CA0 to CA7: CGRAM address

CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
LSB				MSB			
Least significant bit				Most significant bit			

CD1 to CD45: CGRAM data (5×7 , 5×8 , or 5×9 dot matrix display data)

The bit CD_n (where n is an integer between 1 and 45) corresponds to the 5×7 , 5×8 , or 5×9 dot matrix display data. The figure below shows that correspondence. The dots for which the corresponding data CD_n is 1 will be turned on.

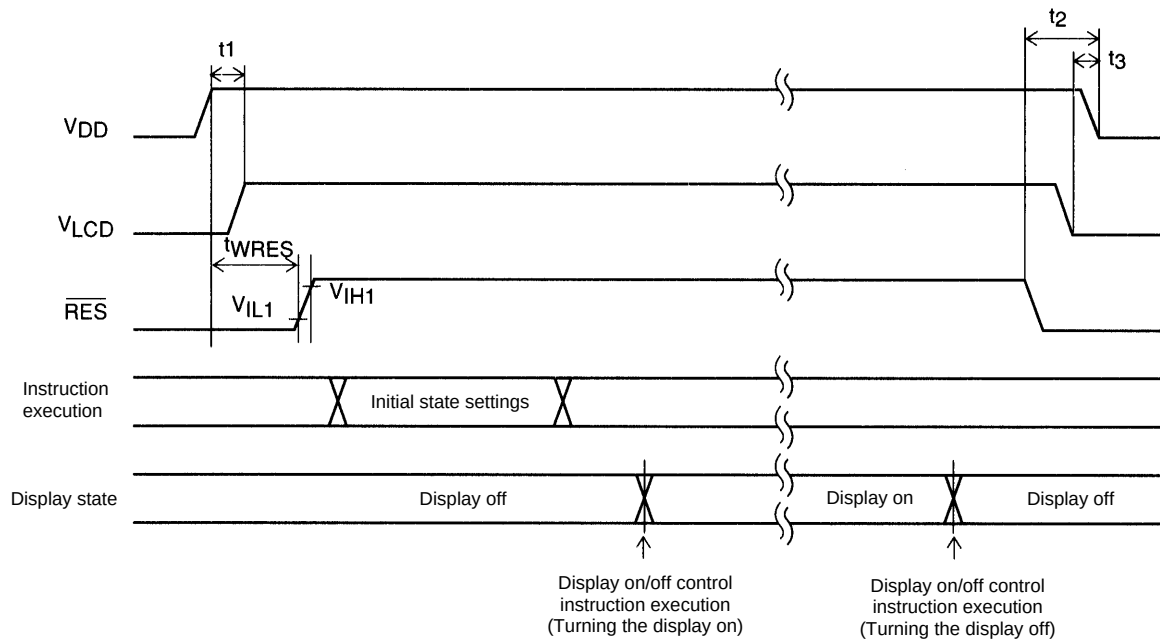
CD1	CD2	CD3	CD4	CD5
CD6	CD7	CD8	CD9	CD10
CD11	CD12	CD13	CD14	CD15
CD16	CD17	CD18	CD19	CD20
CD21	CD22	CD23	CD24	CD25
CD26	CD27	CD28	CD29	CD30
CD31	CD32	CD33	CD34	CD35
CD36	CD37	CD38	CD39	CD40
CD41	CD42	CD43	CD44	CD45

Note:*15. CD1 to CD35: 5×7 dot matrix display data
 CD1 to CD40: 5×8 dot matrix display data
 CD1 to CD45: 5×9 dot matrix display data

Notes on the Power On and Power Off Sequences

- At power on: Logic block power supply (V_{DD}) on $\rightarrow$ LCD driver block power supply (V_{LCD}) on
- At power off: LCD driver block power supply (V_{LCD}) off $\rightarrow$ Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.



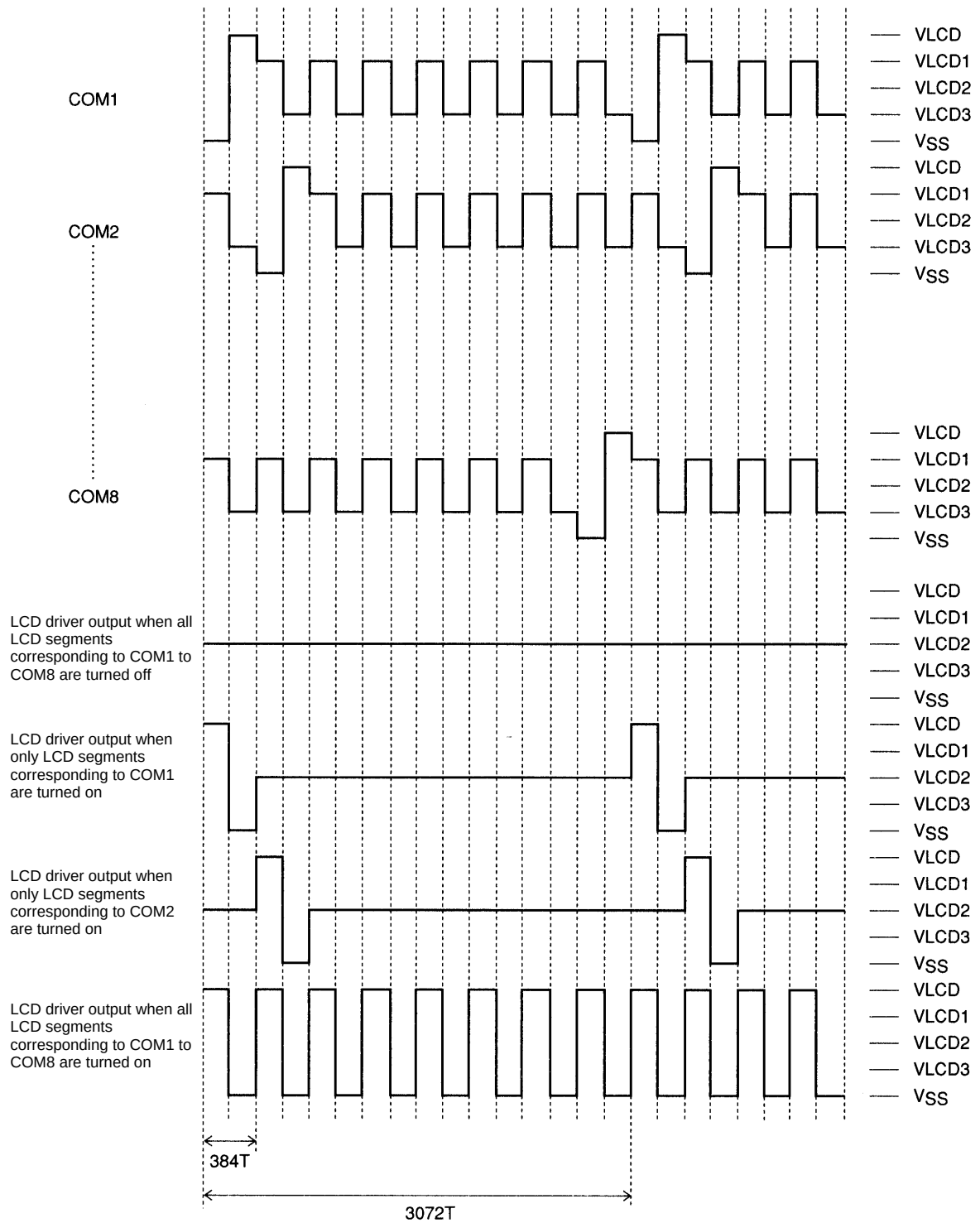
A10725

Initial state settings

- $t_1 \geq 0$
 - $t_2 > 0$
 - $t_3 \geq 0$ ($t_2 > t_3$)
 - $t_{WRES} \dots 1 \mu s \text{ min}$
- Set display technique
 - DGRAM data write
 - ADRAM data write (If ADRAM is used.)
 - CGRAM data write (If CGRAM is used.)
 - Set AC address

Figure 3

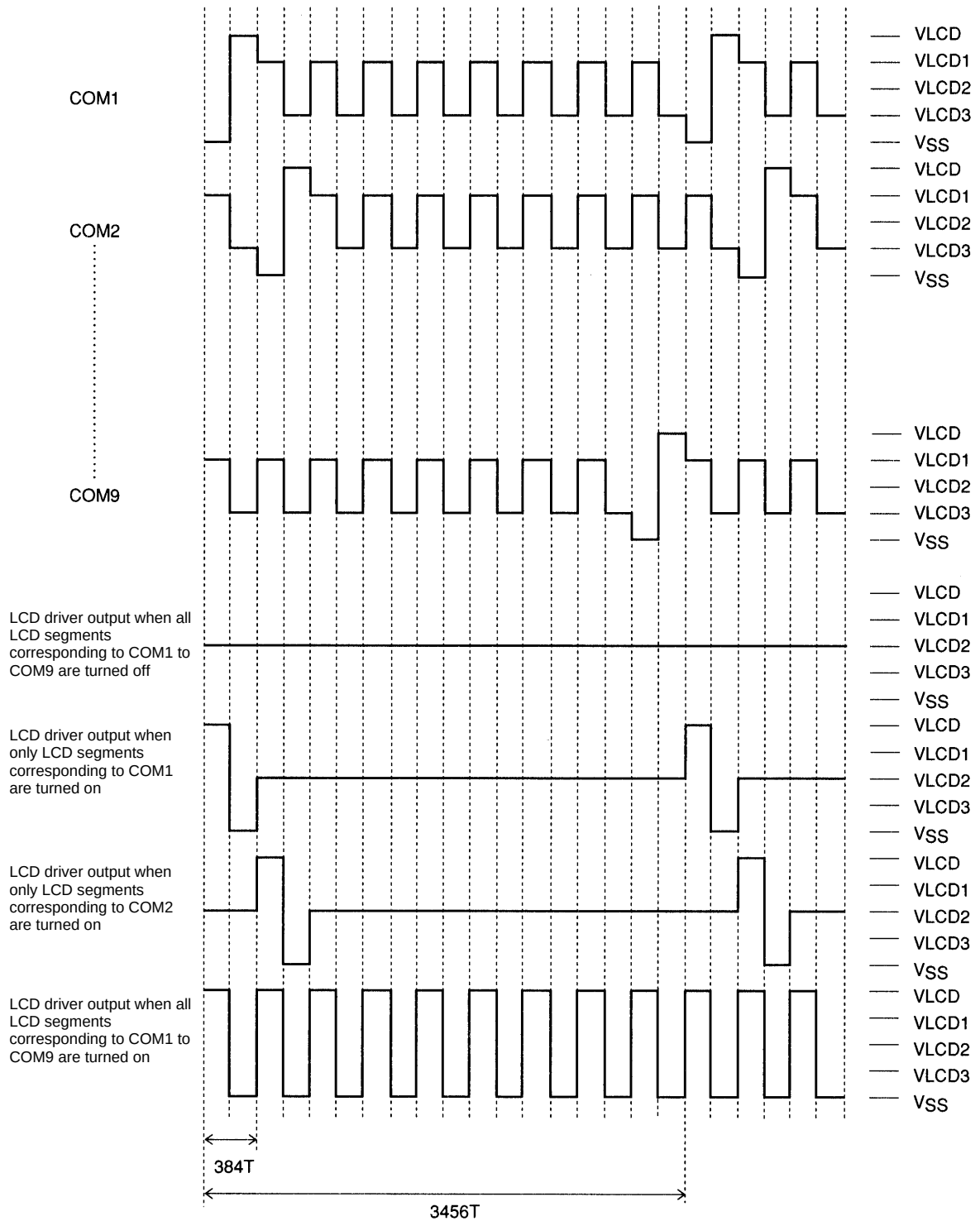
1/8 Duty, 1/4 Bias Drive Technique



A10726

$$T = \frac{1}{f_{osc}}$$

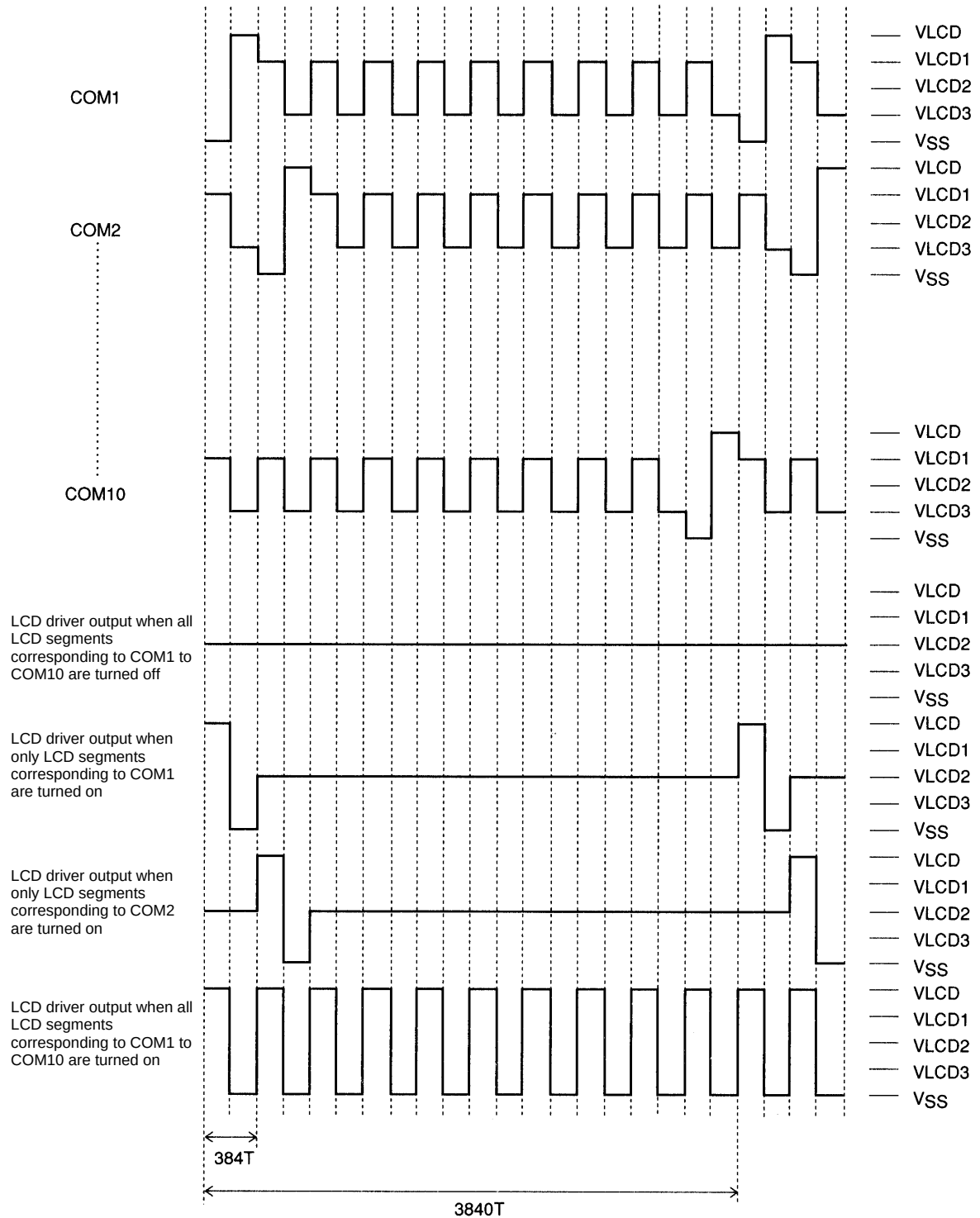
1/9 Duty, 1/4 Bias Drive Technique



A10727

$$T = \frac{1}{f_{osc}}$$

1/10 Duty, 1/4 Bias Drive Technique

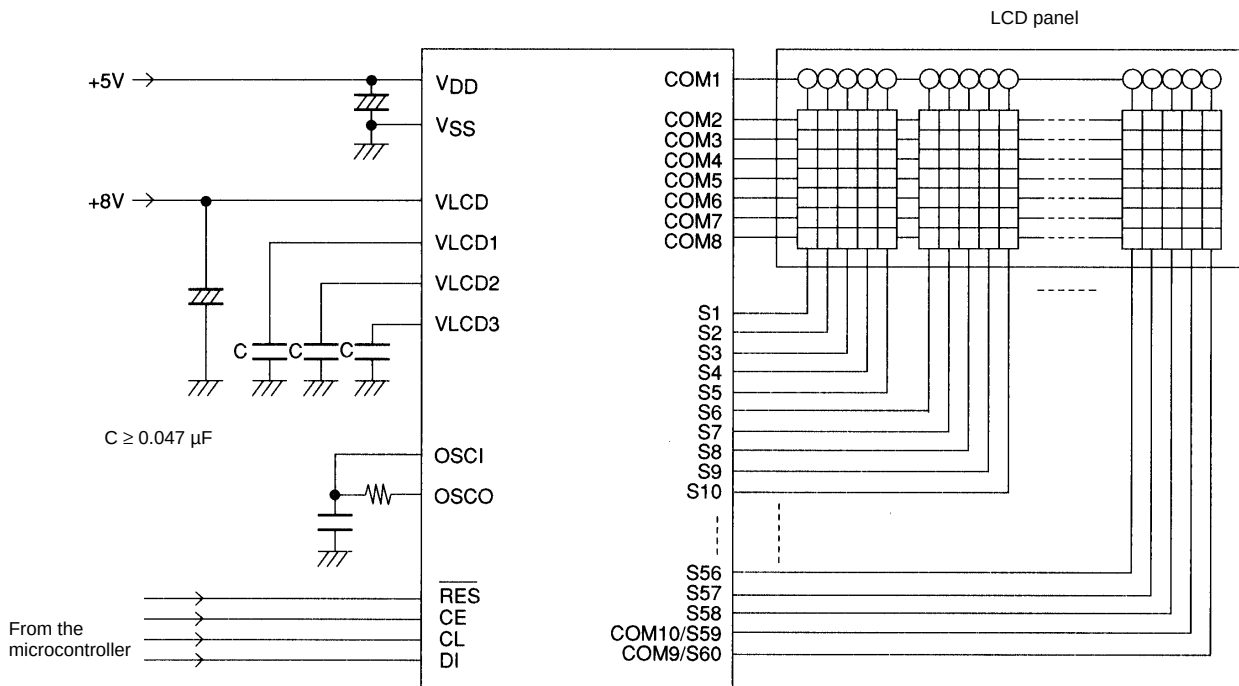


A10728

$$T = \frac{1}{f_{osc}}$$

Sample Application Circuit 1

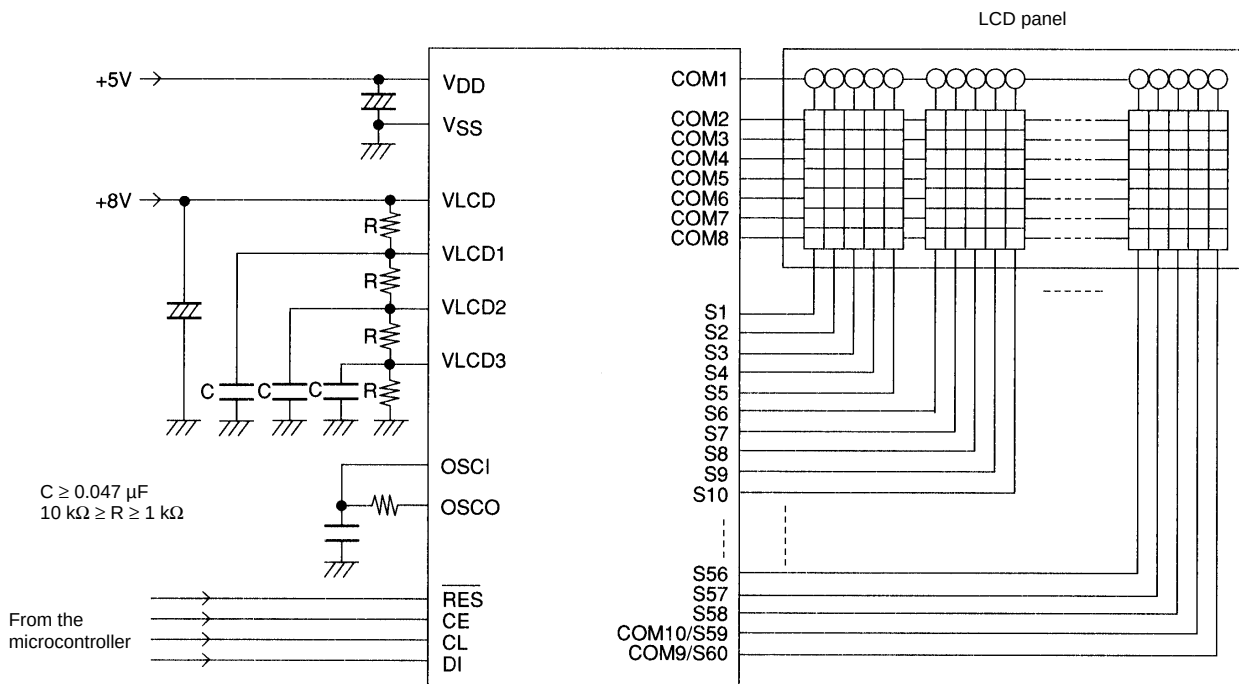
1/8 Duty, 1/4 Bias Drive (For use with normal panels)



A10729

Sample Application Circuit 2

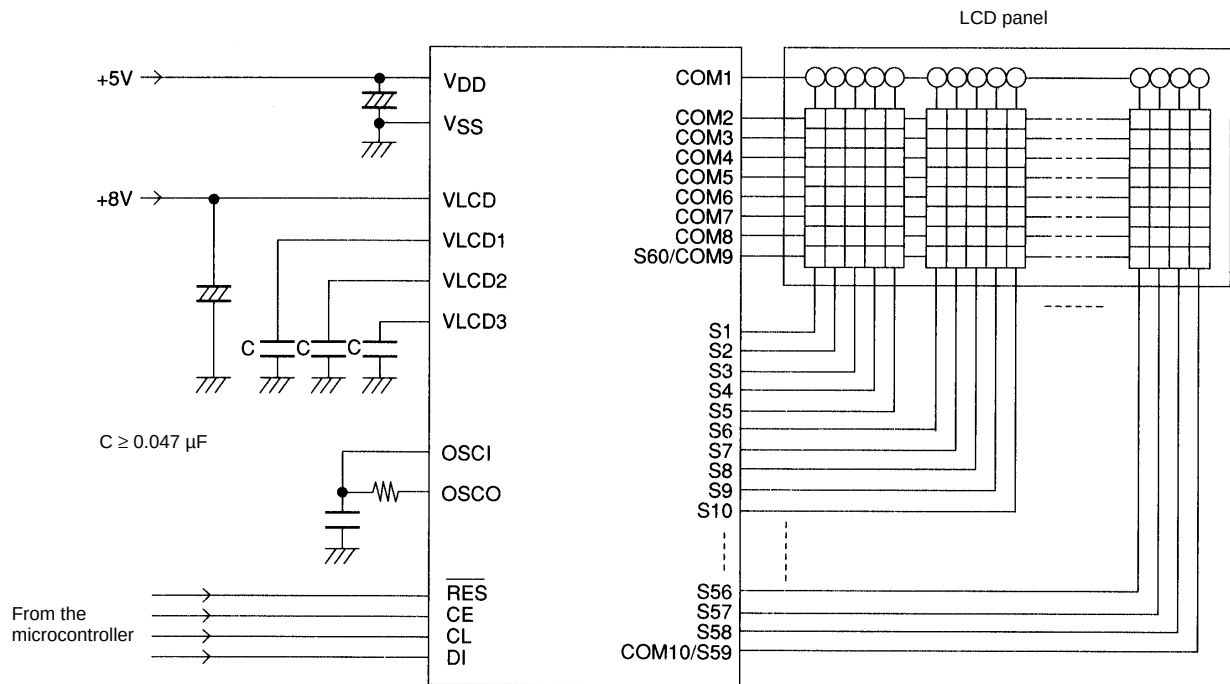
1/8 Duty, 1/4 Bias Drive (For use with large panels)



A10730

Sample Application Circuit 3

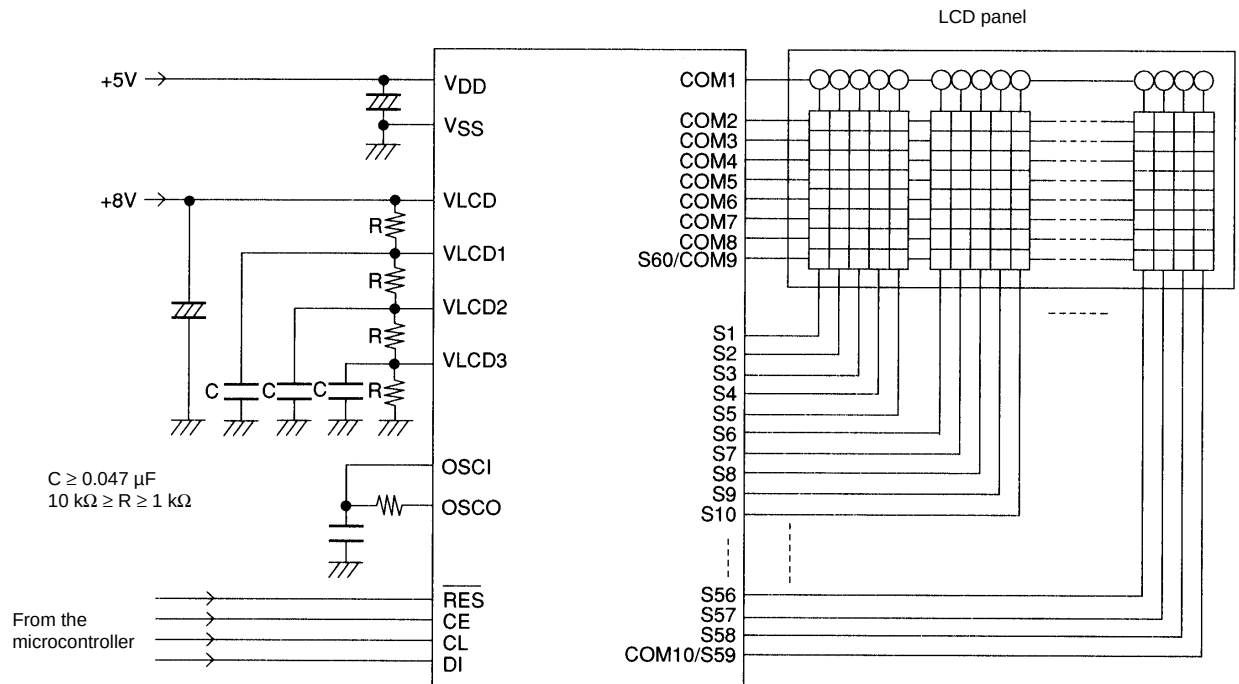
1/9 Duty, 1/4 Bias Drive (For use with normal panels)



A10731

Sample Application Circuit 4

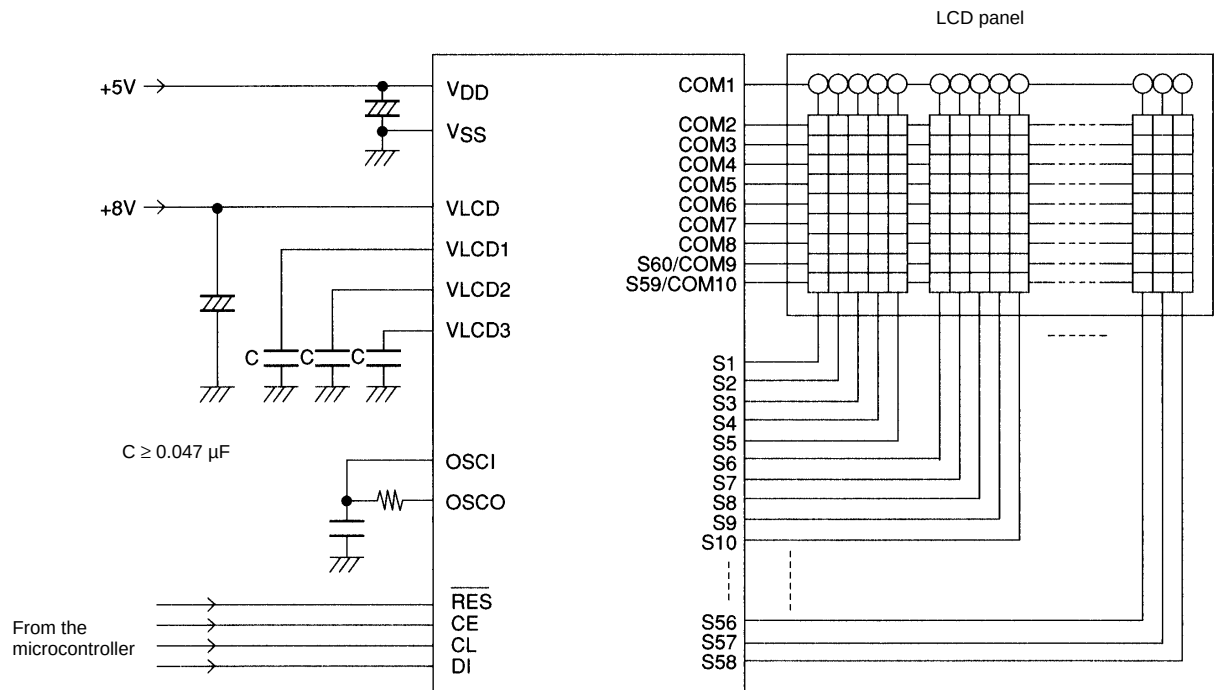
1/9 Duty, 1/4 Bias Drive (For use with large panels)



A10732

Sample Application Circuit 5

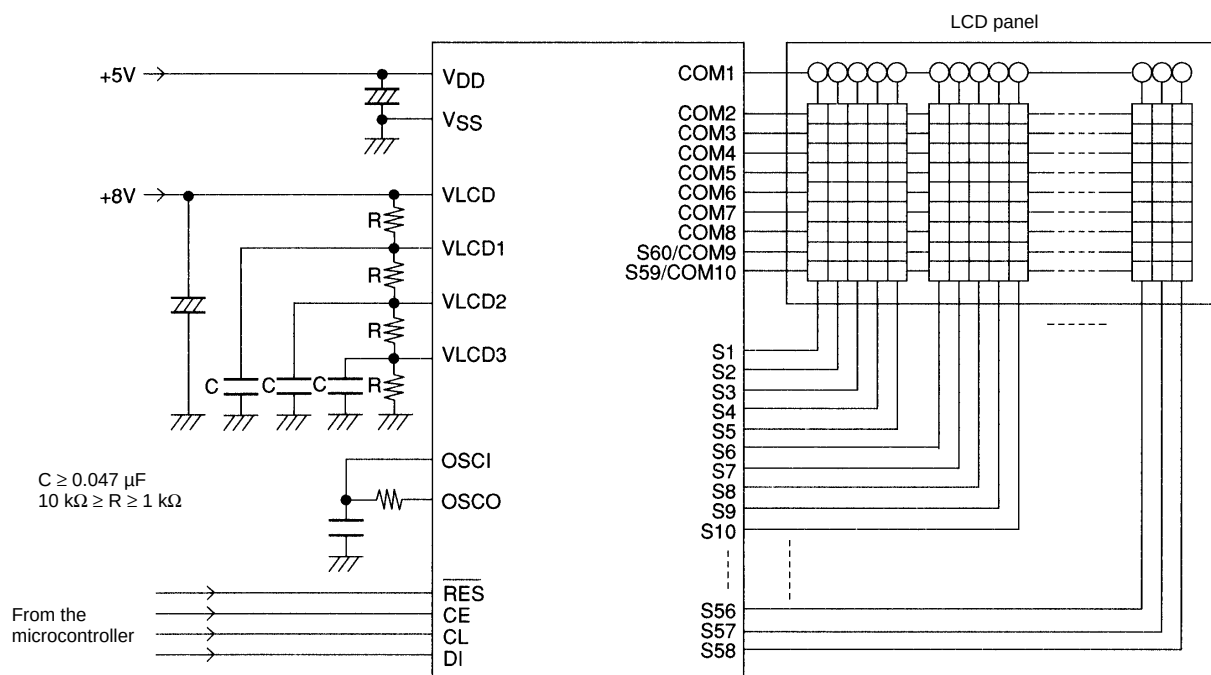
1/10 Duty, 1/4 Bias Drive (For use with normal panels)



A10733

Sample Application Circuit 6

1/10 Duty, 1/4 Bias Drive (For use with large panels)



A10734

Sample Correspondence between Instructions and the Display (When the LC75811-8715 is used)

No.	Instruction (hexadecimal)						Display	Operation
	LSB D40 to D43	D44 to D47	D48 to D51	D52 to D55	D56 to D59	MSB D60 to D63		
1	Power application (Initialization with the RES pin.)							Initializes the IC. The display is in the off state.
2	Set display technique							Sets to 1/8 duty 1/4 bias display drive technique
3	DCRAM data write (increment mode)							Writes the display data " " to DCRAM address 00H
	0	2	0	0	1	A		
4	DCRAM data write (increment mode)							Writes the display data "S" to DCRAM address 01H
					3	5		
5	DCRAM data write (increment mode)							Writes the display data "A" to DCRAM address 02H
					1	4		
6	DCRAM data write (increment mode)							Writes the display data "N" to DCRAM address 03H
					E	4		
7	DCRAM data write (increment mode)							Writes the display data "Y" to DCRAM address 04H
					9	5		
8	DCRAM data write (increment mode)							Writes the display data "O" to DCRAM address 05H
					F	4		
9	DCRAM data write (increment mode)							Writes the display data " " to DCRAM address 06H
					0	2		
10	DCRAM data write (increment mode)							Writes the display data "L" to DCRAM address 07H
					C	4		
11	DCRAM data write (increment mode)							Writes the display data "S" to DCRAM address 08H
					3	5		
12	DCRAM data write (increment mode)							Writes the display data "I" to DCRAM address 09H
					9	4		
13	DCRAM data write (increment mode)							Writes the display data " " to DCRAM address 0AH
					0	2		
14	DCRAM data write (increment mode)							Writes the display data " " to DCRAM address 0BH
					0	2		
15	DCRAM data write (increment mode)							Writes the display data "L" to DCRAM address 0CH
					C	4		
16	DCRAM data write (increment mode)							Writes the display data "C" to DCRAM address 0DH
					3	4		
17	DCRAM data write (increment mode)							Writes the display data "7" to DCRAM address 0EH
					7	3		
18	DCRAM data write (increment mode)							Writes the display data "5" to DCRAM address 0FH
					5	3		
19	DCRAM data write (increment mode)							Writes the display data "8" to DCRAM address 10H
					8	3		
20	DCRAM data write (increment mode)							Writes the display data "1" to DCRAM address 11H
					1	3		
21	DCRAM data write (increment mode)							Writes the display data "1" to DCRAM address 12H
		1	3	0		A		

Continued on next page.

LC75811E, 75811W

Continued from preceding page.

No.	Instruction (hexadecimal)						Display	Operation
	LSB D40 to D43	D44 to D47	D48 to D51	D52 to D55	D56 to D59	MSB D60 to D63		
22	Set AC address							Loads the DGRAM address 00H and the ADRAM address 0H into AC
		0	0	0	0	2		
23	Display on/off control						S A N Y O L S I	Turns on the LCD for all digits (12 digits) in MDATA
	F	F	F	X	1	4		
24	Display shift						S A N Y O L S I L	Shifts the display (MDATA only) to the left
					1	C		
25	Display shift						A N Y O L S I L C	Shifts the display (MDATA only) to the left
					1	C		
26	Display shift						N Y O L S I L C 7	Shifts the display (MDATA only) to the left
					1	C		
27	Display shift						Y O L S I L C 7 5	Shifts the display (MDATA only) to the left
					1	C		
28	Display shift						O L S I L C 7 5 8	Shifts the display (MDATA only) to the left
					1	C		
29	Display shift						L S I L C 7 5 8 1	Shifts the display (MDATA only) to the left
					1	C		
30	Display shift						L S I L C 7 5 8 1 1	Shifts the display (MDATA only) to the left
					1	C		
31	Display on/off control							Set to power saving mode, turns off the LCD for all digits
	0	0	0	X	8	4		
32	Display on/off control						L S I L C 7 5 8 1 1	Turns on the LCD for all digits (12 digits) in MDATA
	F	F	F	X	1	4		
33	Set AC address						S A N Y O L S I	Loads the DGRAM address 00H and the ADRAM address 0H into AC
		0	0	0	0	2		

Note: *16. This example above assumes the use of 12 digits 5 × 7 dot matrix LCD. CGRAM and ADRAM are not used.

X: don't care

LC75811-8715 Character Font (Standard)

Upper 4bits Lower 4bits	MSB 0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000 LSB	CG RAM(1)	α		0	@	P	^	p	á	ë	/	!	タ	≡	À	Ä
0001	β		!	1	A	Q	a	q	â	ä	。	ア	チ	厶	À	Ä
0010	±		"	2	B	R	b	r	é	ê	「	イ	ッ	メ	É	Ê
0011	÷		#	3	C	S	c	s	è	é	」	ウ	テ	モ	È	É
0100	π		\$	4	D	T	d	t	í	ï	,	エ	ト	ヤ	Í	Ï
0101	¿		%	5	E	U	e	u	ì	î	.	オ	ナ	ユ	Ì	Î
0110	ø		&	6	F	V	f	v	ó	ô	ヲ	カ	ニ	ヨ	Ó	Ô
0111	ø		'	7	G	W	g	w	ò	ö	ア	キ	ヌ	ヲ	Ò	Ö
1000	æ		(	8	H	X	h	x	ú	û	イ	ク	リ		Ú	Û
1001	æ		)	9	I	Y	i	y	ù	ü	ウ	ケ	ル		Ü	
1010	œ		*	:	J	Z	j	z	ñ	ñ	エ	コ	ハ		Ã	ä
1011	œ		+	:	K	[	k	{	ñ	ñ	オ	サ	ヒ		Ö	ö
1100	→		.	<	L	¥	l		\$	\$	ヤ	シ	フ		À	á
1101	←		-	=	M	]	m	}	ç	ç	エ	ズ	ヘ		é	í
1110	↑		.	>	N	^	n	~	í	í	エ	セ	ホ		ñ	ñ
1111	↓		/	?	O	—	o	■	Ij	Ij	ッ	ソ	マ		é	é

A10735

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- Техническая поддержка проекта;
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