



Features

- Processed with BCDMOS on SOI (Silicon On Insulator)
- Flexible High Voltage Supplies up to $V_{PP}-V_{NN}=200V$
- DC to 10MHz Analog Signal Frequency
- 60dB Minimum Output-Off Isolation at 5MHz
- Low Quiescent Power Dissipation ($< 1\mu A$ typical)
- Low Output On-Resistance
- Adjustable High Voltage Supplies
- Surface Mount Package

Applications

- Ultrasound Imaging
- Printers
- Industrial Controls and Measurement
- Piezoelectric Transducer Drivers

Description

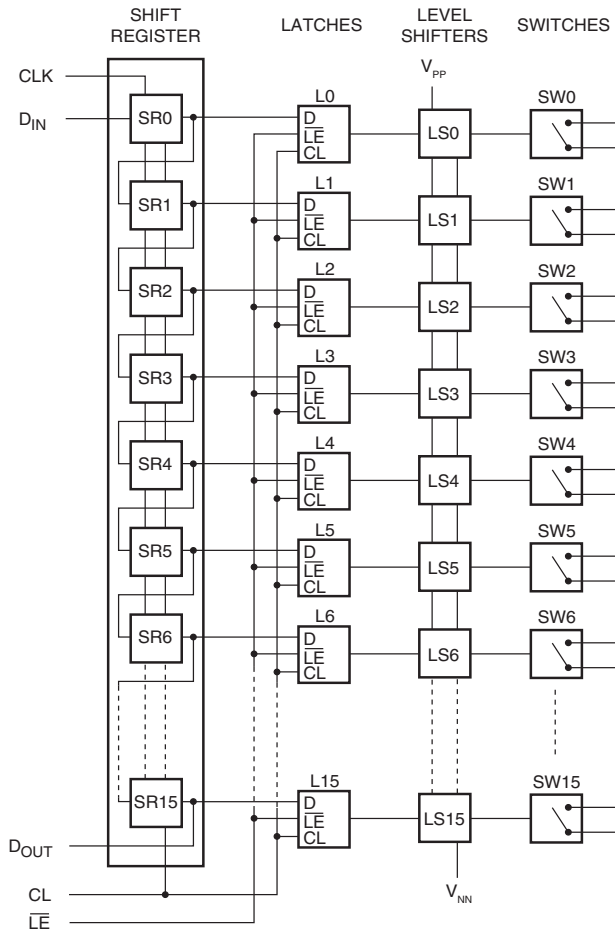
The CPC7601 is a low charge injection 16-channel high-voltage analog switch integrated circuit (IC) for use in applications requiring high voltage switching. Control of the high voltage switching is via low voltage CMOS logic level inputs for direct connectivity to the system controller.

Switch manipulation is managed by a 16-bit serial to parallel shift register whose outputs are buffered and stored by a 16-bit transparent latch. Level shifters buffer the latch outputs and operate the high voltage switches.

Because the CPC7601 is capable of switching high load voltages and has a flexible load voltage range, e.g. $V_{PP}/V_{NN} : +40V/-160V$ or $+100V/-100V$, it is well suited for many medical and industrial applications such as medical ultrasound imaging, printers, and industrial measurement equipment.

Construction of the high voltage switches using IXYS Integrated Circuits Division's reliable SOI BCDMOS process technology allows the switches to be organized as solid state switches with direct gate drive.

Figure 1. Block Diagram



Ordering Information

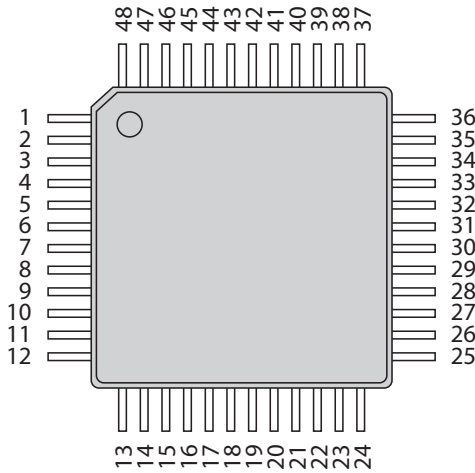
| Part Number | Description |
|-------------|-------------------------------------|
| CPC7601K | 48-Pin LQFP in Trays (250/Tray) |
| CPC7601KTR | 48-Pin LQFP Tape & Reel (2000/Reel) |



| | |
|--|-----------|
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1. Specifications

1.1 Package Pinout



1.2 Pin Description

| Pin | Name | Description |
|----------------------|------------------|--|
| 3 | SW4 | SW4 Output |
| 4 | SW4 | SW4 Output |
| 5 | SW3 | SW3 Output |
| 6 | SW3 | SW3 Output |
| 7 | SW2 | SW2 Output |
| 8 | SW2 | SW2 Output |
| 9 | SW1 | SW1 Output |
| 10 | SW1 | SW1 Output |
| 11 | SW0 | SW0 Output |
| 12 | SW0 | SW0 Output |
| 13 | V _{NN} | Switch Negative High Voltage Supply |
| 15 | V _{PP} | Switch Positive High Voltage Supply |
| 17 | GND | Ground: All Voltages are Referenced to GND |
| 18 | V _{DD} | Logic Positive Supply Voltage |
| 19 | D _{IN} | Serial Data Input |
| 20 | CLK | Clock Input, Positive Edge Trigger |
| 21 | LE | Latch Enable, Active Low |
| 22 | CL | Latch Clear, Active High, Asynchronously Clears Latches and Opens Switches |
| 23 | D _{OUT} | Serial Data Output |
| 24 | N/C | Do not use: Internally Connected to GND |
| 25 | SW15 | SW15 Output |
| 26 | SW15 | SW15 Output |
| 27 | SW14 | SW14 Output |
| 28 | SW14 | SW14 Output |
| 29 | SW13 | SW13 Output |
| 30 | SW13 | SW13 Output |
| 31 | SW12 | SW12 Output |
| 32 | SW12 | SW12 Output |
| 33 | SW11 | SW11 Output |
| 34 | SW11 | SW11 Output |
| 37 | SW10 | SW10 Output |
| 38 | SW10 | SW10 Output |
| 39 | SW9 | SW9 Output |
| 40 | SW9 | SW9 Output |
| 41 | SW8 | SW8 Output |
| 42 | SW8 | SW8 Output |
| 43 | SW7 | SW7 Output |
| 44 | SW7 | SW7 Output |
| 45 | SW6 | SW6 Output |
| 46 | SW6 | SW6 Output |
| 47 | SW5 | SW5 Output |
| 48 | SW5 | SW5 Output |
| 1, 2, 14, 16, 35, 36 | N/C | No Connection |

1.3 Absolute Maximum Ratings

Electrical Absolute Maximum ratings are at 25°C.

All voltages are referenced from ground (GND).

| Parameter | Min | Max | Units |
|--|-----------------|----------------------|-------|
| V _{DD} Logic Power Supply Voltage | -0.5 | 7 | V |
| V _{PP} - V _{NN} Supply Voltage | - | 220 | V |
| V _{PP} Positive High Voltage Supply | -0.5 | V _{NN} +200 | V |
| V _{NN} Negative High Voltage Supply | +0.5 | V _{PP} -200 | V |
| Logic input voltages | -0.5 | V _{DD} +0.3 | V |
| Analog signal range | V _{NN} | V _{PP} | V |
| Peak analog signal current per channel | - | 1 | A |
| Power dissipation | - | 2.3 | W |
| Storage temperature | - 65 | +150 | °C |

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

| Parameter | Symbol | Value |
|--|------------------|--|
| Logic power supply voltage ¹ | V _{DD} | 3V to 5.5V |
| Positive high voltage supply ¹ | V _{PP} | 40V to V _{NN} + 200V |
| Negative high voltage supply ¹ | V _{NN} | -40V to -160V |
| Analog signal voltage, peak-to-peak ² | V _{SIG} | V _{NN} +10V to V _{PP} -10V |
| Operating temperature | T _A | 0°C to 70°C |

¹ Power up/down sequence is arbitrary except that GND must be powered-up first and powered-down last.

² V_{SIG} must be V_{NN} ≤ V_{SIG} ≤ V_{PP} or floating during power up/down transition.

1.5 Electrical Characteristics

1.5.1 Switch Characteristics
(Over recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Test Conditions | 0°C | | +25°C | | | +70°C | | Units | |
|---|----------------------|---|------------------------|-----|-------|-----|-----|-------|-----|-------|---|
| | | | min | max | min | typ | max | min | max | | |
| Switch On-Resistance, Small Signal | R _{ONS} | V _{PP} =40V, V _{NN} =-160V | I _{SW} =5mA | - | 30 | - | 27 | 35 | - | 48 | Ω |
| | | | I _{SW} =200mA | - | 26 | - | 22 | 29 | - | 40 | |
| | | V _{PP} =100V, V _{NN} =-100V | I _{SW} =5mA | - | 30 | - | 27 | 35 | - | 48 | |
| | | | I _{SW} =200mA | - | 26 | - | 22 | 29 | - | 40 | |
| | | V _{PP} =160V, V _{NN} =-40V | I _{SW} =5mA | - | 30 | - | 27 | 35 | - | 48 | |
| | | | I _{SW} =200mA | - | 26 | - | 22 | 29 | - | 40 | |
| Switch On-Resistance Matching, Small Signal | ΔR _{ONS} | V _{PP} =100V, V _{NN} =-100V, I _{SW} =5mA | - | 20 | - | 4 | 20 | - | 20 | % | |
| Switch On-resistance, Large Signal | R _{ONL} | V _{SIG} =V _{PP} -10V, I _{SIG} =1A | - | - | - | 15 | - | - | - | Ω | |
| Switch Off Leakage, Per Switch | I _{SOL} | V _{SIG} =V _{PP} -10V and V _{NN} +10V | - | 5 | - | 0.4 | 10 | - | 15 | μA | |
| DC Offset, Switch Off | V _{OS} | R _L =100kΩ | - | 300 | - | - | 300 | - | 300 | mV | |
| DC Offset, Switch On | V _{OS} | R _L =100kΩ | - | 500 | - | - | 500 | - | 500 | | |
| Switch Output Peak Current | - | V _{SIG} duty cycle < 0.1% | - | - | - | - | 1 | - | - | A | |
| Output Switch Frequency | f _{SW} | Duty cycle = 50% | - | - | - | - | 50 | - | - | kHz | |
| Maximum V _{SIG} Slew Rate | dV/dt | V _{PP} =160V, V _{NN} =-40V | - | 20 | - | - | 20 | - | 20 | V/ns | |
| | | V _{PP} =100V, V _{NN} =-100V | | | | | | | | | |
| | | V _{PP} =40V, V _{NN} =-160V | | | | | | | | | |
| Off Isolation | K _O | f=5MHz, Z _L =1kΩ 15pF load | 30 | - | 30 | - | - | 30 | - | dB | |
| | | f=5MHz, R _L =50Ω | 58 | - | 58 | - | - | 58 | - | | |
| Switch Crosstalk | K _{CR} | f=5MHz, R _L =50Ω | -60 | - | -60 | - | - | -60 | - | dB | |
| Output Switch Isolation Diode Current | I _{ID} | 300ns pulse width, 2.0% duty cycle | - | 300 | - | - | 300 | - | 300 | mA | |
| Off Capacitance, SW to GND | C _{SG(OFF)} | V _{SW} =0V, f=1MHz | 5 | 17 | 5 | - | 17 | 5 | 20 | pF | |
| On Capacitance, SW to GND | C _{SG(ON)} | V _{SW} =0V, f=1MHz | 25 | 40 | 20 | - | 50 | 25 | 50 | | |
| Output Voltage Spike | +V _{SPK} | V _{PP} =40V, V _{NN} =-160V | R _L =50Ω | - | - | - | 150 | - | - | mV | |
| | -V _{SPK} | | | | | | | | | | |
| | +V _{SPK} | V _{PP} =100V, V _{NN} =-100V | | | | | | | | | |
| | -V _{SPK} | | | | | | | | | | |
| | +V _{SPK} | V _{PP} =160V, V _{NN} =-40V | | | | | | | | | |
| | -V _{SPK} | | | | | | | | | | |
| Charge Injection | Q | V _{PP} =100V, V _{NN} =-100V, V _{SIG} =0V | - | - | - | 820 | - | - | - | pC | |

1.5.2 Logic Timing Characteristics
(Over recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Test Conditions | 0°C | | +25°C | | | 70°C | | Units |
|---|------------|--|-----|-----|-------|-----|-----|------|-----|---------|
| | | | min | max | min | typ | max | min | max | |
| Setup Time Before \overline{LE} Rises | t_{SD} | - | 25 | - | 25 | - | - | 25 | - | ns |
| Time Width of \overline{LE} | t_{WLE} | $V_{DD}=3V$ | 56 | - | 56 | - | - | 56 | - | |
| | | $V_{DD}=5V$ | 12 | - | 12 | - | - | 12 | - | |
| Clock Delay Time to Data Out | t_{DO} | $V_{DD}=3V$ | 10 | 100 | 10 | - | 100 | 10 | 100 | |
| | | $V_{DD}=5V$ | 5 | 45 | 5 | - | 45 | 5 | 45 | |
| Time Width of CL | t_{WCL} | - | 55 | - | 55 | - | - | 55 | - | |
| Setup Time, Data to Clock | t_{su} | $V_{DD}=3V$ | 21 | - | - | 21 | - | 21 | - | |
| | | $V_{DD}=5V$ | 7 | - | - | 7 | - | 7 | - | |
| Hold Time, Data from Clock | t_h | - | 2 | - | 2 | - | - | 2 | - | |
| Clock Frequency | f_{CLK} | 50% duty cycle, $f_{DATA} = \frac{1}{2} f_{CLK}$, $V_{DD}=3V$ | - | 8 | - | - | 8 | - | 8 | MHz |
| | | 50% duty cycle, $f_{DATA} = \frac{1}{2} f_{CLK}$, $V_{DD}=5V$ | - | 20 | - | - | 20 | - | 20 | |
| Clock Rise and Fall Times | t_r, t_f | - | - | 50 | - | - | 50 | - | 50 | ns |
| Turn-On Time | t_{on} | $V_{SIG}=V_{PP}-10V, R_L=10k\Omega$ | - | 5 | - | - | 5 | - | 5 | μs |
| Turn-Off Time | t_{off} | | - | 5 | - | - | 5 | - | 5 | |

1.5.3 Logic Timing Waveforms



1.5.4 Logic DC Characteristics
(Over recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Test Conditions | 0°C | | +25°C | | | +70°C | | Units |
|------------------------------------|-----------------|----------------------------|---------------------|---------------------|----------------------|----------------------|---------------------|---------------------|---------------------|-------|
| | | | min | max | min | typ | max | min | max | |
| D _{OUT} Source Capability | V _{OH} | I _{OUT} = - 400μA | - | - | V _{DD} -0.7 | V _{DD} -0.1 | - | - | - | V |
| D _{OUT} Sink Capability | V _{OL} | I _{OUT} = +400μA | - | - | - | 0.04 | 0.7 | - | - | V |
| Input (Logic) Capacitance | C _{IN} | - | - | 10 | - | - | 10 | - | 10 | pF |
| Input, Logic High | V _{IH} | - | 0.9 V _{DD} | - | 0.9 V _{DD} | - | - | 0.9 V _{DD} | - | V |
| Input, Logic Low | V _{IL} | - | - | 0.1 V _{DD} | - | - | 0.1 V _{DD} | - | 0.1 V _{DD} | V |

1.5.5 Supply DC Characteristics
(Over recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Test Conditions | 0°C | | +25°C | | | +70°C | | Units |
|--|------------------|--|-----|-----|-------|------|-----|-------|-----|-------|
| | | | min | max | min | typ | max | min | max | |
| V _{PP} Quiescent Supply Current | I _{PPQ} | All Switches OFF | - | - | - | 0.1 | 50 | - | - | μA |
| | | All Switches ON, I _{SW} =5mA | - | - | - | - | - | - | - | |
| V _{NN} Quiescent Supply Current | I _{NNQ} | All Switches OFF | - | - | - | -0.1 | -50 | - | - | μA |
| | | All Switches ON, I _{SW} =5mA | - | - | - | - | - | - | - | |
| V _{PP} Operating Supply Current | I _{PP} | V _{PP} =40V, V _{NN} =-160V | - | 6.5 | - | - | 7 | - | 8 | mA |
| | | V _{PP} =100V, V _{NN} =-100V | - | 4 | - | - | 5.5 | - | 5.5 | |
| | | V _{PP} =160V, V _{NN} =-40V | - | 4 | - | - | 5 | - | 5.5 | |
| V _{NN} Operating Supply Current | I _{NN} | V _{PP} =40V, V _{NN} =-160V | - | 6.5 | - | - | 7 | - | 8 | mA |
| | | V _{PP} =100V, V _{NN} =-100V | - | 4 | - | - | 5.5 | - | 5.5 | |
| | | V _{PP} =160V, V _{NN} =-40V | - | 4 | - | - | 5 | - | 5.5 | |
| V _{DD} Average Supply Current | I _{DD} | f _{CLK} =5MHz, V _{DD} =5V | - | 4 | - | - | 4 | - | 4 | mA |
| V _{DD} Quiescent Supply Current | I _{DDQ} | - | - | 10 | - | 0.03 | 10 | - | 10 | μA |

1.5.6 Thermal Characteristics

| Parameter | Conditions | Symbol | Minimum | Typical | Maximum | Units |
|--|------------|------------------|---------|---------|---------|-------|
| Thermal Resistance (Junction to Ambient) | Free Air | R _{θJA} | - | - | 53 | °C/W |

2. Functional Description

The CPC7601 takes a serial stream of input data along with a synchronous clock signal. As the clock transits from low to high, the data at the input of each shift register is shifted through from SR(n) to SR(n+1). A high data bit, a “1,” represents an ON switch; a low data bit, a “0,” represents an OFF switch. Data is input and shifted through the internal shift register until all sixteen shift register positions, SR0 through SR15, are in the desired state.

D_{IN}: The data-in line presents data bits to be shifted through the internal shift register. The last bit into the shift register is the SW0 control bit.

CLK: The clock signal's rising edge is associated only with shifting data into and through the shift register.

CL: The clear line overrides all other inputs. When CL is high, the shift register is asynchronously cleared to all “0”s and all latches are set low, which causes all output switches to be turned OFF immediately. When CL is low, all output switches remain in whatever state they are in, ON or OFF, in response to CLK, latch inputs, and the \overline{LE} signal.

\overline{LE} : latch enable controls the state of the latches and thus the state of the eight switches. If \overline{LE} is high, then the latches do not change states, but retain their most recent status: either ON or OFF. With \overline{LE} high, input data and CLK have no effect on the state of the output switches. If \overline{LE} is low, then all latch outputs and their switch states follow the inputs from the shift register. \overline{LE} is overridden by CL: regardless of \overline{LE} 's state, CL clears the latches. See “**Truth Table**” on page 9. Note that holding \overline{LE} active while clocking in new data will cause the outputs to toggle with the shifting data.

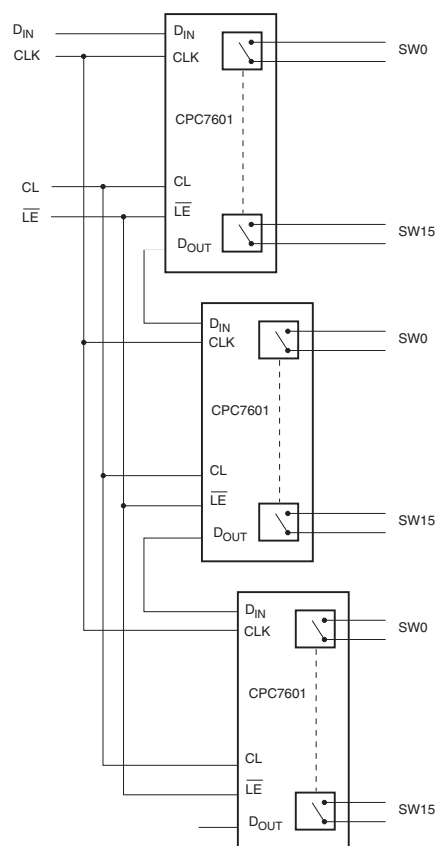
D_{OUT}: The data-out pin is the output of SR15. After sixteen clock pulses, the first bit of sixteen shifted input data bits is output at SR15, and appears on D_{OUT}.

SW0 - SW15: The CPC7601 provides sixteen high-voltage SPST output switches with a nominal small-signal on-resistance of 25Ω. The two connections of each switch are not polarity-sensitive.

V_{PP} and V_{NN}: Voltage inputs to the level shifters for each switch channel that translate the voltage level of the latch output signals to an appropriate level for the voltages being switched. The high-voltage output switches are turned on and off in response to data sent into the latches from the shift register: “0” turns a switch OFF, “1” turns a switch ON.

Two or more CPC7601 devices can be cascaded to form an n-switch arrangement. The D_{OUT} pin of the first is connected to the D_{IN} pin of the next in the series. All devices are connected to the same clock (CLK) signal. \overline{LE} of all devices would normally be connected, as would CL, but this is not necessary.

The first data bit applied to D_{IN} of the CPC7601, whether it's a single device or several cascaded devices, ripples through to the last switch output in line after the application of a full clocking sequence of sixteen clock pulses. Setting the serial I/O device to output the most significant bit (MSB) first, results in the MSB appearing on SW15 of the last device in line after a full clocking sequence.



3. Manufacturing Information

3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

| Device | Moisture Sensitivity Level (MSL) Rating |
|----------|---|
| CPC7601K | MSL 3 |

3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

| Device | Maximum Temperature x Time |
|----------|----------------------------|
| CPC7601K | 260°C for 30 seconds |

3.4 Board Wash

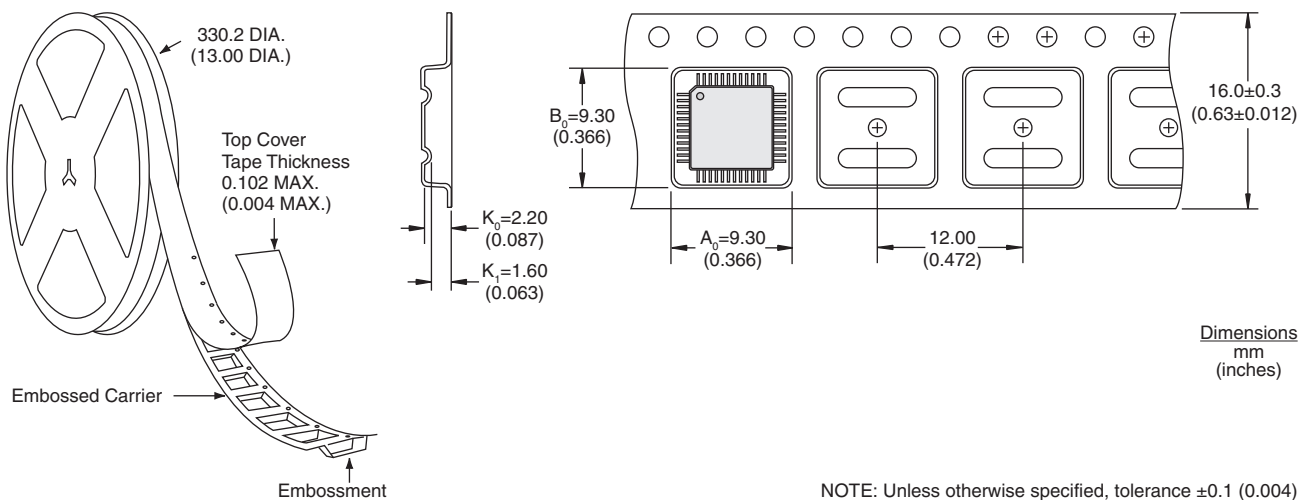
IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.



3.5 Mechanical Dimensions



3.6 Tape and Reel Specifications



For additional information please visit www.ixysic.com

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- Подбор аналогов;
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.