

# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## OptiMOS™

OptiMOS™5 Power-Transistor, 80 V  
BSC030N08NS5

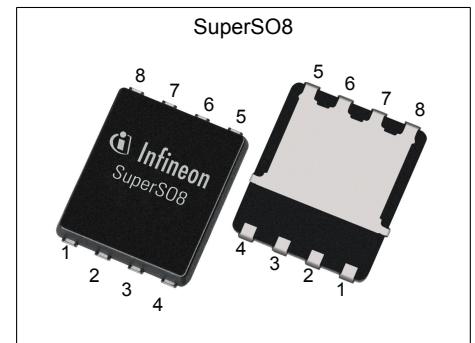
## Data Sheet

Rev. 2.2  
Final

## 1 Description

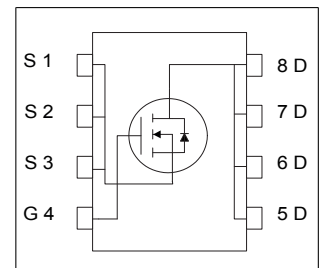
### Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	80	V
$R_{DS(on),max}$	3.0	mΩ
$I_D$	100	A
$Q_{oss}$	73	nC
$Q_G(0V..10V)$	61	nC



Type / Ordering Code	Package	Marking	Related Links
BSC030N08NS5	PG-TDSON-8	030N08NS	-

<sup>1)</sup> J-STD20 and JESD22

**Table of Contents**

Description .....	2
Maximum ratings .....	4
Thermal characteristics .....	4
Electrical characteristics .....	5
Electrical characteristics diagrams .....	7
Package Outlines .....	11
Revision History .....	12
Disclaimer .....	12

## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	100	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ , $R_{thJA}=50\text{K/W}^1)$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>3)</sup>	$E_{AS}$	-	-	250	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	139 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^1)$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	0.5	0.9	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>1)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>2)</sup> See figure 3 for more detailed information

<sup>3)</sup> See figure 13 for more detailed information

## 4 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3	3.8	V	$V_{DS}=V_{GS}$ , $I_D=95\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.6 3.4	3.0 4.5	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=25\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.6	2.4	$\Omega$	-
Transconductance	$g_{fs}$	55	110	-	S	$ V_{DS} >2 I_D /R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	4300	5600	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	700	910	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	32	56	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Rise time	$t_r$	-	12	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Fall time	$t_f$	-	13	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$

<sup>1)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	20	-	nC	$V_{DD}=40\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	12	-	nC	$V_{DD}=40\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>2)</sup>	$Q_{gd}$	-	13	19.5	nC	$V_{DD}=40\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	21	-	nC	$V_{DD}=40\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	$Q_g$	-	61	76	nC	$V_{DD}=40\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	$V_{DD}=40\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	52	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>2)</sup>	$Q_{oss}$	-	73	97.0	nC	$V_{DD}=40\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	100	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.9	1.1	V	$V_{GS}=0\text{ V}$ , $I_F=50\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery time <sup>2)</sup>	$t_{rr}$	-	54	108	ns	$V_R=40\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$	-	94	188	nC	$V_R=40\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> See "Gate charge waveforms" for parameter definition

<sup>2)</sup> Defined by design. Not subject to production test.

## 5 Electrical characteristics diagrams

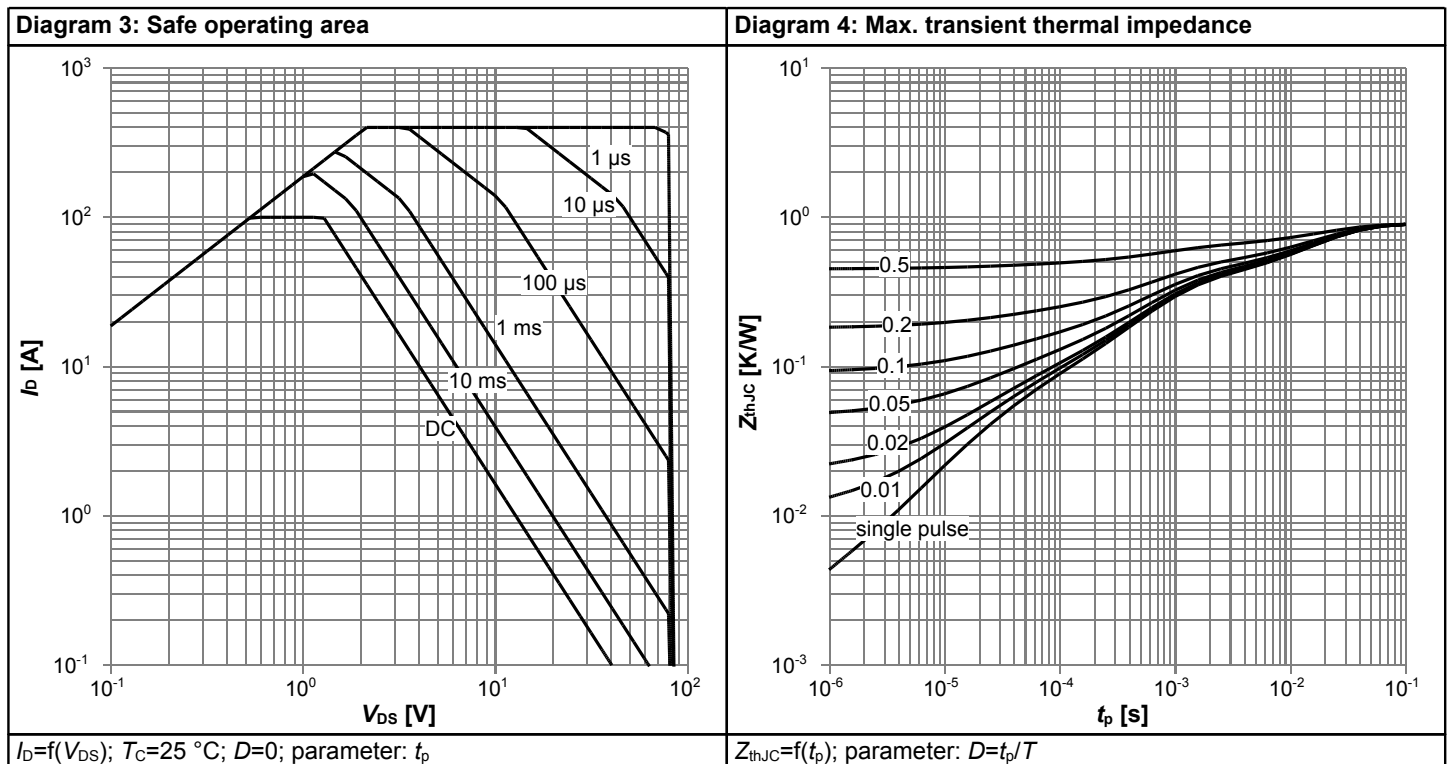
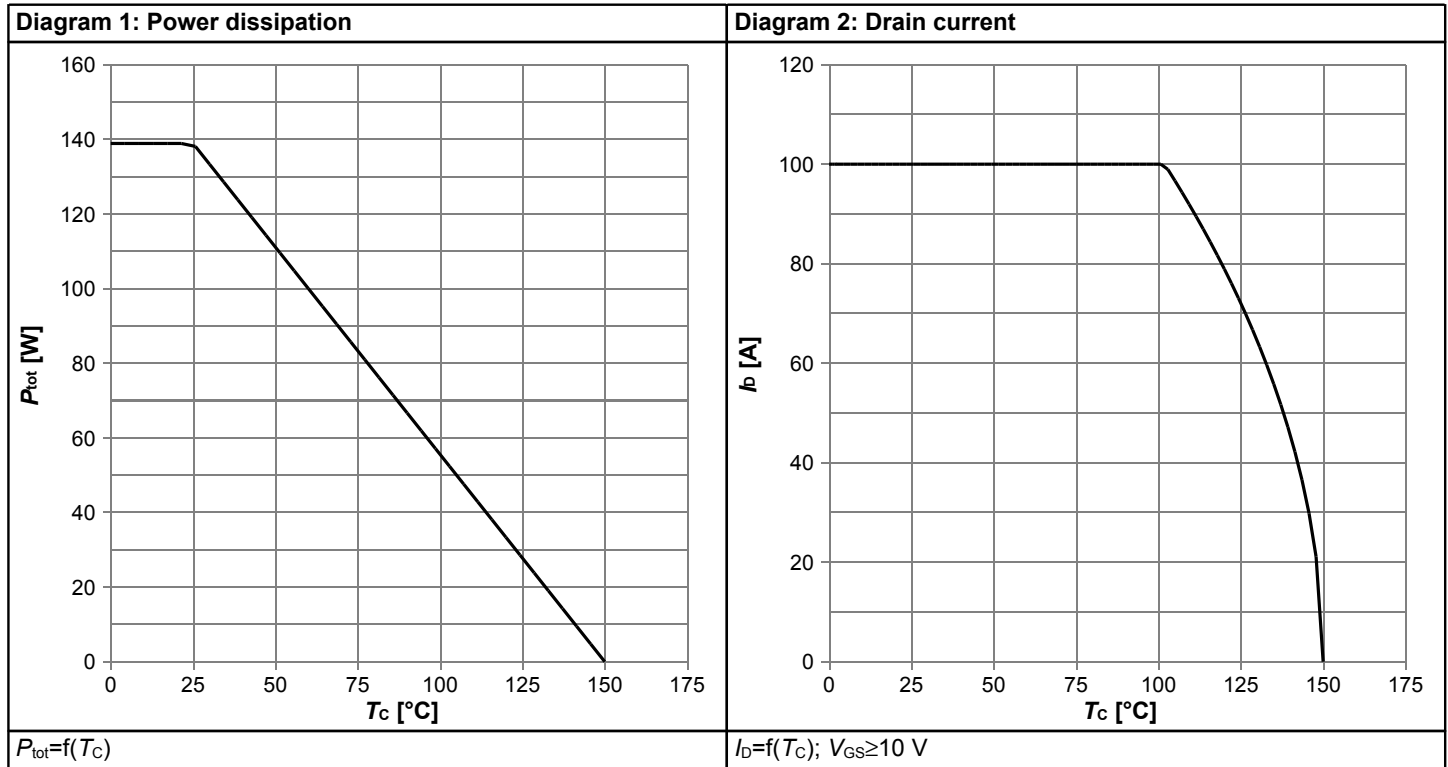
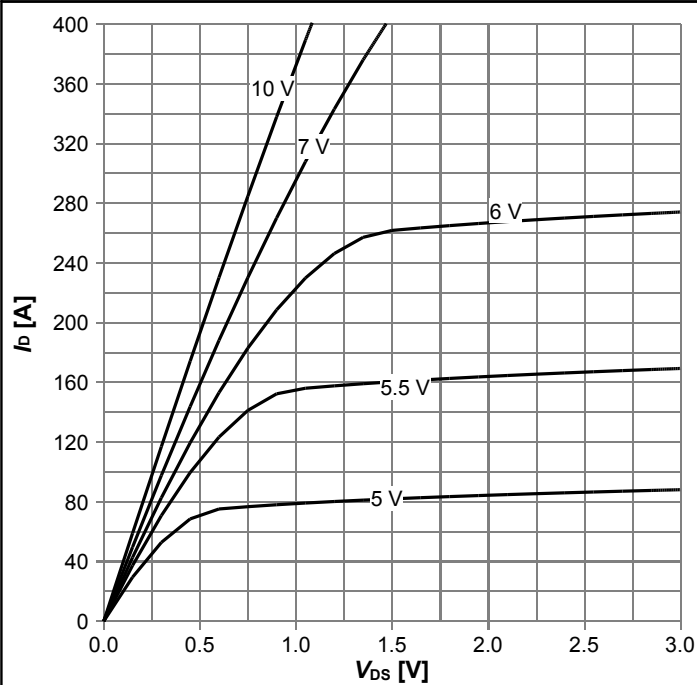
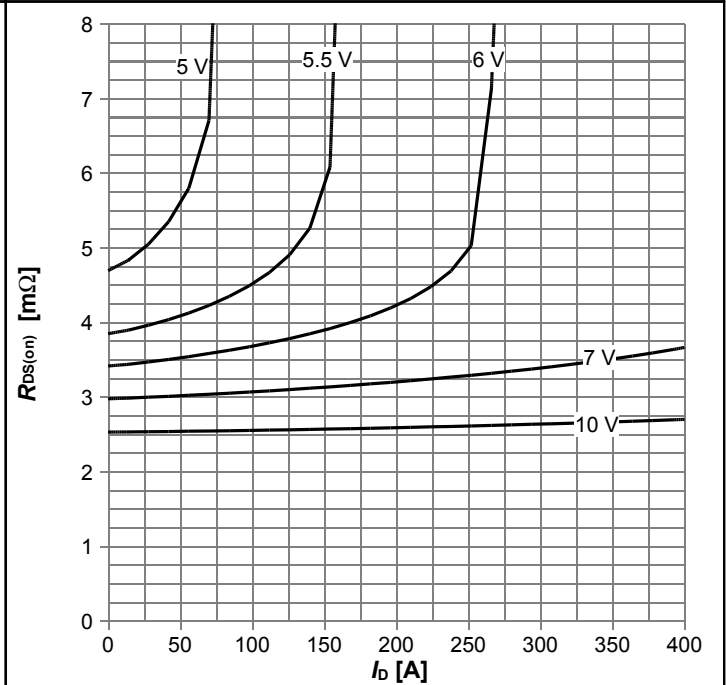


Diagram 5: Typ. output characteristics



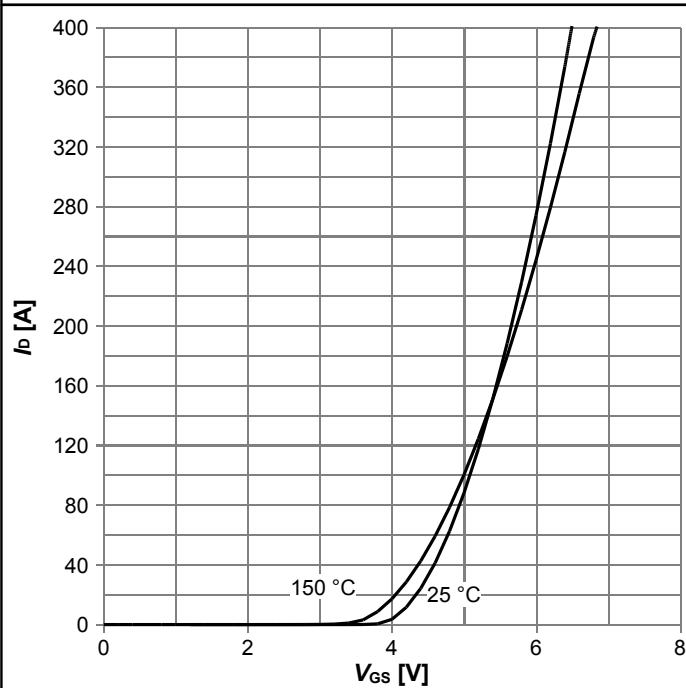
$I_D = f(V_{DS}); T_j = 25^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



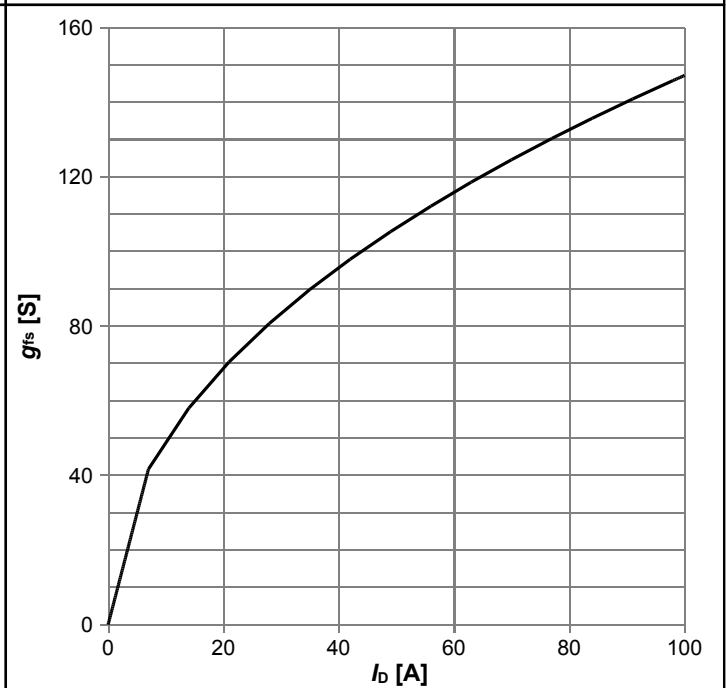
$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

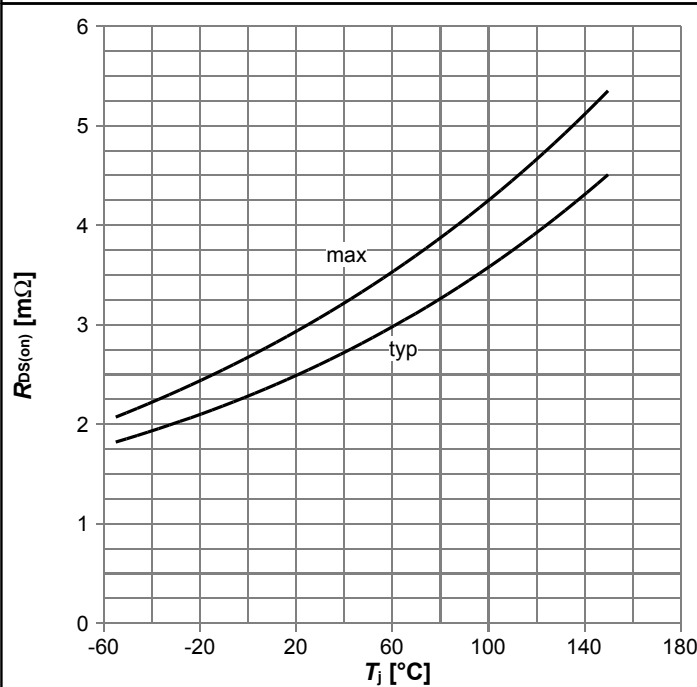
Diagram 8: Typ. forward transconductance



$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

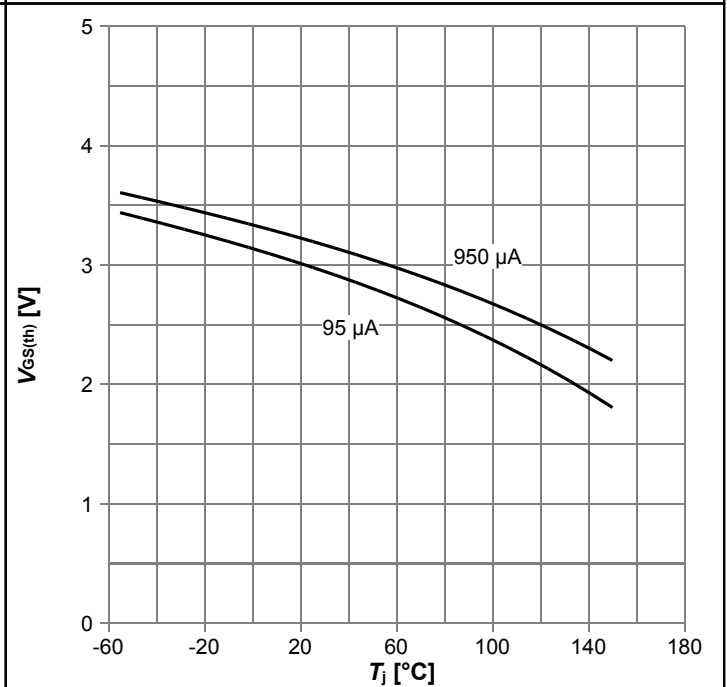


Diagram 9: Drain-source on-state resistance



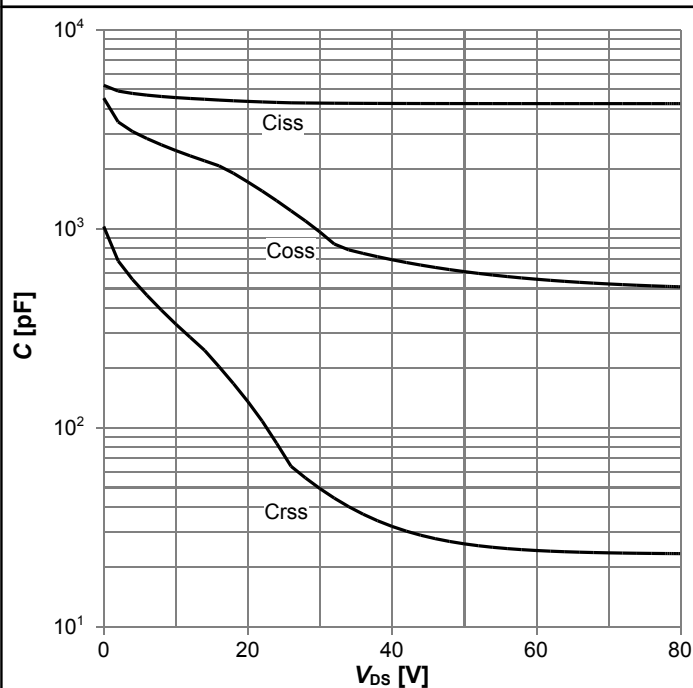
$R_{DS(on)}=f(T_j); I_D=50\text{ A}; V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



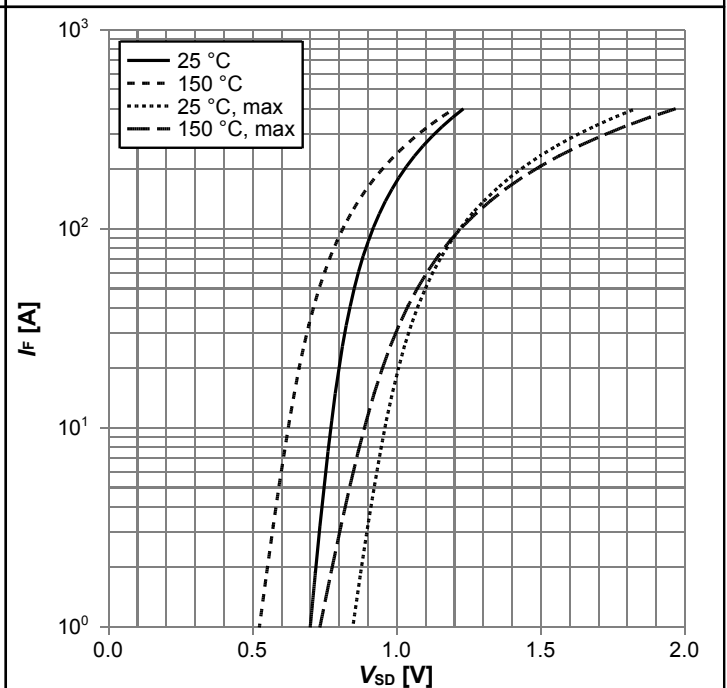
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



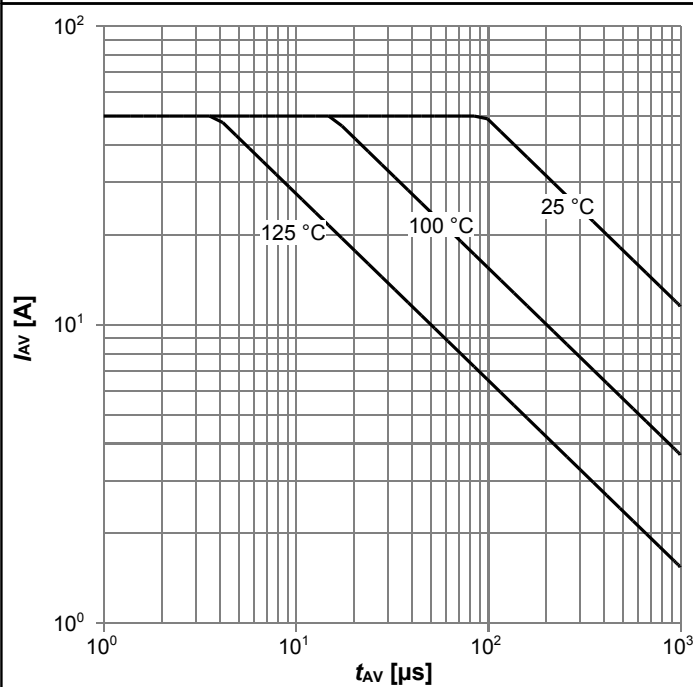
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



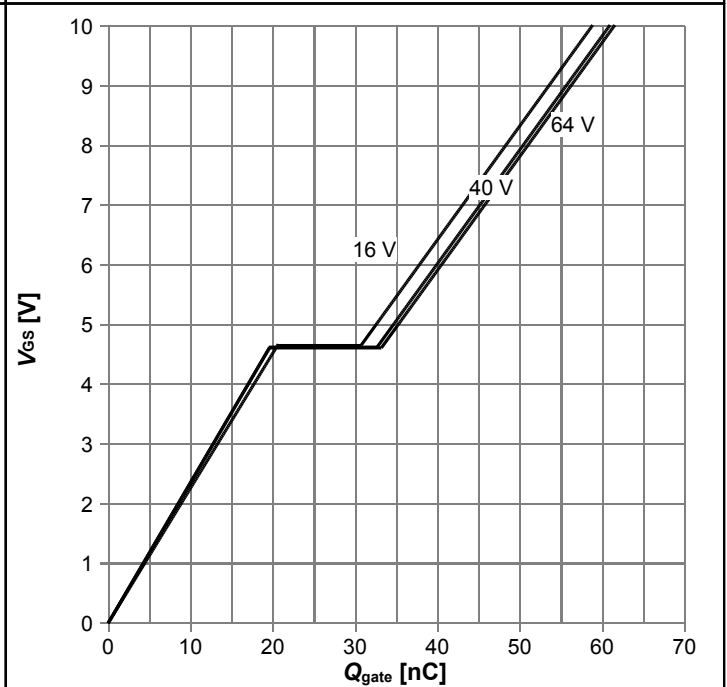
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



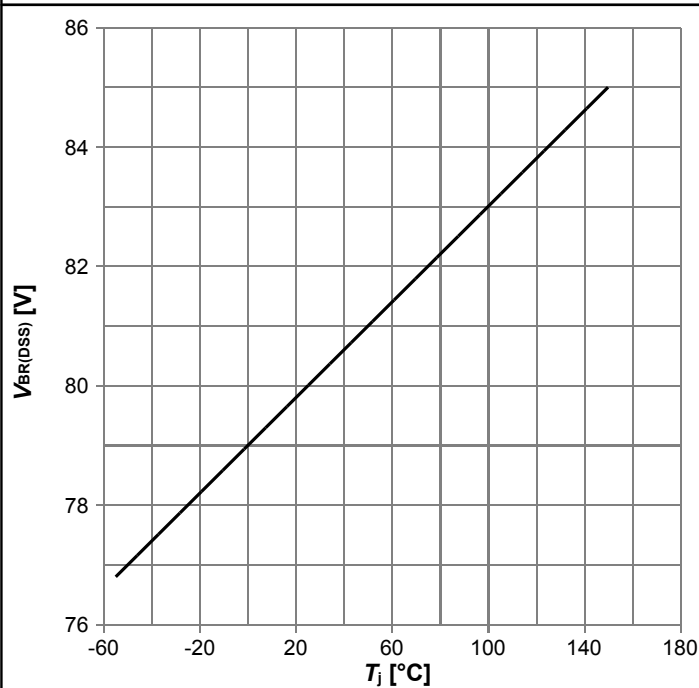
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



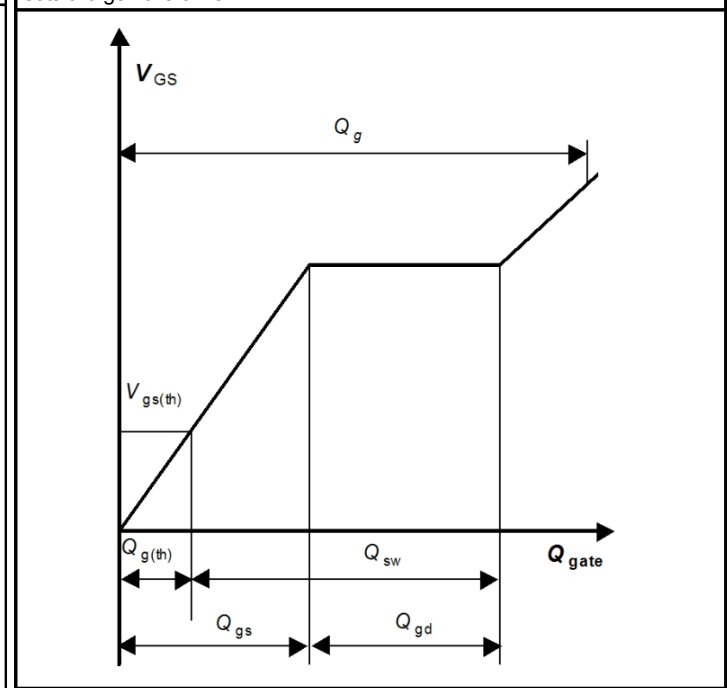
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

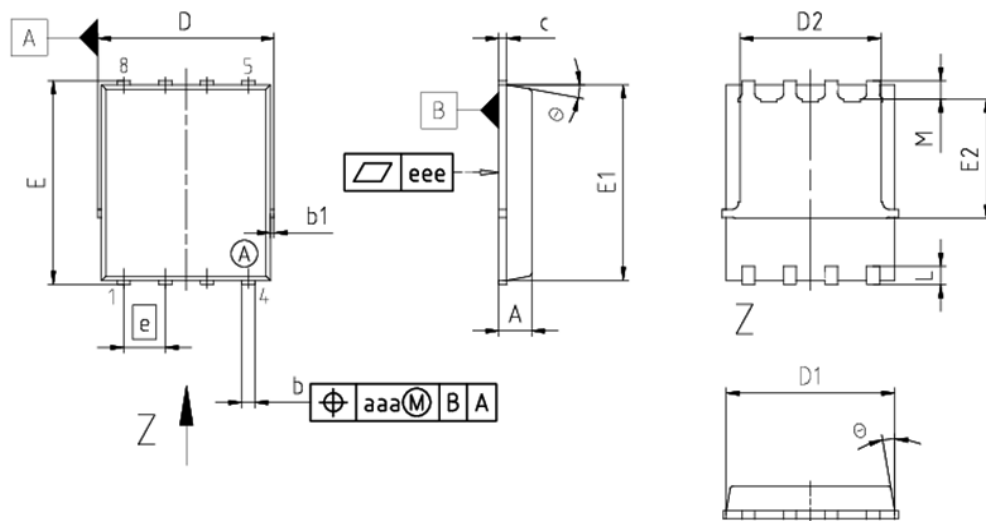


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



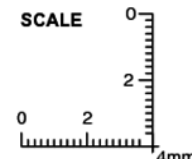
## 6 Package Outlines



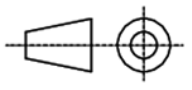
DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
ø	8.5°	12°
aaa	0.25	
eee	0.08	

**DOCUMENT NO.**  
Z8B00003332

**SCALE**



**EUROPEAN PROJECTION**



**ISSUE DATE**  
10-04-2013

**REVISION**  
04

Figure 1 Outline PG-TDSON-8, dimensions in mm

## Revision History

BSC030N08NS5

**Revision: 2014-11-10, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-07-04	Release of final version
2.1	2014-10-14	Rev. 2.1 - Update SOA diagram
2.2	2014-11-10	Rev. 2.2 - Add footnote for Rg and Ciss

### We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

[erratum@infineon.com](mailto:erratum@infineon.com)

### Published by

**Infineon Technologies AG**  
**81726 München, Germany**  
**© 2014 Infineon Technologies AG**  
**All Rights Reserved.**

### Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.