



## 3.3 VOLT TIME SLOT INTERCHANGE DIGITAL SWITCH 4,096 x 4,096

IDT72V70840

### FEATURES:

- 32 serial input and output streams
- 4,096 x 4,096 channel non-blocking switching at 8.192 Mb/s
- Accepts data streams at 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s
- Per-channel Variable Delay Mode for low-latency applications
- Per-channel Constant Delay Mode for frame integrity applications
- Automatic identification of ST-BUS® and GCI serial streams
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel high impedance output control
- Per-channel processor mode to allow microprocessor writes to TX streams
- Direct microprocessor access to all internal memories
- Memory block programming for quick set-up
- IEEE-1149.1 (JTAG) Test Port

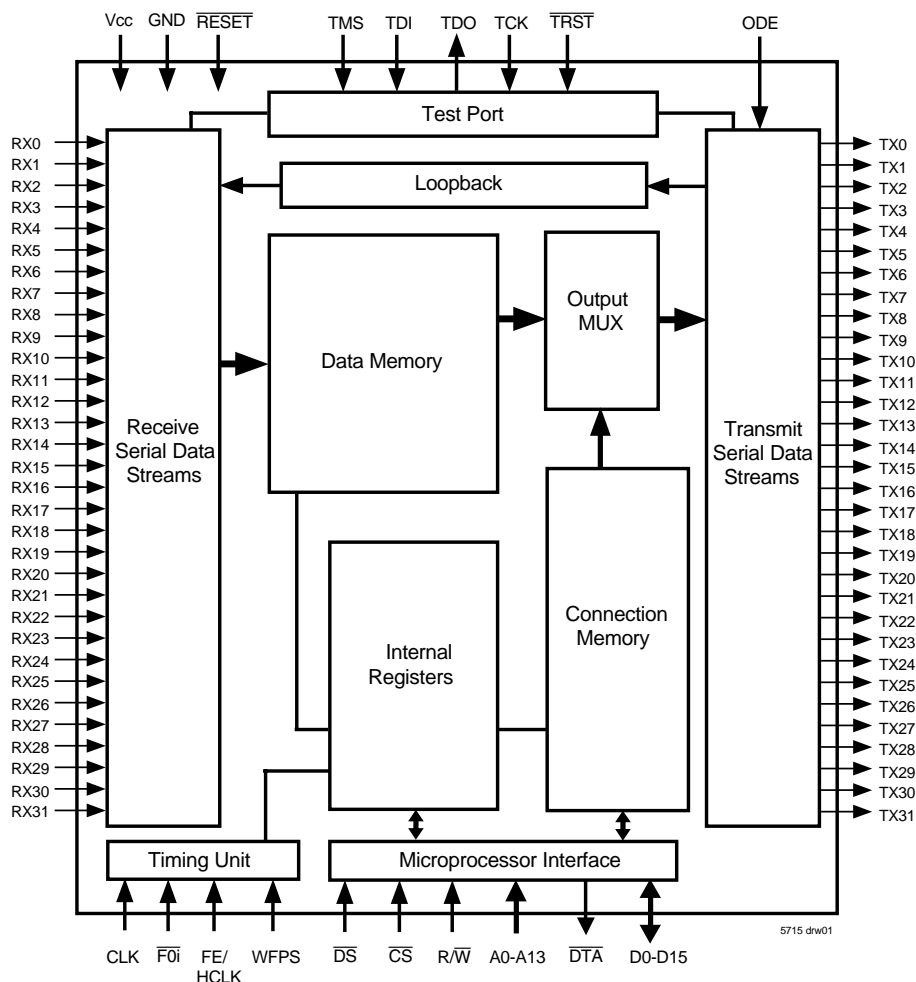
- Internal Loopback for testing
- Available in 144-pin Thin Quad Flatpack (TQFP) and 144-pin Ball Grid Array (BGA) packages
- Operating Temperature Range -40°C to +85°C
- 3.3V I/O with 5V tolerant inputs and TTL compatible outputs

### DESCRIPTION:

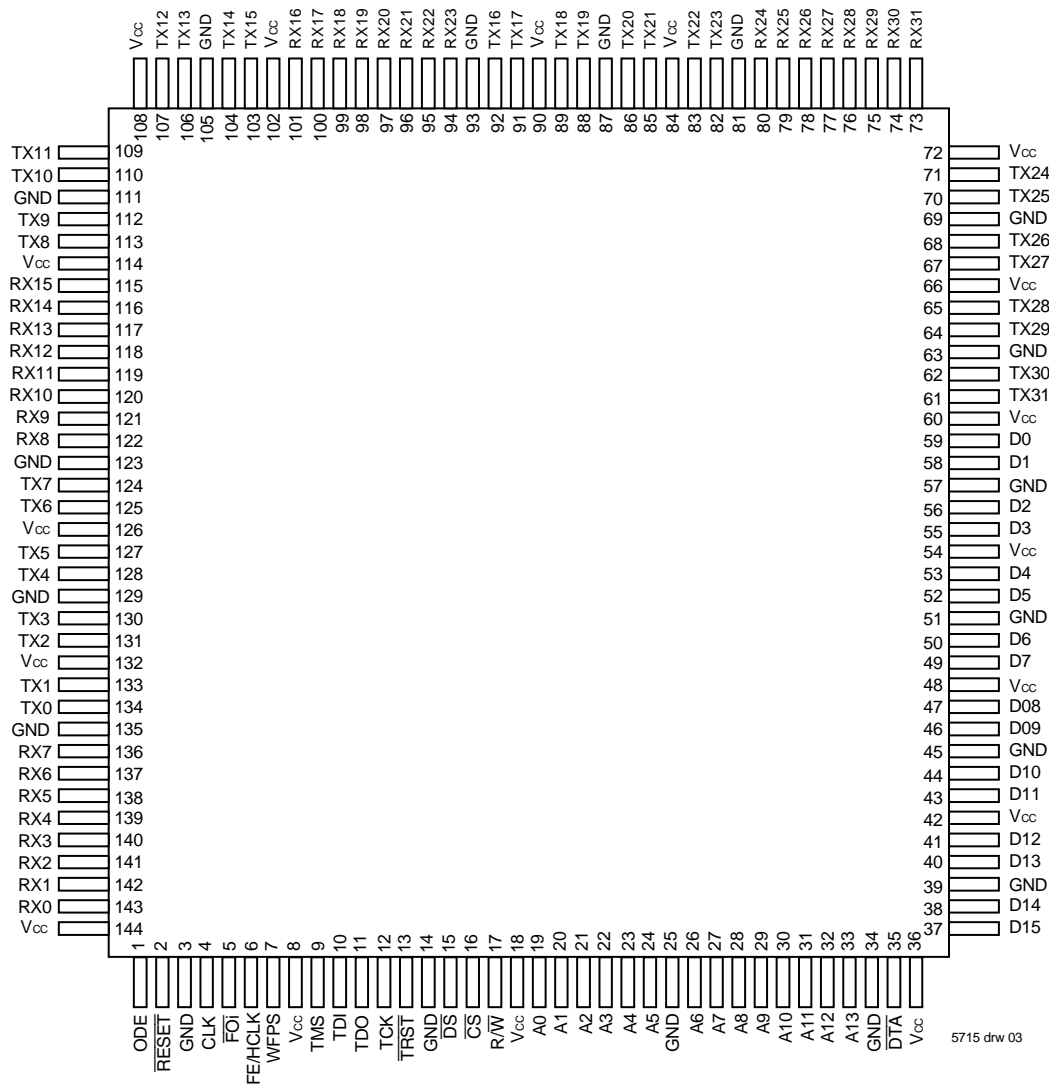
The IDT72V70840 has a non-blocking switch capacity of 1,024 x 1,024 channels at 2.048 Mb/s, 2,048 x 2,048 channels at 4.096 Mb/s, and 4,096 x 4,096 channels at 8.192 Mb/s. With 32 inputs and 32 outputs, programmable per stream control, and a variety of operating modes the IDT72V70840 is designed for the TDM time slot interchange function in either voice or data applications.

Some of the main features of the IDT72V70840 are low power 3.3 Volt operation, automatic ST-BUS®/GCI sensing, memory block programming, simple microprocessor interface, one cycle direct internal memory accesses,

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATIONS



### NOTE:

1. All I/O pins are 5V tolerant except for TMS, TDI and  $\overline{\text{TRST}}$ .

TQFP: 0.50mm pitch, 20mm x 20mm (DA144, order code: DA; DAG 144, order code: DAG)  
TOP VIEW

## PIN DESCRIPTION

| SYMBOL                      | NAME                                       | I/O | DESCRIPTION  |
|-----------------------------|--|-----|--|
| GND                         | Ground.                                    |     | Ground Rail.   |
| Vcc                         | Vcc  |     | +3.3 Volt Power Supply.  |
| TX0-31                      | TX Output 0 to 31<br>(Three-state Outputs) | O   | Serial data output stream. These streams may have a data rate of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s.   |
| RX0-31                      | RX Input 0 to 31                           | I   | Serial data input stream. These streams may have a data rate of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s.  |
| $\overline{F0i}$            | Frame Pulse                                | I   | This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS® and GCI specifications.   |
| FE/HCLK                     | Frame Evaluation/<br>HCLK Clock            | I   | When LOW, this pin is the frame measurement input. When HIGH, the HCLK (4.096 MHz clock) is required for frame alignment in the wide frame pulse (WFP) mode. There is no internal pull-up or pull-down. If this pin is unused, an external pull-up or pull-down must be provided.  |
| CLK                         | Clock                                      | I   | Serial clock for shifting data in/out on the serial streams (RX/TX 0-31). This input accepts a 4.096 MHz clock when data streams @ 2.048 Mb/s, a 8.192 MHz clock when data streams @ 4.096 Mb/s, a 16.384 MHz clock when data streams @ 8.192 Mb/s.  |
| TMS                         | Test Mode Select                           | I   | JTAG signal that controls the state transitions of the TAP controller. This pin is pulled HIGH by an internal pull-up when not driven.   |
| TDI                         | Test Serial Data In                        | I   | JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven.   |
| TDO                         | Test Serial Data Out                       | O   | JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high-impedance state when JTAG scan is not enabled.   |
| TCK                         | Test Clock                                 | I   | Provides the clock to the JTAG test logic.   |
| $\overline{TRST}$           | Test Reset                                 | I   | Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the IDT72V70840 is in the normal functional mode.  |
| $\overline{RESET}$          | Device Reset<br>(Schmitt Trigger Input)    | I   | This input (active LOW) puts the IDT72V70840 in its reset state that clears the device internal counters, registers and brings TX0-31 and microport data outputs to a high-impedance state. The time constant for a power up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the $\overline{RESET}$ pin must be held LOW for a minimum of 100ns to reset the device. |
| WFPS                        | Wide Frame Pulse Select                    | I   | When 1, enables the wide frame pulse (SFP) Frame Alignment interface. When 0, the device operates in ST-BUS® /GCI mode.  |
| $\overline{DS}$             | Data Strobe                                | I   | This active LOW input works in conjunction with $\overline{CS}$ to enable the read and write operations.   |
| $\overline{R/\overline{W}}$ | Read/Write                                 | I   | This input controls the direction of the data bus lines during a microprocessor access.  |
| $\overline{CS}$             | Chip Select                                | I   | Active LOW input used by a microprocessor to activate the microprocessor port of IDT72V70840.  |
| A0-13                       | Address Bus 0 to 13                        | I   | These pins allow direct access to Connection Memory, Data Memory and internal control registers.   |
| D0-15                       | Data Bus 0-15                              | I/O | These pins are the data bits of the microprocessor port.   |
| $\overline{DTA}$            | Data Transfer<br>Acknowledgment            | O   | This active LOW signal indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then goes high-impedance, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is in high-impedance.   |
| ODE                         | Output Drive Enable                        | I   | This is the output enable control for the TX0-31 serial outputs. When ODE input is LOW and the OSB bit of the CR register is LOW, TX0-31 are in a high-impedance state. If this input is HIGH, the TX0-31 output drivers are enabled. However, each channel may still be put into a high-impedance state by using the per channel control bit in the connection memory.  |

## DESCRIPTION (CONTINUED)

JTAG Test Access Port (TAP) and per stream programmable input offset delay, variable or constant throughput modes, internal loopback, output enable, and Processor Mode.

The IDT72V70840 is capable of switching up to 4,096 x 4,096 channels without blocking. Designed to switch 64 Kbit/s PCM or N x 64 Kbit/s data, the device maintains frame integrity in data applications and minimizes throughput delay for voice applications on a per channel basis.

The 32 serial input streams (RX) of the IDT72V70840 can be run up to 8.192 Mb/s allowing 128 channels per 125  $\mu$ s frame. The data rates on the output streams (TX) are identical to those on the input stream.

With two main operating modes, Processor Mode and Connection Mode, the IDT72V70840 can easily switch data from incoming serial streams (Data Memory) or from the controlling microprocessor (Connection Memory). As control and status information is critical in data transmission, the Processor Mode is especially useful when there are multiple devices sharing the input and output streams.

With data coming from multiple sources and through different paths, data entering the device is often delayed. To handle this problem, the IDT72V70840 has a frame evaluation feature to allow individual streams to be offset from the frame pulse in half clock-cycle intervals up to +4.5 clock cycles.

The IDT72V70840 also provides a JTAG test access port, an internal loopback feature, memory block programming, a simple microprocessor interface and automatic ST-BUS<sup>®</sup>/GCI sensing to shorten setup time, aid in debugging and ease use of the device without sacrificing capabilities.

## FUNCTIONAL DESCRIPTION

### DATA AND CONNECTION MEMORY

All data that comes in through the RX inputs go through a serial-to-parallel conversion before being stored into internal Data Memory. The 8 KHz frame pulse ( $\overline{FOI}$ ) is used to mark the 125  $\mu$ s frame boundaries and to sequentially address the input channels in Data Memory.

Data output on the TX streams may come from either the Serial Input Streams (Data Memory) or from the microprocessor (Connection Memory). In the case that RX input data is to be output, the addresses in connection memory are used to specify a stream and channel of the input. The connection memory is setup in such a way that each location corresponds to an output channel for each particular stream. In that way, more than one channel can output the same data.

In Processor Mode, the microprocessor writes data to the connection memory locations corresponding to the stream and channel that is to be output. The lower half (8 least significant bits) of the connection memory is output every frame until the microprocessor changes the data or mode of the channel. By using this Processor Mode capability, the microprocessor can access input and output time-slots on a per channel basis.

The four most significant bits of the connection memory are used to control per channel functions of the output streams. Specifically, there are bits for Processor or Connection mode, Constant or Variable delay, enables or disables of output drivers, and controls for the Loopback function.

If the per channel OE is set to zero, only that particular channel (8-bits) will be in the high-impedance state. If however, the ODE input pin is low or the Output Standby Bit (OSB) in the Control Register is low, all of the outputs will be in a high-impedance state even if a particular channel in connection memory has enabled the output for that channel. In other words, the ODE pin and OSB control bit are master output enables for the device (Table 3).

### SERIAL DATA INTERFACE TIMING

The master clock frequency must always be twice the data rate, e.g. for a serial data rates of 2.048 Mb/s, the master clock (CLK) must be at 4.096 MHz. The input and output stream data rates will always be identical. See control register bits DR1-0 description (Table 5) for data and clock rate selections.

The IDT72V70840 provides two different interface timing modes, ST-BUS<sup>®</sup> or GCI. The IDT72V70840 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS<sup>®</sup> or GCI. In ST-BUS<sup>®</sup> format, every second falling edge of the master clock marks a bit boundary and the data is clocked in on the rising edge of CLK, three quarters of the way into the bit cell. In GCI format, every second rising edge of the master clock marks the bit boundary and data is clocked in on the falling edge of CLK at three quarters of the way into the bit cell.

### INPUT FRAME OFFSET SELECTION

Input frame offset selection allows the channel alignment of individual input streams to be offset with respect to the output stream channel alignment (i.e.  $\overline{FOI}$ ). Although all input data comes in at the same speed, delays can be caused by variable path serial backplanes and variable path lengths which may be implemented in large centralized and distributed switching systems. Because data is often delayed this feature is useful in compensating for the skew between clocks.

Each input stream can have its own delay offset value by programming the frame input offset registers (FOR, Table 8). The maximum allowable skew is +4 master clock (CLK) periods forward with a resolution of 1/2 clock period. The output frame offset cannot be offset or adjusted.

### SERIAL INPUT FRAME ALIGNMENT EVALUATION

The IDT72V70840 provides the frame evaluation (FE) input to determine different data input delays with respect to the frame pulse  $\overline{FOI}$ .

A measurement cycle is started by setting the start frame evaluation (SFE) bit low for at least one frame. When the SFE bit in the Control Register is changed from low to high, the evaluation starts. Two frames later, the complete frame evaluation (CFE) bit of the frame alignment register (FAR) changes from low to high to signal that a valid offset measurement is ready to be read from bits 0 to 11 of the FAR register. The SFE bit must be set to zero before a new measurement cycle is started.

In ST-BUS<sup>®</sup> mode, the falling edge of the frame measurement signal (FE) is evaluated against the falling edge of the ST-BUS<sup>®</sup> frame pulse. In GCI mode, the rising edge of FE is evaluated against the rising edge of the GCI frame pulse. See Table 7 and Figure 1 for the description of the frame alignment register.

### MEMORY BLOCK PROGRAMMING

The IDT72V70840 provides users with the capability of initializing the entire connection memory block in two frames. To set bits 12 to 15 of every connection memory location, first program the desired pattern in bits 5 to 8 of the Control Register.

The block programming mode is enabled by setting the memory block program (MBP) bit of the control register high. When the block programming enable (BPE) bit of the Control Register is set to high, the block programming data will be loaded into the bits 12 to 15 of every connection memory location. The other connection memory bits (bit 0 to bit 11) are loaded with zeros. When the memory block programming is complete, the device resets the BPE bit to zero.

## LOOPBACK CONTROL

The loopback control (LPBK) bit of each connection memory location allows the TX output data to be looped back internally to the RX input for diagnostic purposes.

If the LPBK bit is high, the associated TX output channel data is internally looped back to the RX input channel (i.e., data from TXn channel m routes to the RXn channel m internally); if the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of frame delay offset registers must be set to zero.

## DELAY THROUGH THE IDT72V70840

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, variable throughput delay is best as it ensures minimum delay between input and output data. In wideband data applications, constant throughput delay is best as the frame integrity of the information is maintained through the switch.

The delay through the device varies according to the type of throughput delay selected in the  $\bar{V}/C$  bit of the connection memory.

### VARIABLE DELAY MODE ( $\bar{V}/C$ BIT = 0)

In this mode, the delay is dependent only on the combination of source and destination channels and is independent of input and output streams. The minimum delay achievable in the IDT72V70840 is three time-slots. If the input channel data is switched to the same output channel (channel n, frame p), it will be output in the following frame (channel n, frame p+1). The same is true if the input channel n is switched to output channel n+1 or n+2. If the input channel n is switched to output channel n+3, n+4, ..., the new output data will appear in the same frame. Table 2 shows the possible delays for the IDT72V70840 in the variable delay mode.

### CONSTANT DELAY MODE ( $\bar{V}/C$ BIT = 1)

In this mode, frame integrity is maintained in all switching configurations by making use of a multiple data memory buffer. Input channel data is written into the data memory buffers during frame n will be read out during frame n+2. In the IDT72V70840, the minimum throughput delay achievable in the constant delay mode will be one frame. For example, when input time-slot 31 is switched to output time-slot 0. The maximum delay of 94 time-slots of delay occurs when time-slot 0 in a frame is switched to time-slot 31 in the frame.

## MICROPROCESSOR INTERFACE

The IDT72V70840's microprocessor interface looks like a standard RAM interface to improve integration into a system. With a 12-bit address bus and a 16-bit data bus, read and writes are mapped directly into Data and Connection memories and require only one cycle to access. By allowing the internal memories to be randomly accessed in one cycle, the controlling microprocessor has more time to manage other peripheral devices and can more easily and quickly gather information and setup the switch paths.

Table 4 shows the mapping of the addresses into internal memory blocks and Table 5 shows the Control Register information.

## MEMORY MAPPING

The address bus on the microprocessor interface selects the internal registers and memories of the IDT72V70840.

The two most significant bits of the address select between the registers, Data Memory, and Connection Memory. If A13 and A12 are HIGH, A11-A0 are used to address the Data Memory. If A13 is HIGH and A12 is LOW, A11-A0 are used to address Connection Memory. If A13 is LOW and A12 is HIGH A11-A0 are used to select the Control Register, Frame Alignment Register, and Frame Offset Registers. See Table 4 for mappings.

As explained in the Serial Data Interface Timing and Switching Configurations sections, after system power-up, the Control Register should be programmed immediately to establish the desired switching configuration.

The data in the Control Register consists of the Memory Block Programming bit (MBP), the Block Programming Data (BPE) bits, the Begin Block Programming Enable (BPE), the Output Stand By, Start Frame Evaluation, and Data Rate Select bits. As explained in the Memory Block Programming section, the BPE begins the programming if the MBP bit is enabled. This allows the entire connection memory block to be programmed with the Block Programming Data bits. If the ODE pin is low, the OSB bit enables (if high) or disables (if low) all TX output drivers. If the ODE pin is high, the contents of the OSB bit is ignored and all TX output drivers are enabled.

## CONNECTION MEMORY CONTROL

If the ODE pin or the OSB bit is high, the OE bit of each connection memory location controls the output drivers-enables (if high) or disables (if low). See Table 3 for detail.

The Processor Channel (PC) bit of the Connection Memory selects between Processor Mode and Connection Mode. If high, the contents of the Connection Memory are output on the TX streams. If low, the Stream Address Bit (SAB) and the Channel Address Bit (CAB) of the Connection Memory defines the source information (stream and channel) of the time-slot that will be switched to the output from Data Memory.

Also in the Connection Memory is the  $\bar{V}/C$  (Variable/Constant Delay) bit. Each Connection Memory location allows the per-channel selection between variable and constant throughput delay modes.

If the LPBK bit is high, the associated TX output channel data is internally looped back to the RX input channel (i.e., RXn channel m data comes from the TXn channel m). If the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of the frame delay offset registers must be set to zero.

## INITIALIZATION OF THE IDT72V70840

After power up, the state of the connection memory is unknown. As such, the outputs should be put in high impedance by holding the ODE low. While the ODE is low, the microprocessor can initialize the device, program the active paths, and disable unused outputs by programming the OE bit in connection memory. Once the device is configured, the ODE pin (or OSB bit depending on initialization) can be switched.

**TABLE 1 — CONSTANT THROUGHPUT  
DELAY VALUE**

| Input Rate | Delay for Constant Throughput Delay Mode<br>(m – output channel number)<br>(n – input channel number) |
|------------|---|
| 2.048 Mb/s | $32 + (32 - n) + m$ time-slots  |
| 4.096 Mb/s | $64 + (64 - n) + m$ time-slots  |
| 8.192 Mb/s | $128 + (128 - n) + m$ time-slots  |

**TABLE 2 — VARIABLE THROUGHPUT DELAY VALUE**

| Input Rate | Delay for Variable Throughput Delay Mode<br>(m – output channel number; n – input channel number) |                            |                      |
|------------|---|----------------------------|----------------------|
|            | m < n   | m = n, n+1, n+2            | m > n+2              |
| 2.048 Mb/s | $32 - (n - m)$ time-slots   | $(m - n + 32)$ time-slots  | $(m - n)$ time-slots |
| 4.096 Mb/s | $64 - (n - m)$ time-slots   | $(m - n + 64)$ time-slots  | $(m - n)$ time-slots |
| 8.192 Mb/s | $128 - (n - m)$ time-slots  | $(m - n + 128)$ time-slots | $(m - n)$ time-slots |

**TABLE 3 — OUTPUT HIGH IMPEDANCE CONTROL**

| OE bit in Connection<br>Memory | ODE pin    | OSB bit in CR<br>Register | TX Stream Output<br>Status    |
|--------------------------------|------------|---------------------------|-------------------------------|
| 0                              | Don't Care | Don't Care                | Per Channel<br>High-Impedance |
| 1                              | 0          | 0                         | High-Impedance                |
| 1                              | 0          | 1                         | Enable                        |
| 1                              | 1          | 0                         | Enable                        |
| 1                              | 1          | 1                         | Enable                        |

**TABLE 4 — INTERNAL REGISTER AND ADDRESS MEMORY MAPPING**

| A13 | A12 | A11  | A10  | A9   | A8   | A7   | A6  | A5  | A4  | A3  | A2  | A1  | A0  | RW  | Location             |
|-----|-----|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|----------------------|
| 1   | 1   | STA4 | STA3 | STA2 | STA1 | STA0 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | R   | Data Memory          |
| 1   | 0   | STA4 | STA3 | STA2 | STA1 | STA0 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | R/W | Connect. Memory      |
| 0   | 1   | 0    | 0    | 0    | 0    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | Control Register     |
| 0   | 1   | 0    | 0    | 0    | 1    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | Frame Align Register |
| 0   | 1   | 0    | 0    | 1    | 0    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR0                 |
| 0   | 1   | 0    | 0    | 1    | 1    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR1                 |
| 0   | 1   | 0    | 1    | 0    | 0    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR2                 |
| 0   | 1   | 0    | 1    | 0    | 1    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR3                 |
| 0   | 1   | 0    | 1    | 1    | 0    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR4                 |
| 0   | 1   | 0    | 1    | 1    | 1    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR5                 |
| 0   | 1   | 1    | 0    | 0    | 0    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR6                 |
| 0   | 1   | 1    | 0    | 0    | 1    | x    | x   | x   | x   | x   | x   | x   | x   | R/W | FOR7                 |



**TABLE 5 — CONTROL REGISTER (CR) BITS**

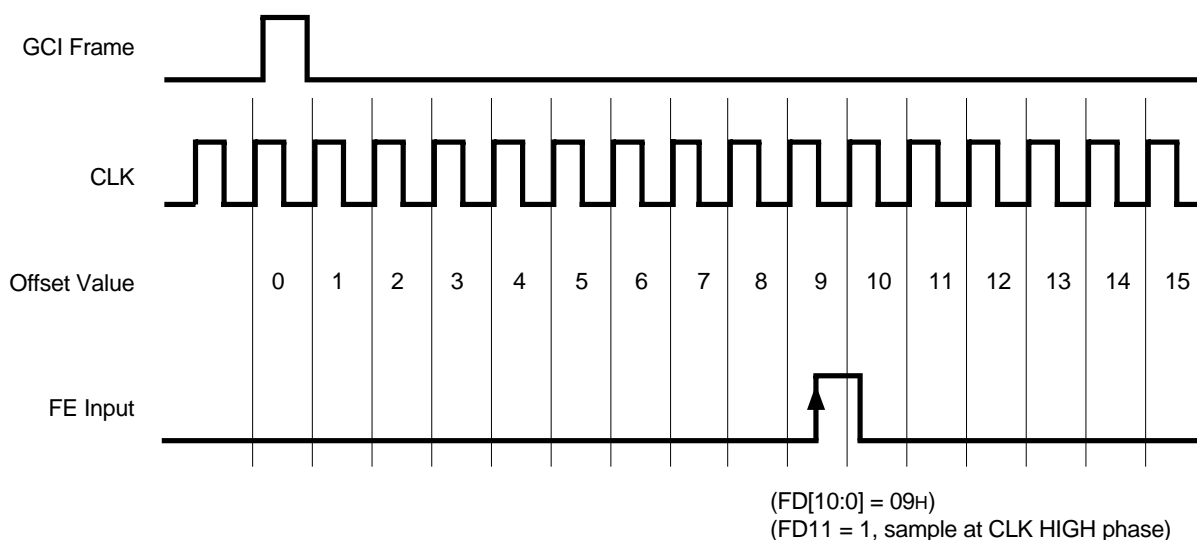
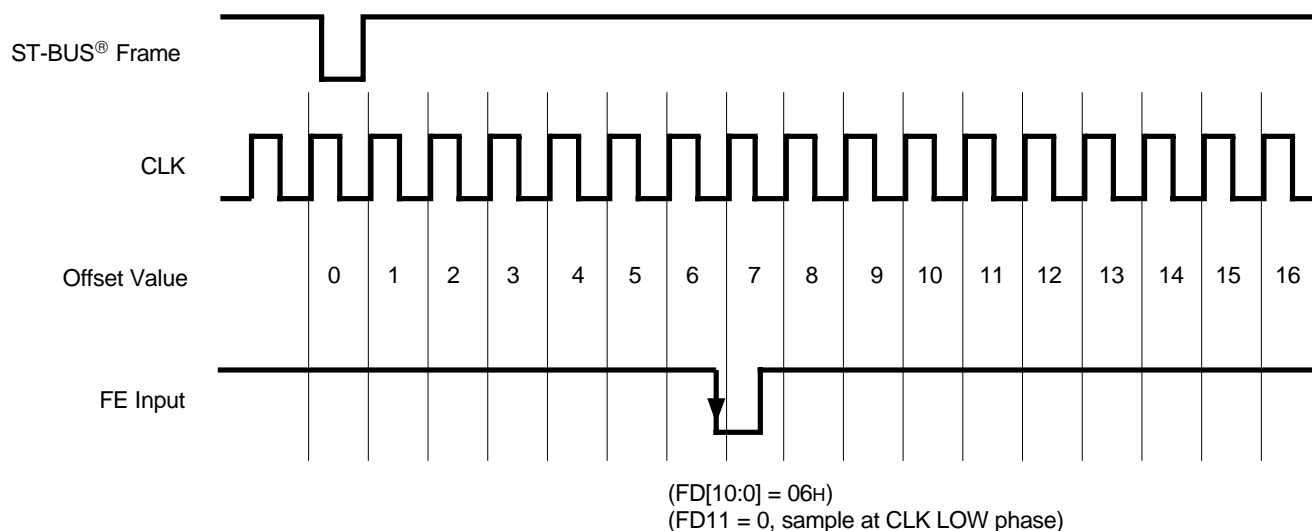
| Reset Value: |   | 0000H. |   |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
|--------------|---|--------|---|----|-----|----|------------|------|------|------|--------------|-----|-----|-----|-----|-----|--|
|              | 15                                      | 14     | 13  | 12 | 11  | 10 | 9          | 8    | 7    | 6    | 5            | 4   | 3   | 2   | 1   | 0   |  |
|              | 0                                       | 0      | 0   | 0  | 0   | 0  | MBP        | BPD3 | BPD2 | BPD1 | BPD0         | BPE | OSB | SFE | DR1 | DR0 |  |
| Bit          | Name                                    |        | Description   |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
| 15-10        | Unused                                  |        | Must be zero for normal operation.  |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
| 9            | MBP<br>(Memory Block Program)           |        | When 1, the connection memory block programming feature is ready for the programming of Connection Memory high bits, bit 11 to bit 15. When 0, this feature is disabled.  |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
| 8-5          | BPD3-0<br>(Block Programming Data)      |        | These bits carry the value to be loaded into the connection memory block whenever the memory block programming feature is activated. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of the bits BPD3-0 are loaded into bit 15 and 12 of the connection memory. Bit 11 to bit 0 of the connection memory are set to 0.  |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
| 4            | BPE<br>(Begin Block Programming Enable) |        | A zero to one transition of this bit enables the memory block programming function. The BPE and BPD4-0 bits in the CR register have to be defined in the same write operation. Once the BPE bit is set HIGH, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE = 1, the BPE or MBP can be set to 0 to abort to ensure proper operation. When BPE = 1, the other bit in the CR register must not be changed for two frames to ensure proper operation. |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
| 3            | OSB<br>(Output Stand By)                |        | When ODE = 0 and OSB = 0, the output drivers of TX0 to TX31 are in high impedance mode. When ODE = 0 and OSB = 1, the output driver of TX0 to TX31 function normally. When ODE = 1, TX0 to TX31 output drivers function normally.   |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
| 2            | SFE<br>(Start Frame Evaluation)         |        | A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the FAR register changes from zero to one, the evaluation procedure stops. To start another frame evaluation cycle, set this bit to zero for at least one frame.  |    |     |    |            |      |      |      |              |     |     |     |     |     |  |
| 1-0          | DR1-0<br>(Data Rate Select)             |        | DR1   |    | DR0 |    | Data Rate  |      |      |      | Master Clock |     |     |     |     |     |  |
|              |   |        | 0   |    | 0   |    | 2.048 Mb/s |      |      |      | 4.096 MHz    |     |     |     |     |     |  |
|              |   |        | 0   |    | 1   |    | 4.096 Mb/s |      |      |      | 8.192 MHz    |     |     |     |     |     |  |
|              |   |        | 1   |    | 0   |    | 8.192 Mb/s |      |      |      | 16.384 MHz   |     |     |     |     |     |  |
|              |   |        | 1   |    | 1   |    | Reserved   |      |      |      | Reserved     |     |     |     |     |     |  |

**TABLE 6 — CONNECTION MEMORY BITS**

|      | 15   | 14          | 13   | 12 | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |  |
|------|--|-------------|--|----|------|------|------|------|------|------|------|------|------|------|------|------|--|
|      | LPBK   | $\bar{V}/C$ | PC   | OE | SAB4 | SAB3 | SAB2 | SAB1 | SAB0 | CAB6 | CAB5 | CAB4 | CAB3 | CAB2 | CAB1 | CAB0 |  |
| Bit  | Name   |             | Description  |    |      |      |      |      |      |      |      |      |      |      |      |      |  |
| 15   | LPBK<br>(Per Channel Loopback)                   |             | When 1, the RX n channel m data comes from the TX n channel m. For proper per channel loopback operations, set the delay offset register bits OFn[2:0] to zero for the streams which are in the loopback mode.   |    |      |      |      |      |      |      |      |      |      |      |      |      |  |
| 14   | $\bar{V}/C$ (Variable/Constant Throughput Delay) |             | This bit is used to select between the variable (LOW) and constant delay (HIGH) mode on a per-channel basis.   |    |      |      |      |      |      |      |      |      |      |      |      |      |  |
| 13   | PC<br>(Processor Channel)                        |             | When 1, the contents of the connection memory are output on the corresponding output channel and stream. Only the lower byte (bit 7 – bit 0) will be output to the TX output pins. When 0, the contents of the connection memory are the data memory address of the switched input channel and stream. |    |      |      |      |      |      |      |      |      |      |      |      |      |  |
| 12   | OE<br>(Output Enable)                            |             | This bit enables the TX output drivers on a per-channel basis. When 1, the output driver functions normally. When 0, the output driver is in a high-impedance state.   |    |      |      |      |      |      |      |      |      |      |      |      |      |  |
| 11-7 | SAB4-0 (Source Stream Address Bits)              |             | The binary value is the number of the data stream for the source of the connection.  |    |      |      |      |      |      |      |      |      |      |      |      |      |  |
| 6-0  | CAB6-0 (Source Channel Address Bits)             |             | The binary value is the number of the channel for the source of the connection.  |    |      |      |      |      |      |      |      |      |      |      |      |      |  |

**TABLE 7 — FRAME ALIGNMENT REGISTER (FAR) BITS**

|  |                                 |   |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
|--|---------------------------------|---|-----|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|--|---|---|---|-----|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Reset Value:   |                                 | 0000 <sub>H</sub> .   |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
| 15   | 14                              | 13  | 12  | 11   | 10   | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
| <table><tr><td>0</td><td>0</td><td>0</td><td>CFE</td><td>FD11</td><td>FD10</td><td>FD9</td><td>FD8</td><td>FD7</td><td>FD6</td><td>FD5</td><td>FD4</td><td>FD3</td><td>FD2</td><td>FD1</td><td>FD0</td></tr></table> |                                 |   |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  | 0 | 0 | 0 | CFE | FD11 | FD10 | FD9 | FD8 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 |
| 0  | 0                               | 0   | CFE | FD11 | FD10 | FD9 | FD8 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
| Bit  | Name                            | Description   |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
| 15-13  | Unused                          | Must be zero for normal operation   |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
| 12   | CFE (Complete Frame Evaluation) | When CFE = 1, the frame evaluation is completed and bits FD10 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when SFE bit in the CR register is changed from 1 to 0.   |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
| 11   | FD11 (Frame Delay Bit 11)       | The falling edge of FE (or rising edge for GCI mode) is sampled during the CLK-high phase (FD11 = 1) or during the CLK-low phase (FD11 = 0). This bit allows the measurement resolution to ½ CLK cycle. |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |
| 10-0   | FD10-0 (Frame Delay Bits)       | The binary value expressed in these bits refers to the measured input offset value. These bits are reset to zero when the SFE bit of the CR register changes from 1 to 0. (FD10 – MSB, FD0 – LSB)       |     |      |      |     |     |     |     |     |     |     |     |     |     |  |  |   |   |   |     |      |      |     |     |     |     |     |     |     |     |     |     |



*Figure 1. Example for Frame Alignment Measurement*

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**TABLE 8 — FRAME INPUT OFFSET REGISTER (FOR) BITS**

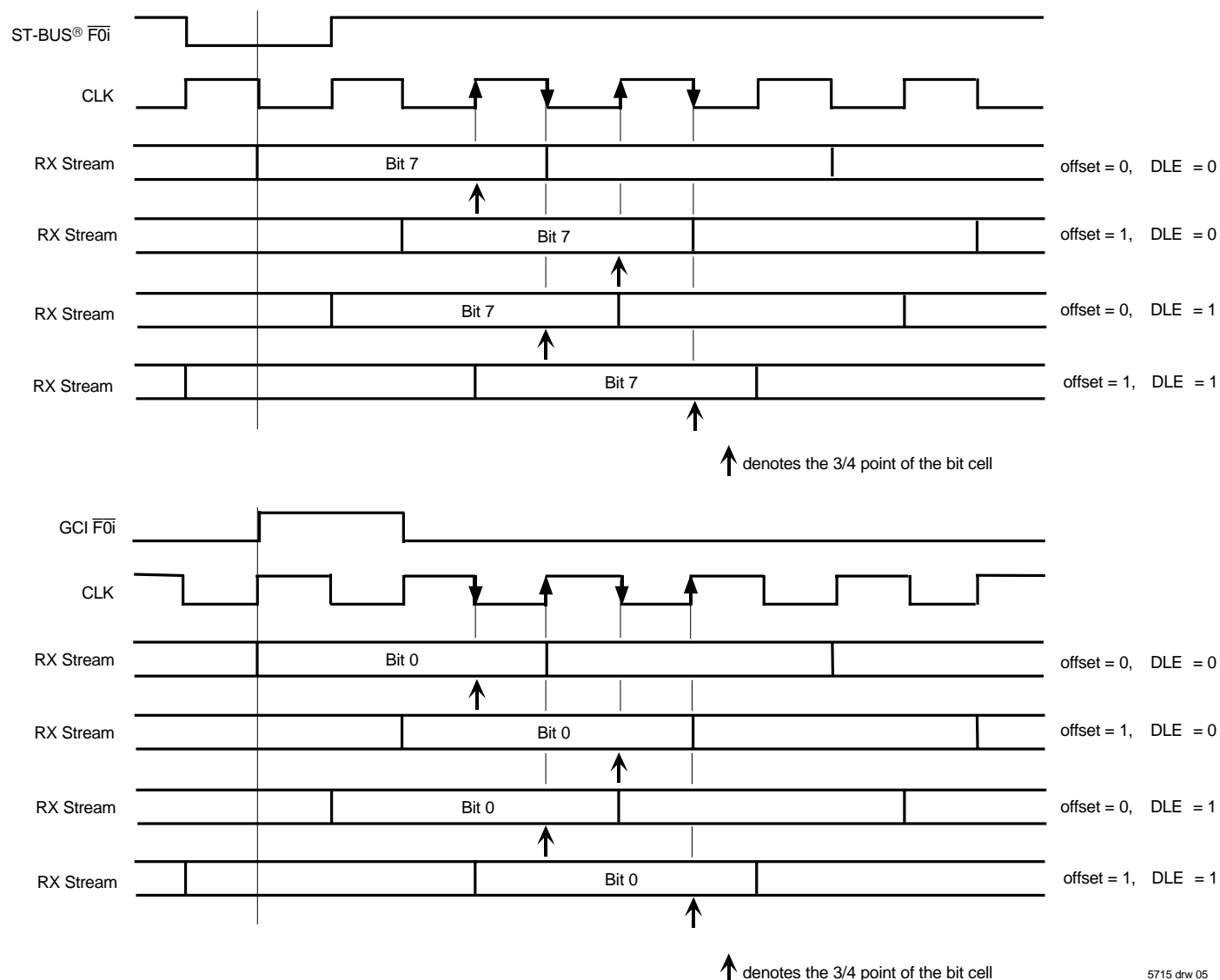
| Reset Value: 0000 <sub>H</sub> for all FOR registers.   |   |
|---|---|
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF32 OF31 OF30 DLE3 OF22 OF21 OF20 DLE2 OF12 OF11 OF10 DLE1 OF02 OF01 OF00 DLE0</div> </div> </div>                 |   |
| FOR0 Register   |   |
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF72 OF71 OF70 DLE7 OF62 OF61 OF60 DLE6 OF52 OF51 OF50 DLE5 OF42 OF41 OF40 DLE4</div> </div> </div>                 |   |
| FOR1 Register   |   |
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF112 OF111 OF110 DLE11 OF102 OF101 OF100 DLE10 OF92 OF91 OF90 DLE9 OF82 OF81 OF80 DLE8</div> </div> </div>         |   |
| FOR2 Register   |   |
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF312 OF311 OF310 DLE31 OF142 OF141 OF140 DLE14 OF132 OF131 OF130 DLE13 OF122 OF121 OF120 DLE12</div> </div> </div> |   |
| FOR3 Register   |   |
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF192 OF191 OF190 DLE19 OF182 OF181 OF180 DLE18 OF172 OF171 OF170 DLE17 OF162 OF161 OF160 DLE16</div> </div> </div> |   |
| FOR4 Register   |   |
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF232 OF231 OF230 DLE23 OF222 OF221 OF220 DLE22 OF212 OF211 OF210 DLE21 OF202 OF201 OF200 DLE20</div> </div> </div> |   |
| FOR5 Register   |   |
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF272 OF271 OF270 DLE27 OF262 OF261 OF260 DLE26 OF252 OF251 OF250 DLE25 OF242 OF241 OF240 DLE24</div> </div> </div> |   |
| FOR6 Register   |   |
| <div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> <div> <div>OF312 OF311 OF310 DLE31 OF302 OF301 OF300 DLE30 OF292 OF291 OF290 DLE29 OF282 OF281 OF280 DLE28</div> </div> </div> |   |
| FOR7 Register   |   |
| Name <sup>(1)</sup>   | Description   |
| OFn2, OFn1, OFn0<br>(Offset Bits 2, 1 & 0)  | These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the RX input pin: i.e., to start a new frame. The input frame offset can be selected to +4.5 clock periods from the point where the external frame pulse input signal is applied to the $\overline{FOI}$ input of the device. See Figure 1.  |
| DLEn  | ST-BUS <sup>®</sup> mode:<br>(Data Latch Edge)<br>DLEn = 0, if clock rising edge is at the $\frac{3}{4}$ point of the bit cell.<br>DLEn = 1, if when clock falling edge is at the $\frac{3}{4}$ of the bit cell.<br>GCI mode:<br>DLEn = 0, if clock falling edge is at the $\frac{3}{4}$ point of the bit cell.<br>DLEn = 1, if when clock rising edge is at the $\frac{3}{4}$ of the bit cell. |

**NOTE:**

1. n denotes an input stream number from 0 to 31.

**TABLE 9 — OFFSET BITS (OFn2, OFn1, OFn0, DLEn) & FRAME DELAY BITS (FD11, FD2-0)**

| Input Stream<br>Offset          | Measurement Result from<br>Frame Delay Bits |     |     |     | Corresponding<br>Offset Bits |      |      |      |
|---------------------------------|---|-----|-----|-----|------------------------------|------|------|------|
|                                 | FD11  | FD2 | FD1 | FD0 | OFn2                         | OFn1 | OFn0 | DLEn |
| No clock period shift (Default) | 1   | 0   | 0   | 0   | 0                            | 0    | 0    | 0    |
| + 0.5 clock period shift        | 0   | 0   | 0   | 0   | 0                            | 0    | 0    | 1    |
| + 1.0 clock period shift        | 1   | 0   | 0   | 1   | 0                            | 0    | 1    | 0    |
| + 1.5 clock period shift        | 0   | 0   | 0   | 1   | 0                            | 0    | 1    | 1    |
| + 2.0 clock period shift        | 1   | 0   | 1   | 0   | 0                            | 1    | 0    | 0    |
| + 2.5 clock period shift        | 0   | 0   | 1   | 0   | 0                            | 1    | 0    | 1    |
| + 3.0 clock period shift        | 1   | 0   | 1   | 1   | 0                            | 1    | 1    | 0    |
| + 3.5 clock period shift        | 0   | 0   | 1   | 1   | 0                            | 1    | 1    | 1    |
| + 4.0 clock period shift        | 1   | 1   | 0   | 0   | 1                            | 0    | 0    | 0    |
| + 4.5 clock period shift        | 0   | 1   | 0   | 0   | 1                            | 0    | 0    | 1    |


**Figure 2. Examples for Input Offset Delay Timing**

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## JTAG SUPPORT

The IDT72V70840 JTAG interface conforms to the Boundary-Scan standard IEEE-1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

### TEST ACCESS PORT (TAP)

The Test Access Port (TAP) provides access to the test functions of the IDT72V70840. It consists of three input pins and one output pin.

- Test Clock Input (TCK)

TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remain independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

- Test Mode Select Input (TMS)

The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vcc when it is not driven from an external source.

- Test Data Input (TDI)

Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vcc when it is not driven from an external source.

- Test Data Output (TDO)

Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.

- Test Reset (TRST)

Reset the JTAG scan structure. This pin is internally pulled to Vcc.

## INSTRUCTION REGISTER

In accordance with the IEEE-1149.1 standard, the IDT72V70840 uses public instructions. The IDT72V70840 JTAG Interface contains a two-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning. See Table below for Instruction decoding.

| Value | Instruction    | Function                      |
|-------|----------------|-------------------------------|
| 11    | Bypass         | Select Bypass Register        |
| 10    | Sample/Preload | Select Boundary Scan Register |
| 01    | Sample/Preload | Select Boundary Scan Register |
| 00    | EXTEST         | Select Boundary Scan Register |

### *JTAG Instruction Register Decoding*

## TEST DATA REGISTER

As specified in IEEE-1149.1, the IDT72V70840 JTAG Interface contains two test data registers:

- The Boundary-Scan register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the IDT72V70840 core logic.

- The Bypass Register

The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO. The IDT72V70840 boundary scan register bits are shown in Table 10. Bit 0 is the first bit clocked out. All three-state enable bits are active high.

**TABLE 10 — BOUNDARY SCAN REGISTER BITS**

| Device Pin | Boundary Scan Bit 0 to bit 167 |                  |                 |
|------------|--------------------------------|------------------|-----------------|
|            | Three-State Control            | Output Scan Cell | Input Scan Cell |
| ODE        |                                |                  | 0               |
| RESET      |                                |                  | 1               |
| CLK        |                                |                  | 2               |
| F0i        |                                |                  | 3               |
| FE/HCLK    |                                |                  | 4               |
| WFPS       |                                |                  | 5               |
| DS         |                                |                  | 6               |
| CS         |                                |                  | 7               |
| R/W        |                                |                  | 8               |
| A0         |                                |                  | 9               |
| A1         |                                |                  | 10              |
| A2         |                                |                  | 11              |
| A3         |                                |                  | 12              |
| A4         |                                |                  | 13              |
| A5         |                                |                  | 14              |
| A6         |                                |                  | 15              |
| A7         |                                |                  | 16              |
| A8         |                                |                  | 17              |
| A9         |                                |                  | 18              |
| A10        |                                |                  | 19              |
| A11        |                                |                  | 20              |
| A12        |                                |                  | 21              |
| A13        |                                |                  | 22              |
| DTA        |                                | 23               |                 |
| D15        | 24                             | 25               | 26              |
| D14        | 27                             | 28               | 29              |
| D13        | 30                             | 31               | 32              |
| D12        | 33                             | 34               | 35              |
| D11        | 36                             | 37               | 38              |
| D10        | 39                             | 40               | 41              |
| D9         | 42                             | 43               | 44              |
| D8         | 45                             | 46               | 47              |
| D7         | 48                             | 49               | 50              |
| D6         | 51                             | 52               | 53              |
| D5         | 54                             | 55               | 56              |
| D4         | 57                             | 58               | 59              |
| D3         | 60                             | 61               | 62              |
| D2         | 63                             | 64               | 65              |
| D1         | 66                             | 67               | 68              |
| D0         | 69                             | 70               | 71              |
| TX31       | 72                             | 73               |                 |
| TX30       | 74                             | 75               |                 |
| TX29       | 76                             | 77               |                 |
| TX28       | 78                             | 79               |                 |
| TX27       | 80                             | 81               |                 |
| TX26       | 82                             | 83               |                 |
| TX25       | 84                             | 85               |                 |
| TX24       | 86                             | 87               |                 |
| RX31       |                                |                  | 88              |
| RX30       |                                |                  | 89              |
| RX29       |                                |                  | 90              |
| RX28       |                                |                  | 91              |

| Device Pin | Boundary Scan Bit 0 to bit 167 |                  |                 |
|------------|--------------------------------|------------------|-----------------|
|            | Three-State Control            | Output Scan Cell | Input Scan Cell |
| RX27       |                                |                  | 92              |
| RX26       |                                |                  | 93              |
| RX25       |                                |                  | 94              |
| RX24       |                                |                  | 95              |
| TX23       | 96                             | 97               |                 |
| TX22       | 98                             | 99               |                 |
| TX21       | 100                            | 101              |                 |
| TX20       | 102                            | 103              |                 |
| TX19       | 104                            | 105              |                 |
| TX18       | 106                            | 107              |                 |
| TX17       | 108                            | 109              |                 |
| TX16       | 110                            | 111              |                 |
| RX23       |                                |                  | 112             |
| RX22       |                                |                  | 113             |
| RX21       |                                |                  | 114             |
| RX20       |                                |                  | 115             |
| RX19       |                                |                  | 116             |
| RX18       |                                |                  | 117             |
| RX17       |                                |                  | 118             |
| RX16       |                                |                  | 119             |
| TX15       | 120                            | 121              |                 |
| TX14       | 122                            | 123              |                 |
| TX13       | 124                            | 125              |                 |
| TX12       | 126                            | 127              |                 |
| TX11       | 128                            | 129              |                 |
| TX10       | 130                            | 131              |                 |
| TX9        | 132                            | 133              |                 |
| TX8        | 134                            | 135              |                 |
| RX15       |                                |                  | 136             |
| RX14       |                                |                  | 137             |
| RX13       |                                |                  | 138             |
| RX12       |                                |                  | 139             |
| RX11       |                                |                  | 140             |
| RX10       |                                |                  | 141             |
| RX9        |                                |                  | 142             |
| RX8        |                                |                  | 143             |
| TX7        | 144                            | 145              |                 |
| TX6        | 146                            | 147              |                 |
| TX5        | 148                            | 149              |                 |
| TX4        | 150                            | 151              |                 |
| TX3        | 152                            | 153              |                 |
| TX2        | 154                            | 155              |                 |
| TX1        | 156                            | 157              |                 |
| TX0        | 158                            | 159              |                 |
| RX7        |                                |                  | 160             |
| RX6        |                                |                  | 161             |
| RX5        |                                |                  | 162             |
| RX4        |                                |                  | 163             |
| RX3        |                                |                  | 164             |
| RX2        |                                |                  | 165             |
| RX1        |                                |                  | 166             |
| RX0        |                                |                  | 167             |

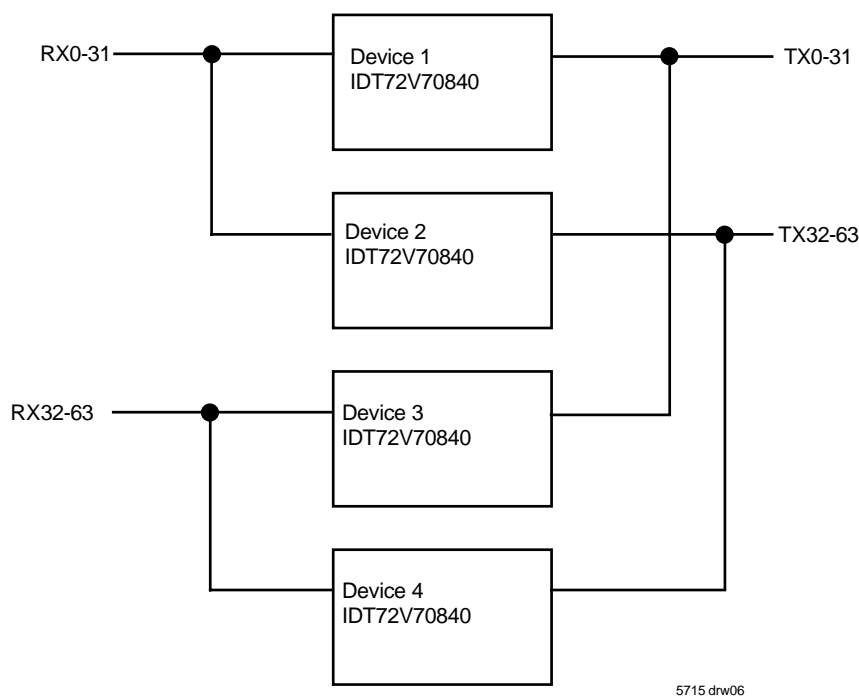
## APPLICATIONS

### CREATING LARGE SWITCH MATRICES

To create a switch matrix with twice the capacity of a given TSIS device, four devices must be used. In the example below, four IDT72V70840, 4096 x 4096 channel capacity devices are used to create an 8192 x 8192 channel switch matrix.

As can be seen, Device #1 and Device #2 will receive the same incoming RX0-31 data and thus have the same contents in Data Memory. On the output

side, however Device #1 is used to switch data out on to TX0-31 where as Device #2 is used to switch out on TX32-63. Likewise Device #3 and Device #4 are used in the same way as Device #1 and Device #2 but switch RX32-63, to TX0-31 and TX32-63. With this configuration all possible combinations of input and output streams are possible. In short, Device #1 is used to switch RX0-31 to TX0-31, Device #2 to switch RX0-31 to TX32-63, Device #3 to switch RX32-63 to TX0-31, and Device #4 to switch RX32-63 to TX32-63.



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Figure 3. Creating Larger Switch Matrices

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol          | Parameter                  | Min.     | Max. | Unit |
|-----------------|----------------------------|----------|------|------|
| V <sub>CC</sub> | Supply Voltage             | 3.0      | 3.6  | V    |
| V <sub>I</sub>  | Voltage on Digital Inputs  | GND -0.3 | 5.3  | V    |
| I <sub>O</sub>  | Current at Digital Outputs | -50      | 50   | mA   |
| T <sub>S</sub>  | Storage Temperature        | -55      | +125 | °C   |
| P <sub>D</sub>  | Package Power Dissipation  | —        | 2    | W    |

### NOTE:

- Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

| Symbol          | Parameter                        | Min. | Typ. | Max. | Unit |
|-----------------|----------------------------------|------|------|------|------|
| V <sub>CC</sub> | Positive Supply                  | 3.0  | 3.3  | 3.6  | V    |
| V <sub>IH</sub> | Input HIGH Voltage               | 2.0  | —    | 5.3  | V    |
| V <sub>IL</sub> | Input LOW Voltage                | —    | —    | 0.8  | V    |
| TOP             | Operating Temperature Commercial | -40  | 25   | +85  | °C   |

### NOTE:

- Voltages are with respect to Ground unless otherwise stated.

## DC ELECTRICAL CHARACTERISTICS

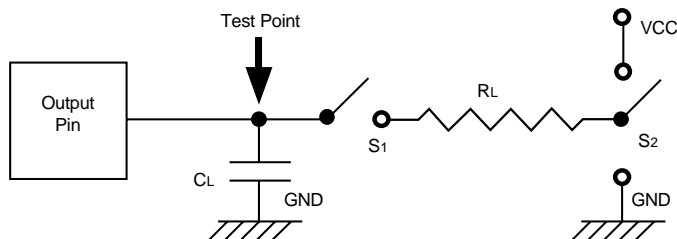
| Symbol                           | Parameter   | Min. | Typ.           | Max.           | Units          |
|----------------------------------|---|------|----------------|----------------|----------------|
| I <sub>CC</sub> <sup>(2)</sup>   | Supply Current @ 2.048 Mb/s<br>@ 4.096 Mb/s<br>@ 8.192 Mb/s | -    | 15<br>25<br>47 | 20<br>35<br>70 | mA<br>mA<br>mA |
| I <sub>IL</sub> <sup>(3,4)</sup> | Input Leakage (input pins)                                  | -    | -              | 50             | μA             |
| I <sub>OZ</sub> <sup>(3,4)</sup> | High-impedance Leakage                                      | -    | -              | 50             | μA             |
| V <sub>OH</sub> <sup>(5)</sup>   | Output HIGH Voltage   | 2.4  | -              | -              | V              |
| V <sub>OL</sub> <sup>(6)</sup>   | Output LOW Voltage  | -    | -              | 0.4            | V              |

### NOTES:

- Voltages are with respect to ground (GND) unless otherwise stated.
- Outputs unloaded.
- 0 ≤ V ≤ V<sub>CC</sub>.
- Maximum leakage on pins (output or I/O pins in high-impedance state) is over an applied voltage (V).
- I<sub>OH</sub> = 10 mA.
- I<sub>OL</sub> = 10 mA.

## AC ELECTRICAL CHARACTERISTICS - TIMING PARAMETER MEASUREMENT VOLTAGE LEVELS

| Symbol          | Rating                               | Level | Unit |
|-----------------|--------------------------------------|-------|------|
| V <sub>TT</sub> | TTL Threshold                        | 1.5   | V    |
| V <sub>HM</sub> | TTL Rise/Fall Threshold Voltage HIGH | 2.0   | V    |
| V <sub>LM</sub> | TTL Rise/Fall Threshold Voltage LOW  | 0.8   | V    |



S1 is open circuit except when testing output levels or high impedance states.

S2 is switched to VCC or GND when testing output levels or high impedance states.

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Figure 4. Output Load

## AC ELECTRICAL CHARACTERISTICS - FRAME PULSE AND CLK

| Symbol                            | Parameter  | Min. | Typ. | Max. | Units |
|-----------------------------------|--|------|------|------|-------|
| t <sub>FPW</sub> <sup>(1)</sup>   | Frame Pulse Width (ST-BUS®, GCI)                           |      |      |      |       |
|                                   | Bit rate = 2.048 Mb/s                                      | 26   | —    | 295  | ns    |
|                                   | Bit rate = 4.096 Mb/s                                      | 26   | —    | 145  | ns    |
|                                   | Bit rate = 8.192 Mb/s                                      | 26   | —    | 80   | ns    |
| t <sub>FPS</sub> <sup>(1)</sup>   | Frame Pulse Setup time before CLK falling (ST-BUS® or GCI) | 5    | —    | —    | ns    |
| t <sub>FPH</sub> <sup>(1)</sup>   | Frame Pulse Hold Time from CLK falling (ST-BUS® or GCI)    | 10   | —    | —    | ns    |
| t <sub>CP</sub> <sup>(1)</sup>    | CLK Period   |      |      |      |       |
|                                   | Bit rate = 2.048 Mb/s                                      | 190  | —    | 300  | ns    |
|                                   | Bit rate = 4.096 Mb/s                                      | 110  | —    | 150  | ns    |
|                                   | Bit rate = 8.192 Mb/s                                      | 58   | —    | 70   | ns    |
| t <sub>CH</sub> <sup>(1)</sup>    | CLK Pulse Width HIGH                                       |      |      |      |       |
|                                   | Bit rate = 2.048 Mb/s                                      | 85   | —    | 150  | ns    |
|                                   | Bit rate = 4.096 Mb/s                                      | 50   | —    | 75   | ns    |
|                                   | Bit rate = 8.192 Mb/s                                      | 20   | —    | 40   | ns    |
| t <sub>CL</sub> <sup>(1)</sup>    | CLK Pulse Width LOW  |      |      |      |       |
|                                   | Bit rate = 2.048 Mb/s                                      | 85   | —    | 150  | ns    |
|                                   | Bit rate = 4.096 Mb/s                                      | 50   | —    | 75   | ns    |
|                                   | Bit rate = 8.192 Mb/s                                      | 20   | —    | 40   | ns    |
| t <sub>r</sub> , t <sub>f</sub>   | Clock Rise/Fall Time                                       | —    | —    | 10   | ns    |
| t <sub>HFPW</sub> <sup>(2)</sup>  | Wide Frame Pulse Width<br>Bit rate = 8.192 Mb/s            | 195  | —    | 295  | ns    |
| t <sub>HFPS</sub> <sup>(2)</sup>  | Frame Pulse Setup Time before HCLK falling                 | 5    | —    | 150  | ns    |
| t <sub>HFPH</sub> <sup>(2)</sup>  | Frame Pulse Hold Time from HCLK falling                    | 10   | —    | 150  | ns    |
| t <sub>HCP</sub> <sup>(2)</sup>   | HCLK (4.096 MHz) Period<br>Bit rate = 8.192 Mb/s           | 190  | —    | 300  | ns    |
| t <sub>HCH</sub> <sup>(2)</sup>   | HCLK (4.096 MHz) Pulse Width HIGH<br>Bit rate = 8.192 Mb/s | 85   | —    | 150  | ns    |
| t <sub>HCL</sub> <sup>(2)</sup>   | HCLK (4.096 MHz) Pulse Width LOW<br>Bit rate = 8.192 Mb/s  | 85   | —    | 150  | ns    |
| t <sub>Hr</sub> , t <sub>Hf</sub> | HCLK Rise/Fall Time  | —    | —    | 10   | ns    |
| t <sub>DIF</sub> <sup>(3)</sup>   | Delay between falling edge of HCLK and falling edge of CLK | -10  | —    | 10   | ns    |

### NOTES:

1. WFPS Pin = 0.
2. WFPS Pin = 1
3. WFPS Pin = 0 or 1.

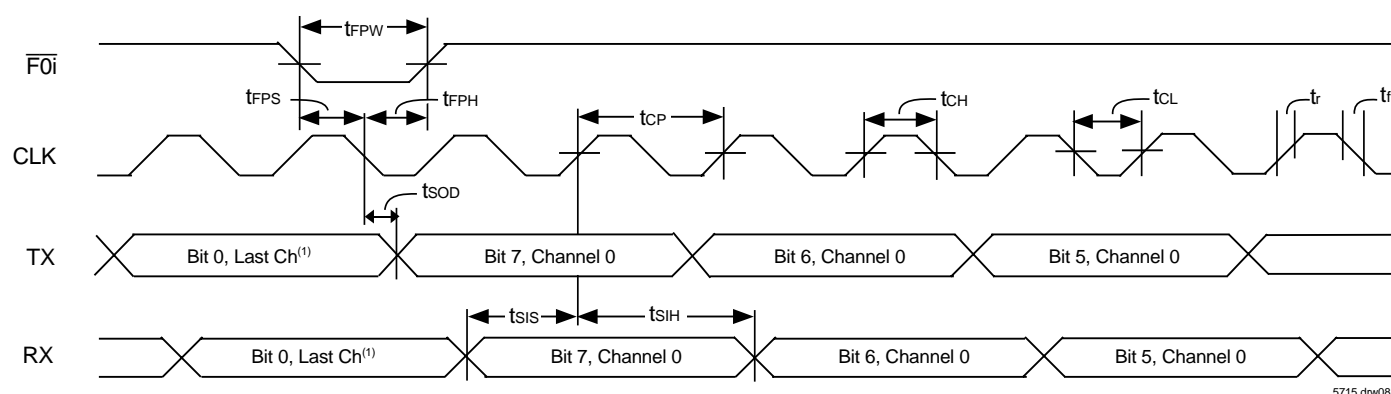


# AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup> — SERIAL STREAM (ST-BUS<sup>®</sup> and GCI)

| Symbol    | Parameter  | Min. | Typ. | Max. | Units |
|-----------|--|------|------|------|-------|
| $t_{SIS}$ | RX Setup Time                                    | 5    | —    | —    | ns    |
| $t_{SIH}$ | RX Hold Time                                     | 10   | —    | —    | ns    |
| $t_{SOD}$ | TX Delay – Active to Active<br>@ 2.048 Mb/s      | —    | —    | 30   | ns    |
|           | @ 4.096 Mb/s                                     | —    | —    | 30   | ns    |
|           | @ 8.192 Mb/s                                     | —    | —    | 30   | ns    |
| $t_{DZ}$  | TX Delay – Active to High-Z<br>@ 2.048 Mb/s      | —    | —    | 30   | ns    |
|           | @ 4.096 Mb/s                                     | —    | —    | 30   | ns    |
|           | @ 8.192 Mb/s                                     | —    | —    | 30   | ns    |
| $t_{ZD}$  | TX Delay – High-Z to Active<br>@ 2.048 Mb/s      | —    | —    | 30   | ns    |
|           | @ 4.096 Mb/s                                     | —    | —    | 30   | ns    |
|           | @ 8.192 Mb/s                                     | —    | —    | 30   | ns    |
| $t_{ODE}$ | Output Driver Enable (ODE) Delay<br>@ 2.048 Mb/s | —    | —    | 30   | ns    |
|           | @ 4.096 Mb/s                                     | —    | —    | 30   | ns    |
|           | @ 8.192 Mb/s                                     | —    | —    | 30   | ns    |

## NOTE:

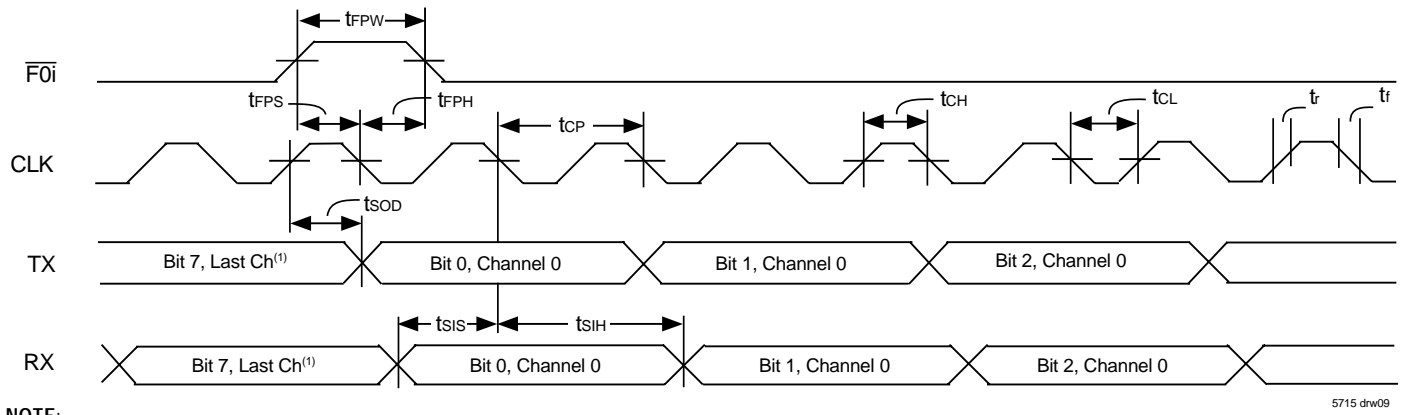
1. High Impedance is measured by pulling to the appropriate rail with  $R_L$  (1K), with timing corrected to cancel time taken to discharge  $C_L$  (150 pF).



## NOTE:

- @ 2.048 Mb/s mode, last channel = ch 31,  
@ 4.096 Mb/s mode, last channel = ch 63,  
@ 8.192 Mb/s mode, last channel = ch 127.

Figure 5. ST-BUS<sup>®</sup> Timing



NOTE:

1. @ 2.048 Mb/s mode, last channel = ch 31,  
@ 4.096 Mb/s mode, last channel = ch 63,  
@ 8.192 Mb/s mode, last channel = ch 127.

Figure 6. GCI Timing

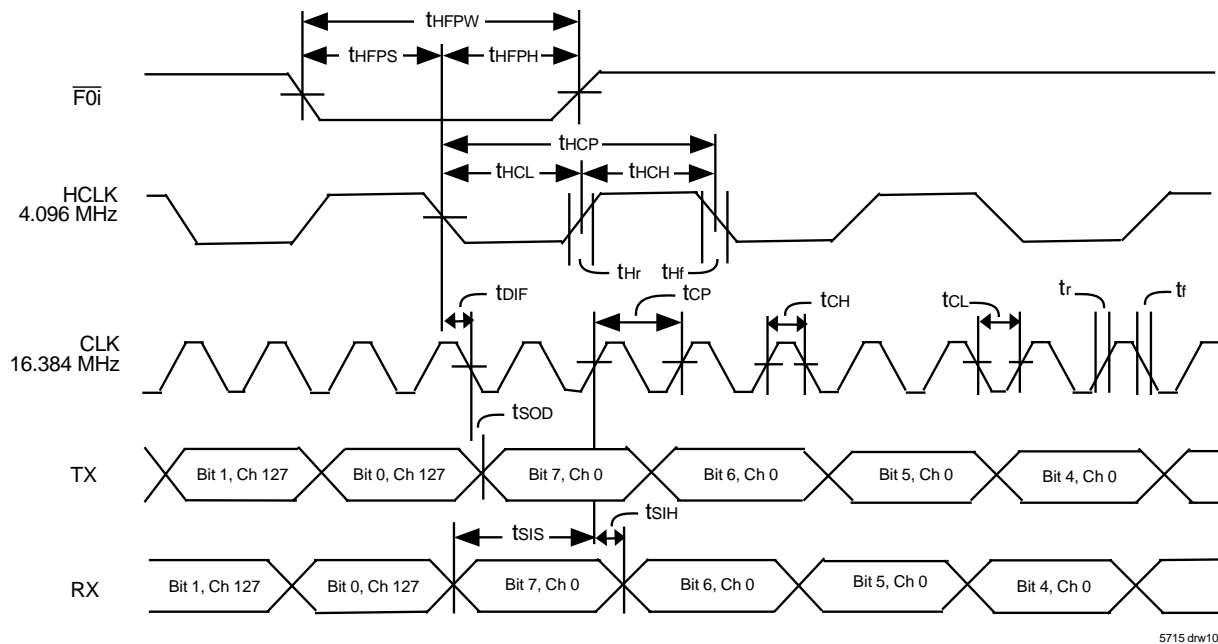


Figure 7. WFP Bus Timing (@ 8.192 Mb/s, when pin WFPS is HIGH)

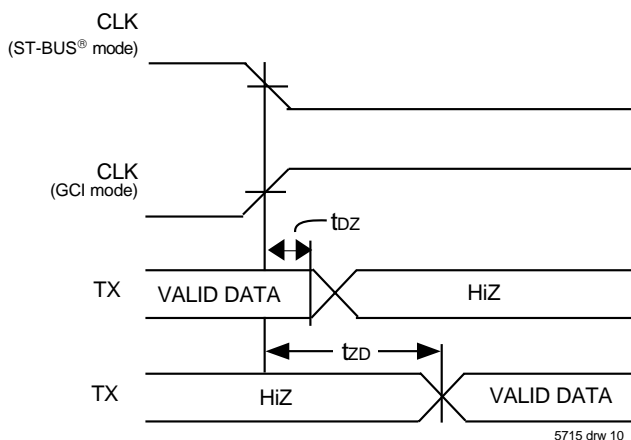


Figure 8. Serial Output and External Control

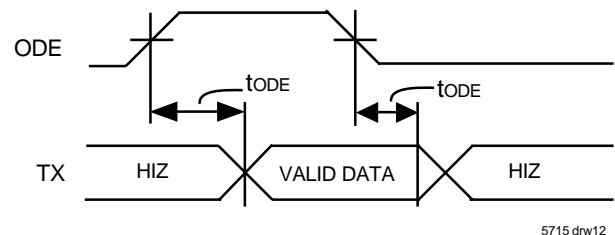


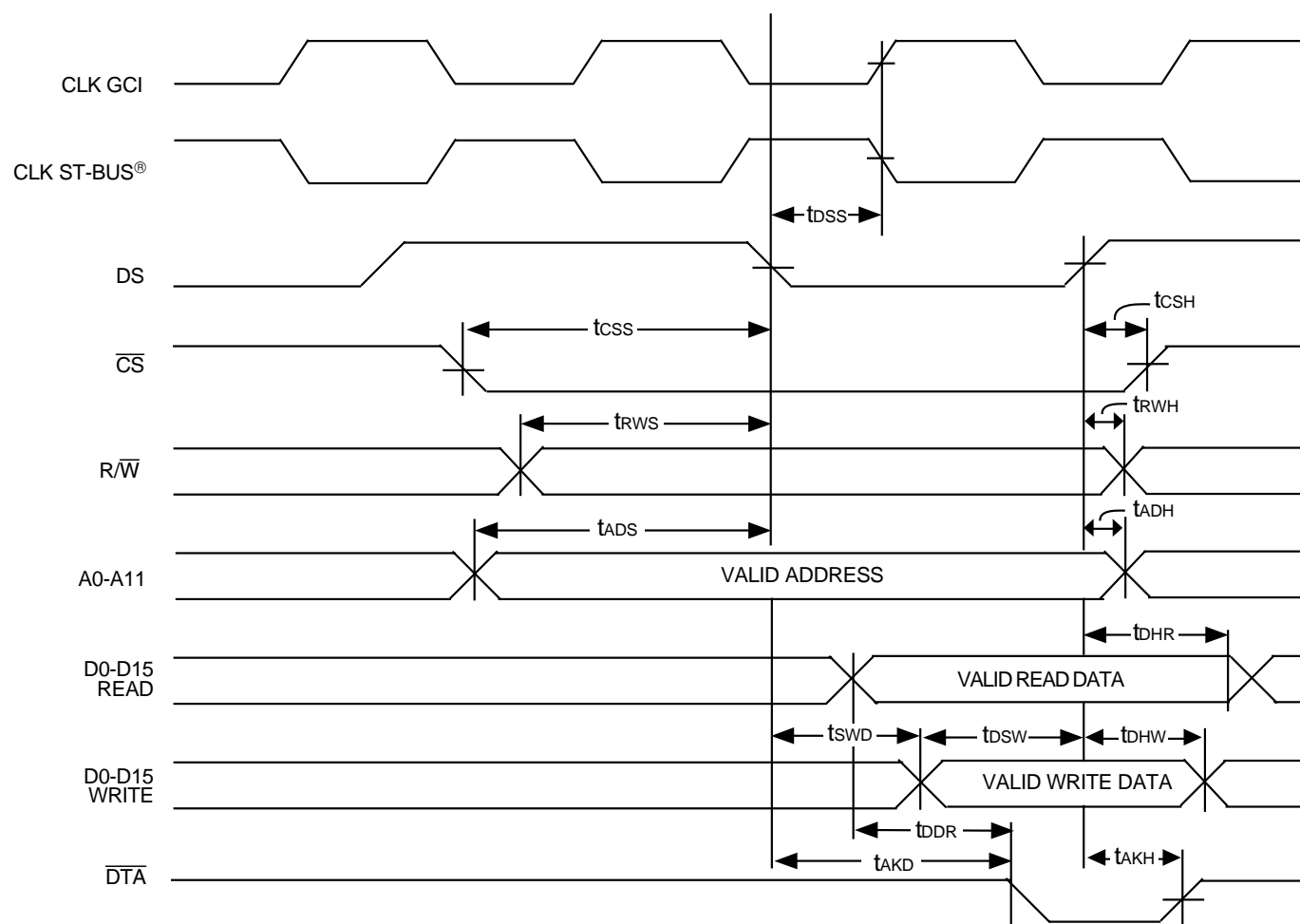
Figure 9. Output Driver Enable (ODE)

## AC ELECTRICAL CHARACTERISTICS - MICROPROCESSOR INTERFACE TIMING

| Symbol                              | Parameter   | Min. | Typ. | Max. | Units |
|-------------------------------------|---|------|------|------|-------|
| t <sub>CS</sub>                     | CS Setup from DS falling  | 0    | —    | —    | ns    |
| t <sub>RWS</sub>                    | R/W Setup from DS falling   | 3    | —    | —    | ns    |
| t <sub>ADS</sub>                    | Address Setup from DS falling   | 2    | —    | —    | ns    |
| t <sub>CSH</sub>                    | CS Hold after DS rising   | 0    | —    | —    | ns    |
| t <sub>RWH</sub>                    | R/W Hold after DS Rising  | 3    | —    | —    | ns    |
| t <sub>ADH</sub>                    | Address Hold after DS Rising  | 2    | —    | —    | ns    |
| t <sub>DDR</sub> <sup>(1)</sup>     | Data Setup from $\overline{DTA}$ LOW on Read  | 2    | —    | —    | ns    |
| t <sub>DHR</sub> <sup>(1,2,3)</sup> | Data Hold on Read   | 10   | 15   | 25   | ns    |
| t <sub>DSW</sub>                    | Data Setup on Write (Fast Write)  | 10   | —    | —    | ns    |
| t <sub>SWD</sub>                    | Valid Data Delay on Write (Slow Write)  | -    | —    | 0    | ns    |
| t <sub>DHW</sub>                    | Data Hold on Write  | 5    | —    | —    | ns    |
| t <sub>AKD</sub> <sup>(1)</sup>     | Acknowledgment Delay:<br>Reading/Writing Registers<br>Reading/Writing Memory @ 2.048 Mb/s<br>@ 4.096 Mb/s<br>@ 8.192 Mb/s |      |      | 30   | ns    |
|                                     |   |      |      | 345  | ns    |
|                                     |   |      |      | 200  | ns    |
|                                     |   |      |      | 120  | ns    |
| t <sub>AKH</sub> <sup>(1,2,3)</sup> | Acknowledgment Hold Time  | —    | —    | 20   | ns    |
| t <sub>DSS</sub> <sup>(4)</sup>     | Data Strobe Setup Time  | 2    | —    | —    | ns    |

### NOTES:

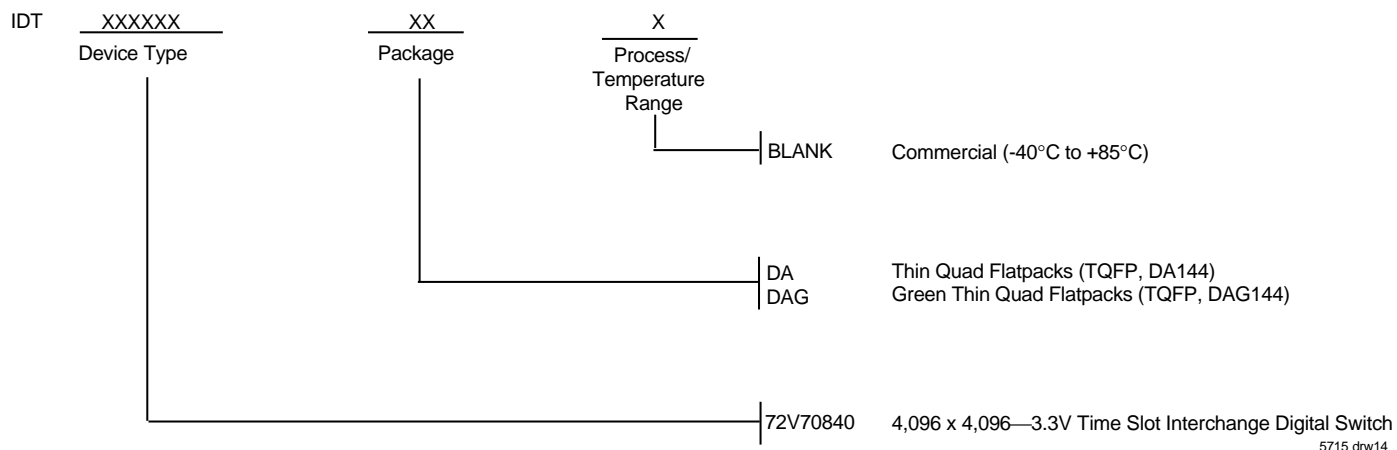
1. C<sub>L</sub> = 150pF
2. R<sub>L</sub> = 1K
3. High Impedance is measured by pulling to the appropriate rail with R<sub>L</sub>, with timing corrected to cancel time taken to discharge C<sub>L</sub>.
4. To achieve one clock cycle fast memory access, this setup time, t<sub>DSS</sub> should be met. Otherwise, worst case memory access operation is determined by t<sub>AKD</sub>.



5715 drw13

Figure 10. Motorola Non-Multiplexed Bus Timing

## ORDERING INFORMATION



## DATASHEET DOCUMENT HISTORY

|            |   |
|------------|---|
| 5/05/2000  | pg. 1                                       |
| 6/08/2000  | pgs. 1, 2, 3 and 19.                        |
| 8/30/2000  | pgs. 2, 4, 6, 9, 11, 13, 14, 16, 17 and 19. |
| 01/24/2001 | pg. 14                                      |
| 10/22/2001 | pg. 1.                                      |
| 1/04/2002  | pgs. 1 and 15.                              |
| 12/14/2006 | pgs. 2 and 20.                              |
| 10/06/2008 | pg. 3.                                      |



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