

### Description

The AP2162A and AP2172A are dual channel current-limited integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB standards and available with both polarities of Enable input.

The devices have fast short-circuit response time for improved overall system robustness, and have integrated output discharge function to ensure completely controlled discharging of the output voltage capacitor. They provide a complete protection solution for application subject to heavy capacitive loads and the prospect of short circuit, and offer reverse current blocking, over-current, over-temperature and short-circuit protection, as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

All devices are available in SO-8, MSOP-8-EP and DFN3030E-8 packages.

### Features

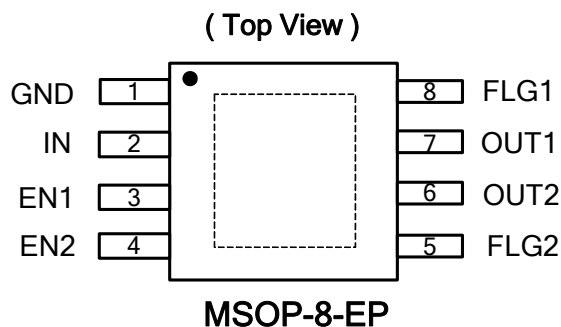
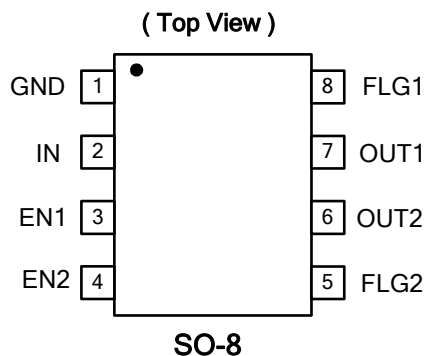
- Dual channel current-limited power switch with output discharge
- Fast short-circuit response time: 2 $\mu$ s
- 1.4A accurate current limiting
- Reverse Current Blocking
- 85m $\Omega$  on-resistance
- Input voltage range: 2.7V – 5.5V
- Built-in soft-start with 0.6ms typical rise time
- Short circuit and thermal protection
- Fault report (FLG) with blanking time (7ms typ)
- ESD protection: 2KV HBM, 300V MM
- Active high (AP2172A) or active low (AP2162A) enable
- Ambient temperature range: -40°C to 85°C
- SO-8, MSOP-8-EP and DFN3030E-8 (Exposed Pad): Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

### Applications

- LCD TVs & Monitors
- Set-Top-Boxes, Residential Gateways
- Laptops, Desktops, Servers,
- Printers, Docking Stations, HUBs

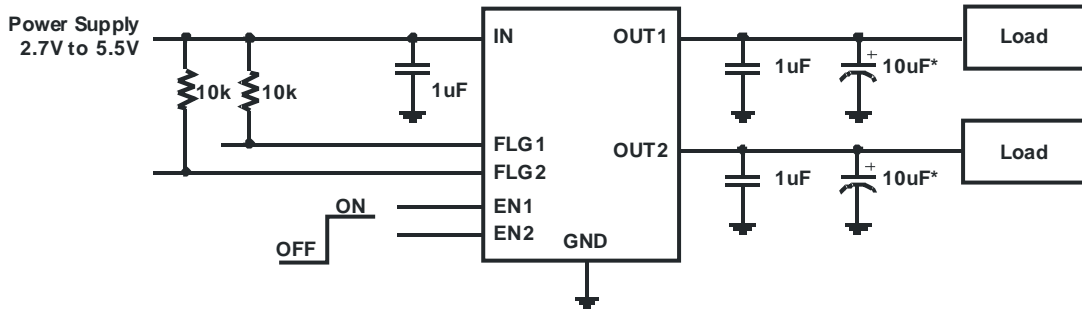
Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html).

### Pin Assignments



### Typical Application Circuit

AP2172 A Enable Active High



Note: \* USB 2.0 requires 120 $\mu$ F per hub

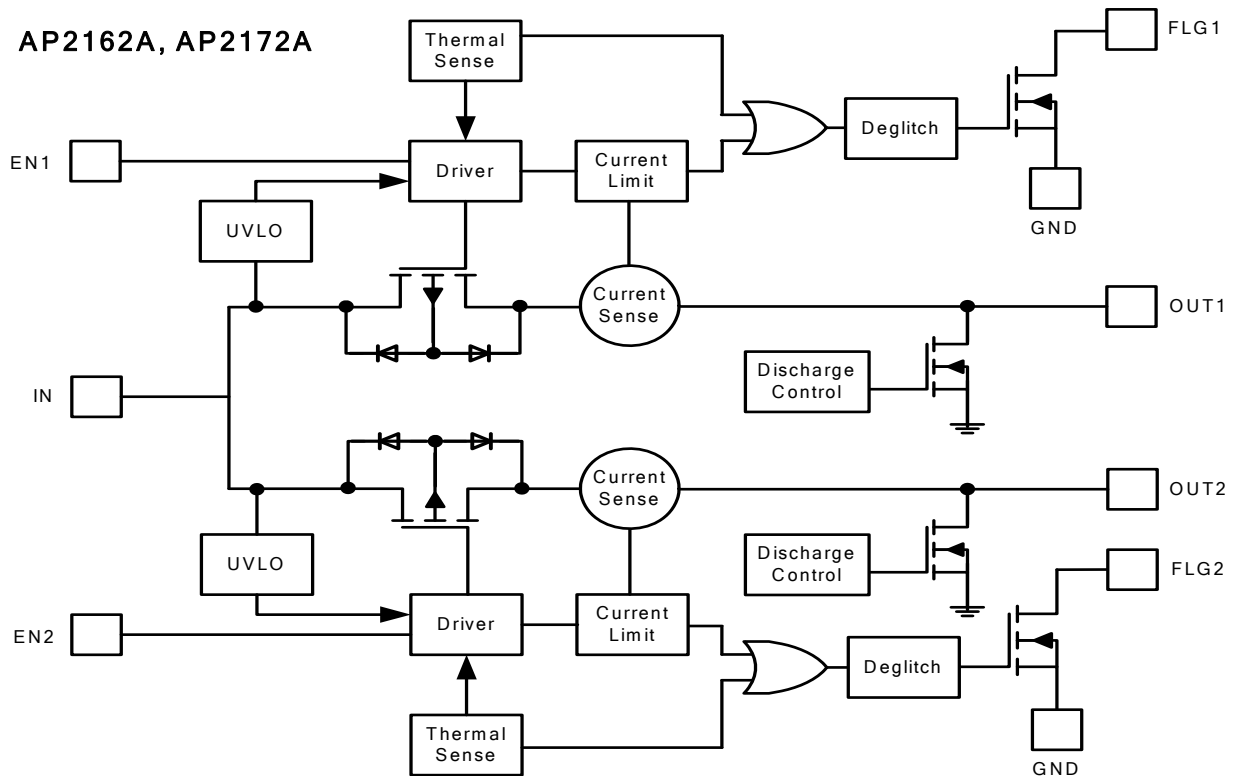
### Available Options

Part Number	Channel	Enable pin (EN)	Current limit (typical)	Recommended maximum continuous load current
AP2162A	2	Active Low	1.4A	1.0A
AP2172A	2	Active High	1.4A	1.0A

### Pin Descriptions

Pin Name	Pin Number	Descriptions
GND	1	Ground
IN	2	Voltage input pin
EN1	3	Switch 1 enable input, active low (AP2162A) or active high (AP2172A)
EN2	4	Switch 2 enable input, active low (AP2162A) or active high (AP2172A)
FLG2	5	Switch 2 over-current and over-temperature fault report; open-drain flag is active low when triggered
OUT2	6	Switch 2 voltage output pin
OUT1	7	Switch 1 voltage output pin
FLG1	8	Switch 1 over-current and over-temperature fault report; open-drain flag is active low when triggered
Exposed Pad	-	Internally connected to GND; recommend connecting to the GND externally for improved power dissipation

### Functional Block Diagram



### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	300	V
$V_{IN}$	Input Voltage	6.5	V
$V_{OUT}$	Output Voltage	$V_{IN} + 0.3$	V
$V_{EN}, V_{FLG}$	Enable Voltage	6.5	V
$I_{load}$	Maximum Continuous Load Current	Internal Limited	A
$T_{Jmax}$	Maximum Junction Temperature	150	°C
$T_{ST}$	Storage Temperature Range (Note 2)	-65 to 150	°C

Notes: 2. UL Recognized Rating from -30°C to 70°C (Diodes qualified  $T_{ST}$  from -65°C to 150°C)

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{IN}$	Input voltage	2.7	5.5	V
$I_{OUT}$	Output Current	0	1.0	A
$T_A$	Operating Ambient Temperature	-40	85	°C

### Electrical Characteristics (T<sub>A</sub> = 25°C, V<sub>IN</sub> = +5.0V, unless otherwise stated)

Symbol	Parameter	Test Conditions (Note 3)	Min	Typ.	Max	Unit	
V <sub>UVLO</sub>	Input UVLO		1.6	2.0	2.4	V	
I <sub>SHDN</sub>	Input Shutdown Current	Disabled, I <sub>OUT</sub> = 0		0.1	1	μA	
I <sub>Q</sub>	Input Quiescent Current, Dual	Enabled, I <sub>OUT</sub> = 0		115	180	μA	
I <sub>LEAK</sub>	Input Leakage Current	Disabled, OUT grounded			1	μA	
I <sub>REV</sub>	Reverse Leakage Current	Disabled, V <sub>IN</sub> = 0V, V <sub>OUT</sub> = 5V, I <sub>REV</sub> at V <sub>IN</sub>		0.01	0.1	μA	
R <sub>DS(ON)</sub>	Switch on-resistance	V <sub>IN</sub> = 5V, I <sub>OUT</sub> = 1A, T <sub>A</sub> = 25°C		90	110	mΩ	
			SO-8				
			MSOP-8-EP, DFN3030E-8		85 105		
		V <sub>IN</sub> = 5V, I <sub>OUT</sub> = 1A, -40°C ≤ T <sub>A</sub> ≤ 85°C			135		
		V <sub>IN</sub> = 3.3V, I <sub>OUT</sub> = 1A, T <sub>A</sub> = 25°C		110	130		
		MSOP-8-EP, DFN3030E-8		105	125		
		V <sub>IN</sub> = 3.3V, I <sub>OUT</sub> = 1A, -40°C ≤ T <sub>A</sub> ≤ 85°C			170		
I <sub>LIMIT</sub>	Over-Load Current Limit	V <sub>IN</sub> = 5V, V <sub>OUT</sub> = 4V, C <sub>L</sub> =10μF	-40°C ≤ T <sub>A</sub> ≤ 85°C	1.1	1.4	1.7	A
I <sub>LIMIT_G</sub>	Ganged Over-Load Current Limit	V <sub>IN</sub> = 5V, V <sub>OUT</sub> = 4.8V, OUT1 & OUT2 tied together, C <sub>L</sub> =10μF	-40°C ≤ T <sub>A</sub> ≤ 85°C	2.2	2.8	3.4	A
I <sub>Trig</sub>	Current limiting trigger threshold	Output Current Slew rate (<100A/s), C <sub>L</sub> =10μF		1.8			A
I <sub>Trig_G</sub>	Ganged current limiting trigger threshold	OUT1 & OUT2 tied together, Output Current Slew rate (<100A/s), C <sub>L</sub> =10μF		3.6			A
I <sub>OS</sub>	Short-circuit current per channel	OUTx connected to ground, device enabled into short circuit, C <sub>L</sub> =10μF		1.4			A
I <sub>OS_G</sub>	Ganged short-circuit current	OUT1 & OUT2 connected to ground, device enabled into short-circuit, C <sub>L</sub> =10μF		2.2	2.8	3.4	A
T <sub>SHORT</sub>	Short-circuit response time	V <sub>OUT</sub> = 0V to I <sub>OUT</sub> = I <sub>LIMIT</sub> (output shorted to ground)		2			μs
V <sub>IL</sub>	EN Input Logic Low Voltage	V <sub>IN</sub> = 2.7V to 5.5V			0.8		V
V <sub>IH</sub>	EN Input Logic High Voltage	V <sub>IN</sub> = 2.7V to 5.5V	2				V
I <sub>SINK</sub>	EN Input leakage	V <sub>EN</sub> = 0V to 5.5V			1		μA
I <sub>LEAK-O</sub>	Output leakage current	Disabled, V <sub>OUT</sub> = 0V		0.5	1		μA
T <sub>R</sub>	Output turn-on rise time	C <sub>L</sub> = 1μF, R <sub>load</sub> = 5Ω		0.6	1.5		ms
T <sub>F</sub>	Output turn-off fall time	C <sub>L</sub> = 1μF, R <sub>load</sub> = 5Ω		0.05	0.3		ms
T <sub>D(ON)</sub>	Output turn-on delay time	C <sub>L</sub> = 100μF, R <sub>load</sub> = 5Ω		0.2	0.5		ms
T <sub>D(OFF)</sub>	Output turn-off delay time	C <sub>L</sub> = 100μF, R <sub>load</sub> = 5Ω		0.1	0.3		ms
R <sub>FLG</sub>	FLG output FET on-resistance	I <sub>FLG</sub> = 10mA		20	40		Ω
I <sub>FOH</sub>	FLG off current	V <sub>FLG</sub> = 5V		0.01	1		μA
T <sub>Blank</sub>	FLG blanking time	C <sub>L</sub> =10μF	4	7	15		ms
R <sub>DIS</sub>	Discharge resistance (Note 4)	V <sub>IN</sub> = 5V, disabled, I <sub>OUT</sub> = 1mA		100			Ω
T <sub>SHDN</sub>	Thermal shutdown threshold	Enabled, R <sub>load</sub> =1kΩ		140			°C
T <sub>HYS</sub>	Thermal shutdown hysteresis			25			°C
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient	SO-8 (Note 5)		115			°C/W
		MSOP-8-EP (Note 6)		75			
		DFN3030E-8 (Note 6)		60			

Notes: 3. Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

4. The discharge function is active when the device is disabled (when enable is de-asserted or during power-up power-down when V<sub>IN</sub> < V<sub>UVLO</sub>). The discharge function offers a resistive discharge path for the external storage capacitor for limited time.

5. Test condition for SO-8: Device mounted on FR-4 substrate PCB with minimum recommended pad layout.

6. Test condition for MSOP-8-EP and DFN3030E-8: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Typical Performance Characteristics**

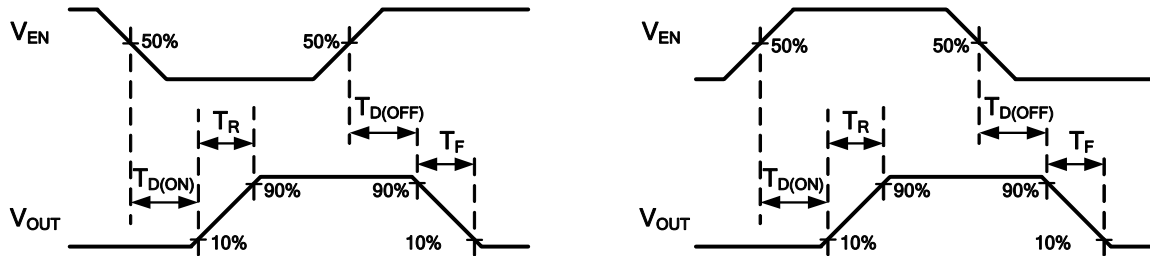


Figure 1. Voltage Waveforms: AP2162A (left), AP2172A (right)

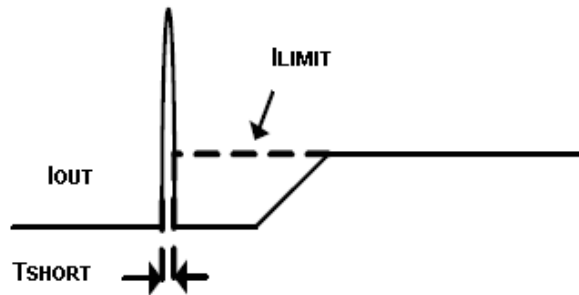
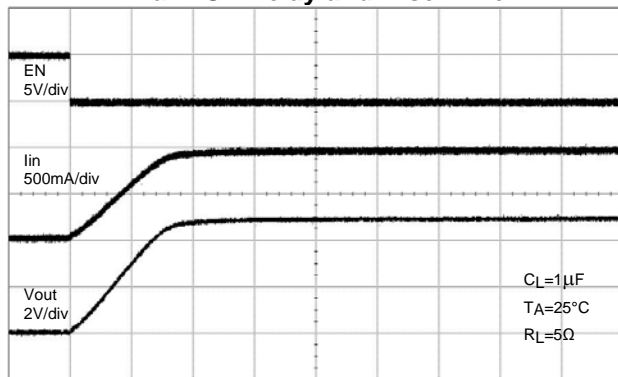


Figure 2. Response Time to Short Circuit Waveform

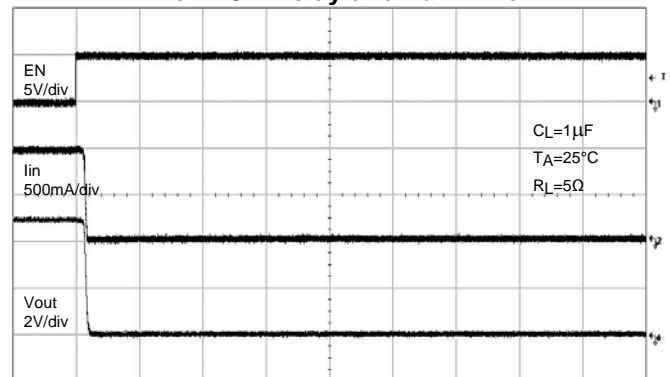
All Enable Plots are for AP2162A Active Low

**Turn-On Delay and Rise Time**



500us/div

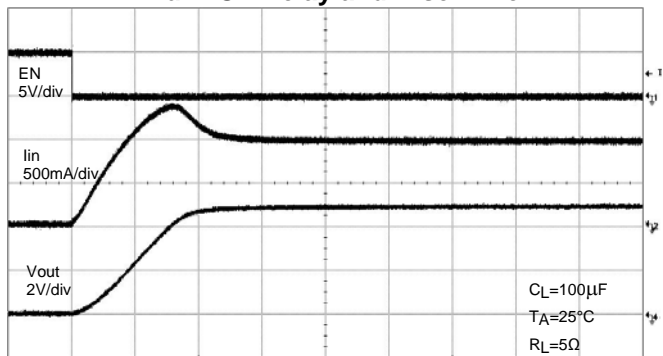
**Turn-Off Delay and Fall Time**



500us/div

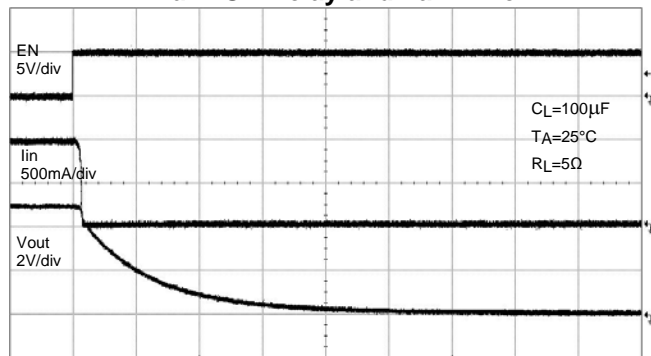
**Typical Performance Characteristics (Continued)**

**Turn-On Delay and Rise Time**



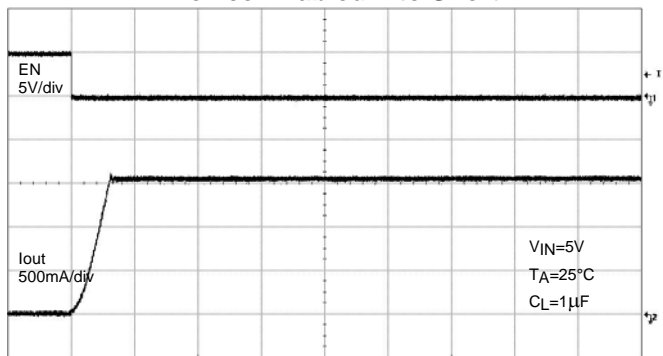
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**Turn-Off Delay and Fall Time**



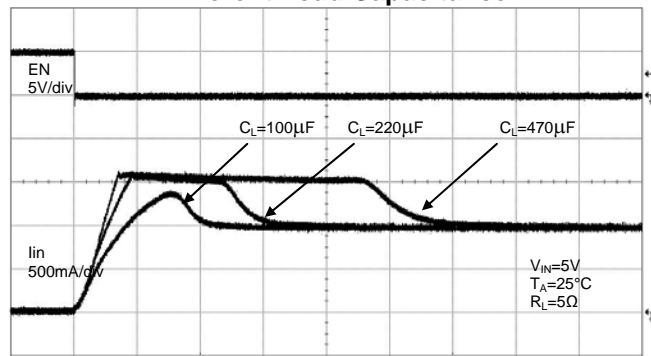
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**Short Circuit Current, Device Enabled Into Short**



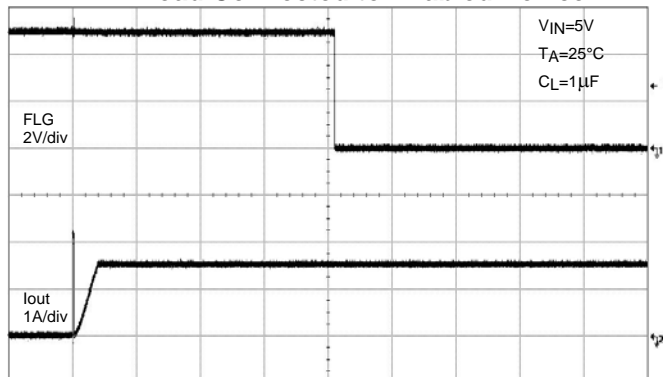
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**Inrush Current with Different Load Capacitance**



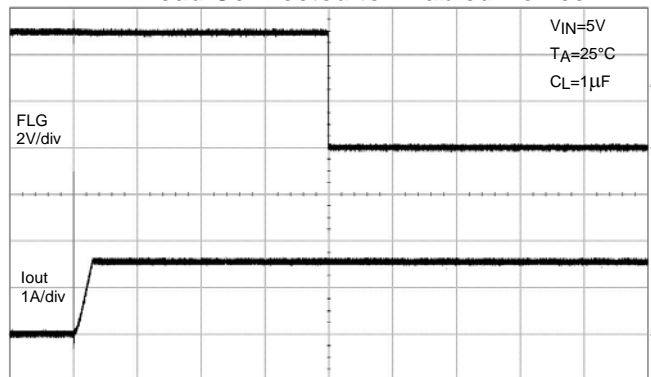
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**2  $\Omega$  Load Connected to Enabled Device**



2ms/div

**1  $\Omega$  Load Connected to Enabled Device**

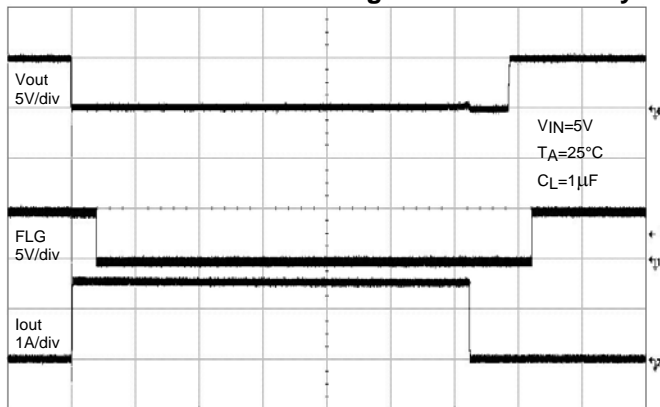


2ms/div

NEW PRODUCT

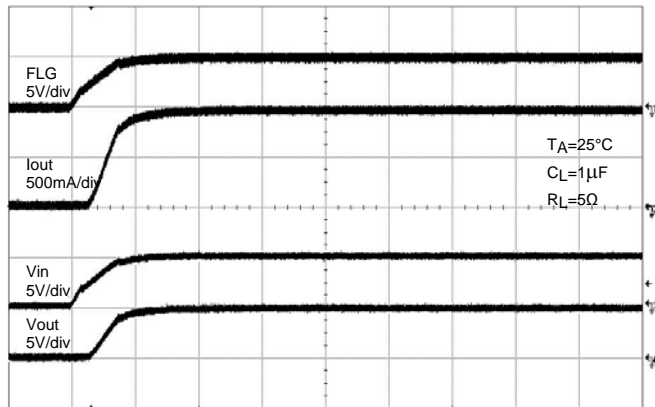
**Typical Performance Characteristics (Continued)**

**Short Circuit with Blanking Time and Recovery**



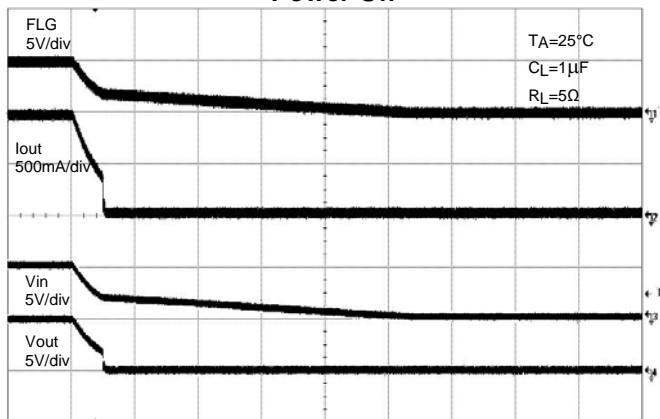
20ms/div

**Power On**



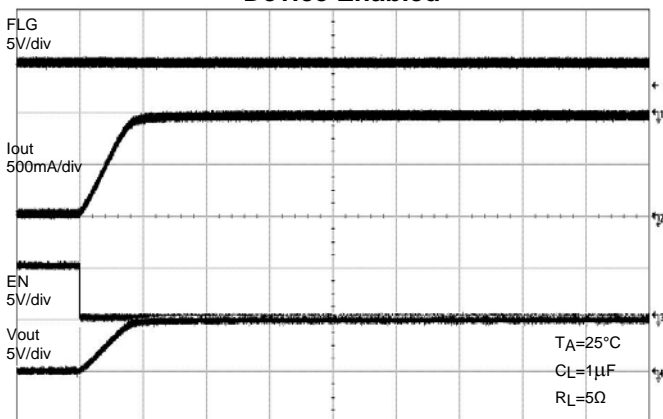
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**Power Off**



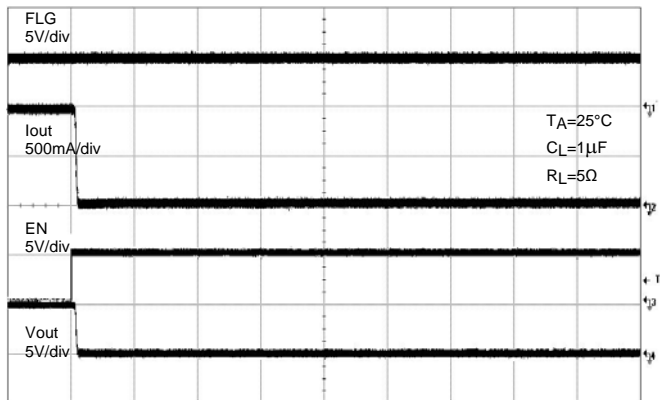
10ms/div

**Device Enabled**



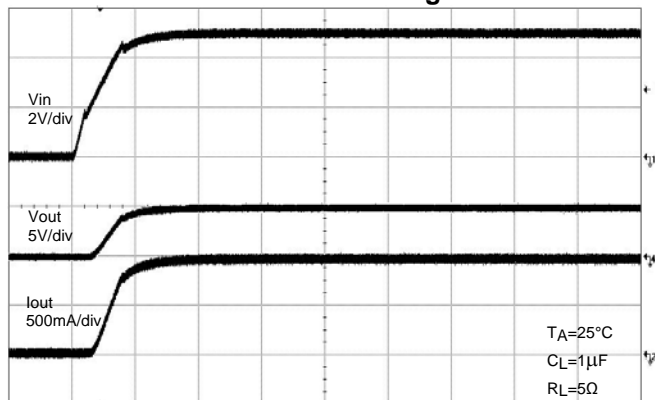
1ms/div

**Device Disabled**



1ms/div

**UVLO Increasing**

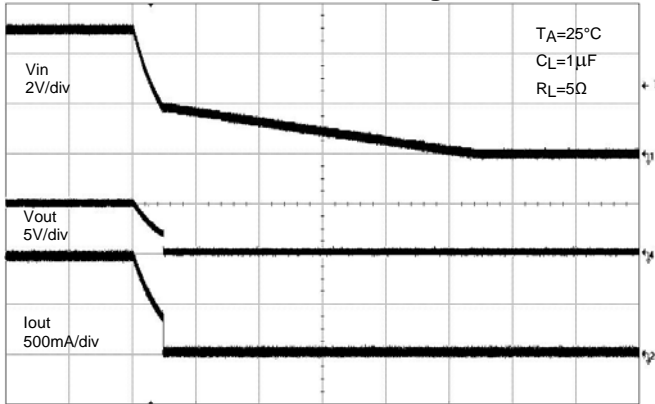


1ms/div

NEW PRODUCT

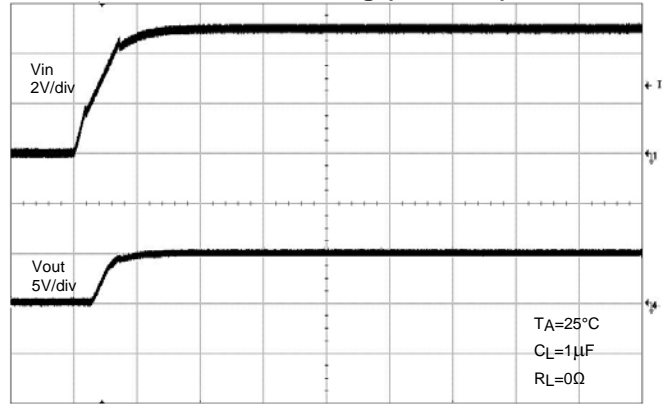
**Typical Performance Characteristics (Continued)**

**UVLO Decreasing**



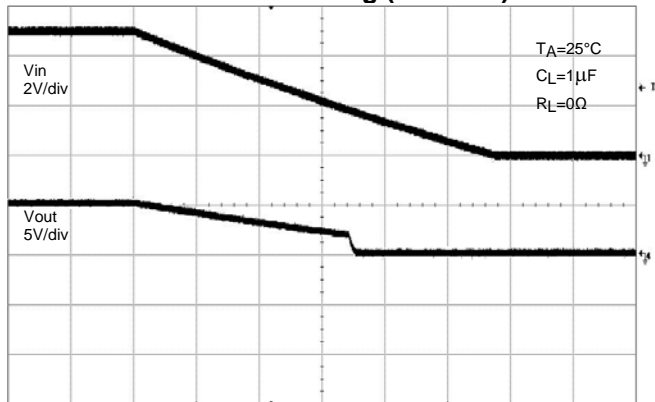
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**UVLO Increasing (No Load)**



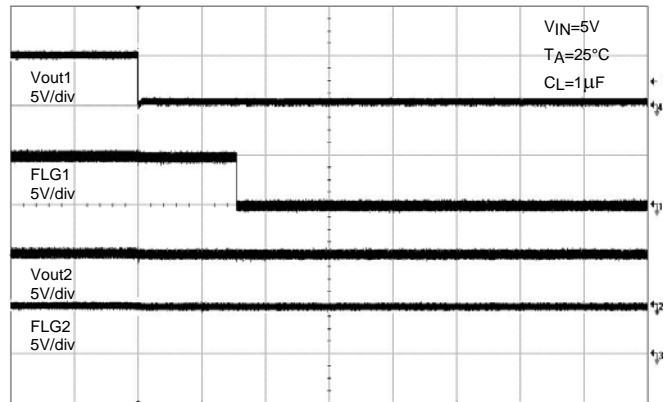
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**UVLO Decreasing (No Load)**



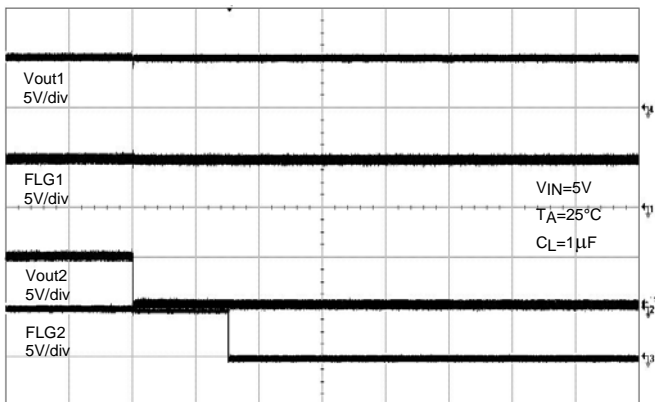
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**Channel 1 Enabled and Shorted with Channel 2 Enabled**



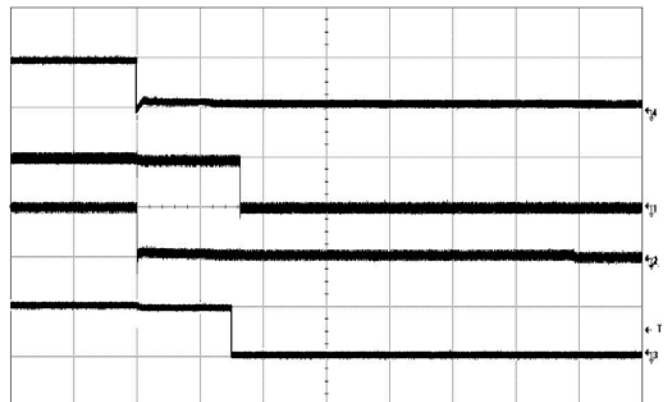
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**Channel 2 Enabled and Shorted with Channel 1 Enabled**



5ms/div

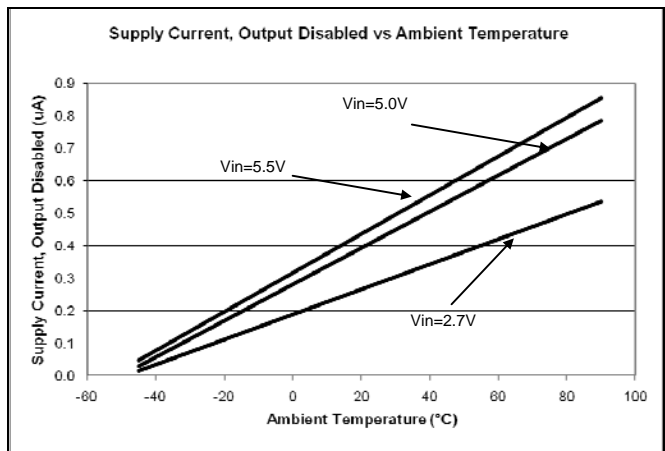
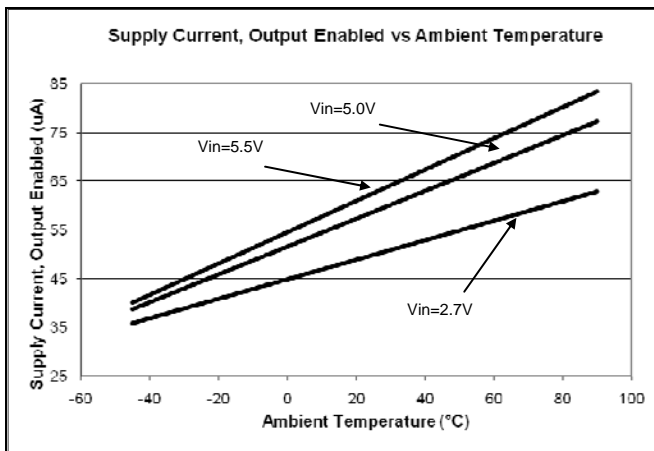
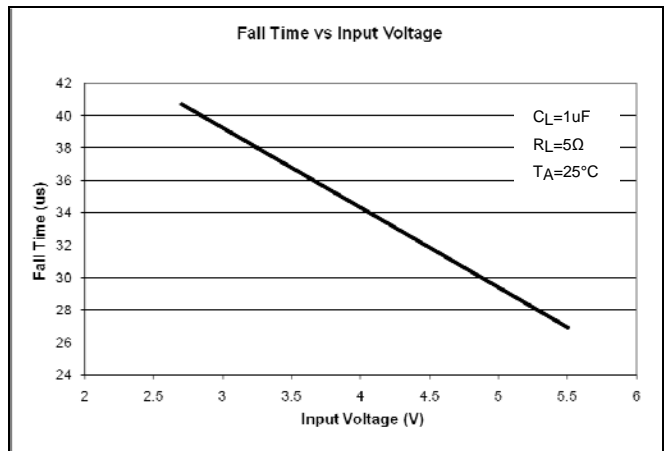
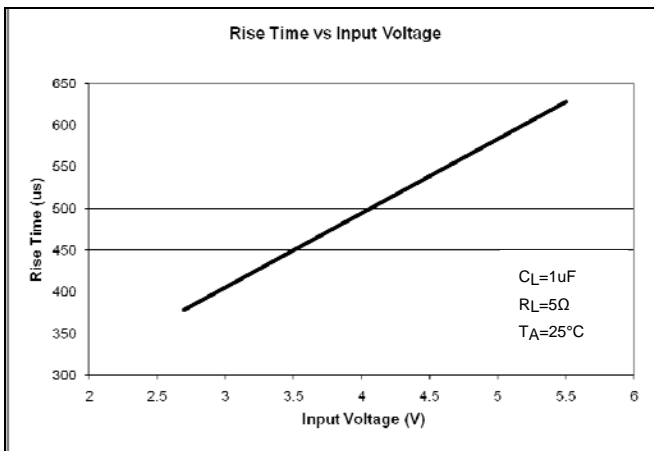
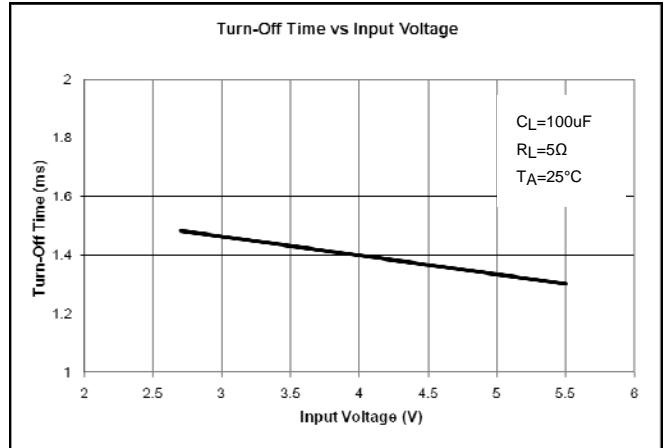
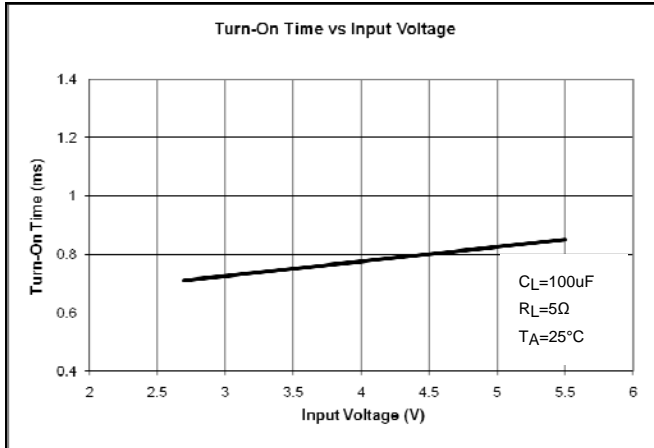
**Channels 1 and 2 Enabled and Shorted**



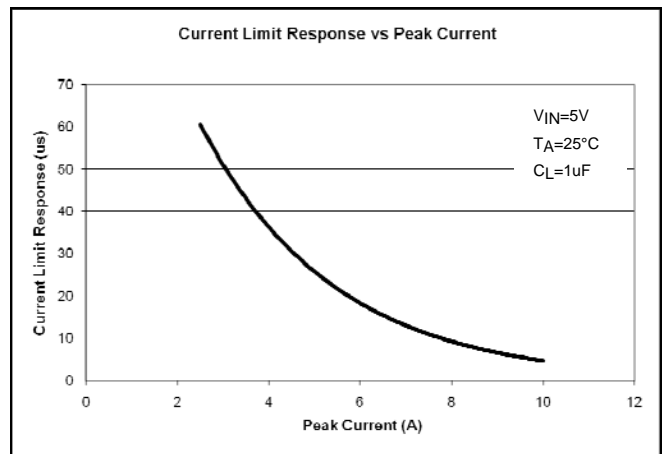
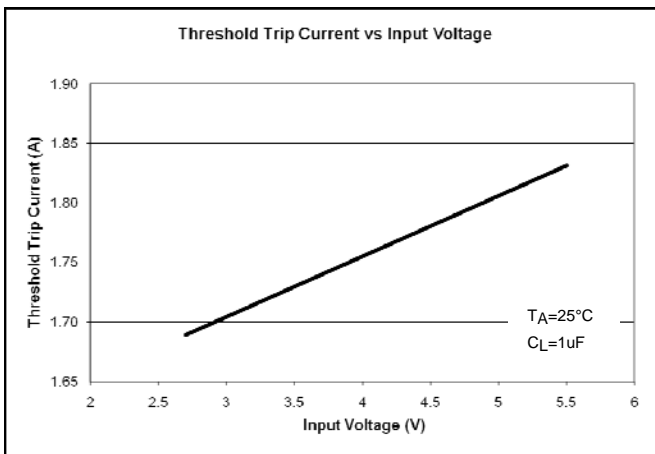
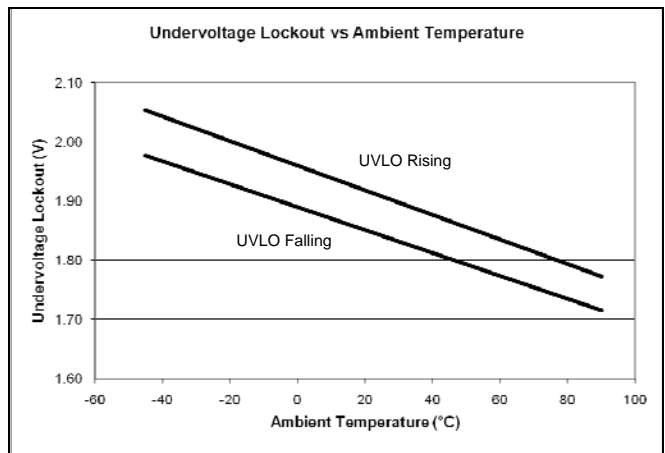
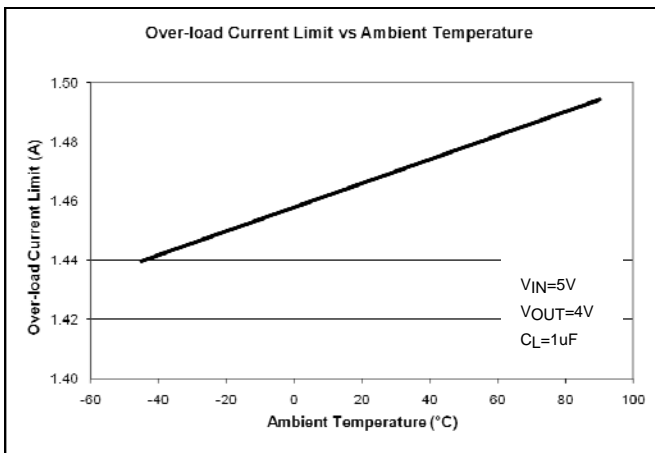
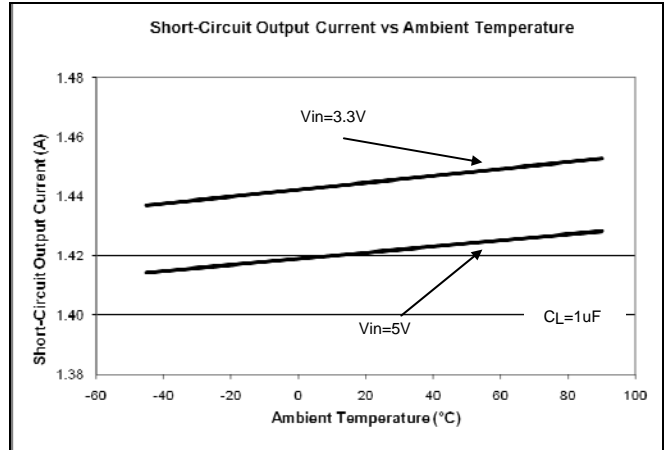
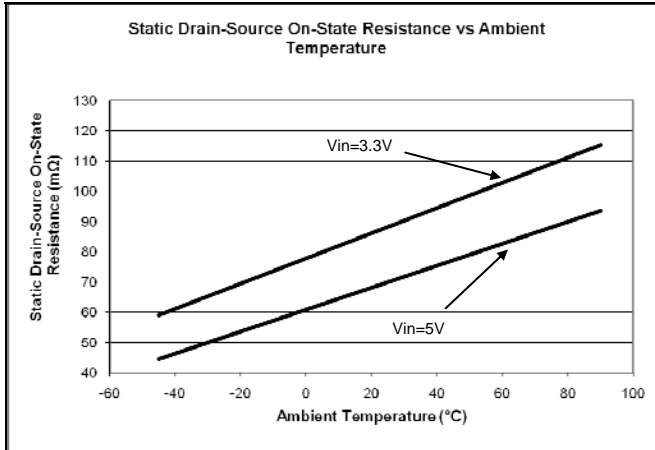
5ms/div



**Typical Performance Characteristics (Continued)**



**Typical Performance Characteristics (Continued)**



## Application Note

### Power Supply Considerations

A 0.1 $\mu$ F to 1 $\mu$ F X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 1 $\mu$ F ceramic capacitor improves the immunity of the device to short-circuit transients.

### Over-current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before  $V_{IN}$  has been applied. The AP2162A/AP2172A senses the short circuit and immediately clamps output current to a certain safe level namely  $I_{LIMIT}$ .

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher inrush current may flow for a very short period of time before the current limit function can react. The input capacitor(s) rapidly discharge through the device, activating current limit circuitry. Protection is achieved by momentarily opening the P-MOS high-side power switch and then gradually turning it on. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at  $I_{LIMIT}$ . The threshold for activating current limiting is 1.4A typical per channel.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold ( $I_{TRIP}$ ) is reached or until the thermal limit of the device is exceeded. The AP2162A/AP2172A is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at  $I_{LIMIT}$ .

### FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7-ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The AP2162A/AP2172A is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

### Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ( $T_A$ ) and  $R_{DS(ON)}$ , the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient temperature °C

$R_{\theta JA}$  = Thermal resistance

$P_D$  = Total power dissipation

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**Application Note (Continued)**

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**Thermal Protection**

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2162A/AP2172A implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately 25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7-ms deglitch.

**Under-voltage Lockout (UVLO)**

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 2V, even if the switch is enabled. Whenever the input voltage falls below approximately 2V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

**Discharge Function**

The discharge function of the device is active when enable is disabled or de-asserted. The discharge function with the N-MOS power switch implementation is activated and offers a resistive discharge path for the external storage capacitor. This is designed for discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

**Host/Self-Powered HUBs**

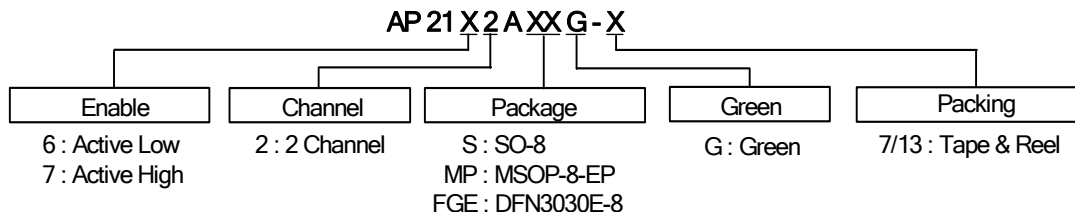
Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports. This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

**Generic Hot-Plug Applications**

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the AP2162A/AP2172A, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2162A/AP2172A also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2162A/AP2172A between the Vcc input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

### Ordering Information

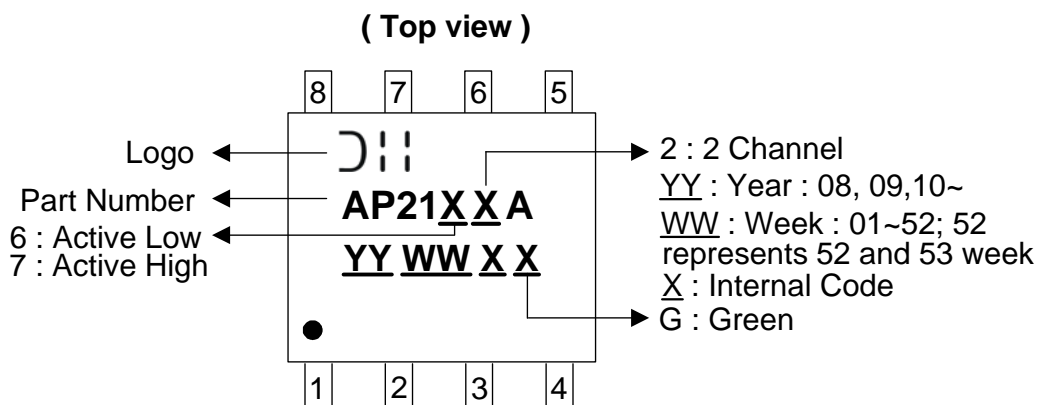


Device	Package Code	Packaging (Note 7)	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP21X2ASG-13	S	SO-8	2500/Tape & Reel	-13
AP21X2AMPG-13	MP	MSOP-8-EP	2500/Tape & Reel	-13
AP21X2AFGEG-7	FGE	DFN3030E-8	3000/Tape & Reel	-7

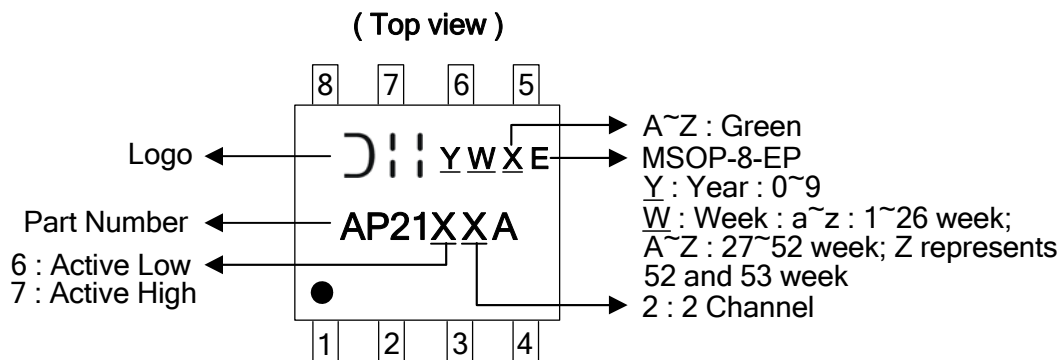
Notes: 7. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

### Marking Information

#### (1) SO-8



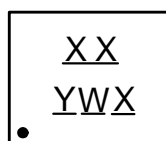
#### (2) MSOP-8-EP



### Marking Information (Continued)

#### (3) DFN3030E-8

#### ( Top View )



XX : Identification Code

Y : Year : 0~9

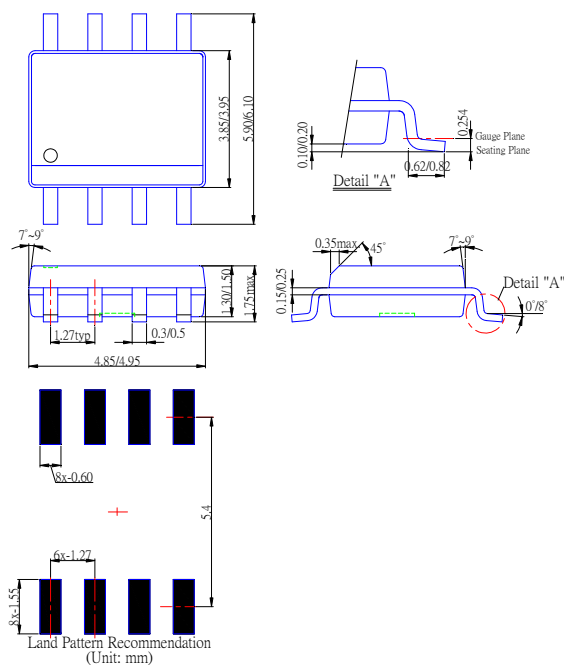
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week

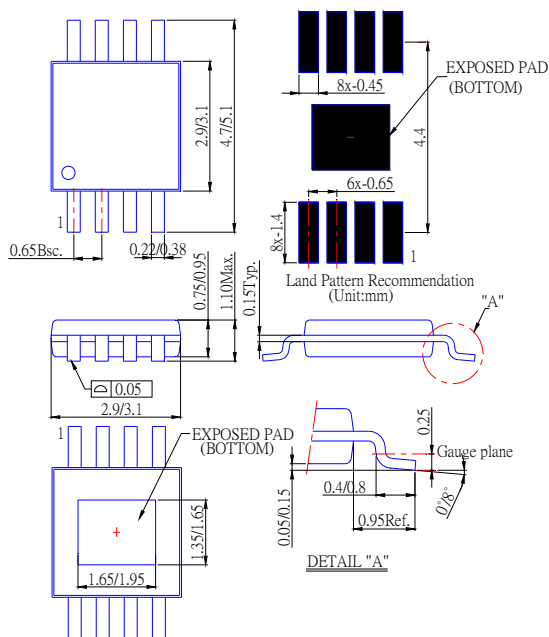
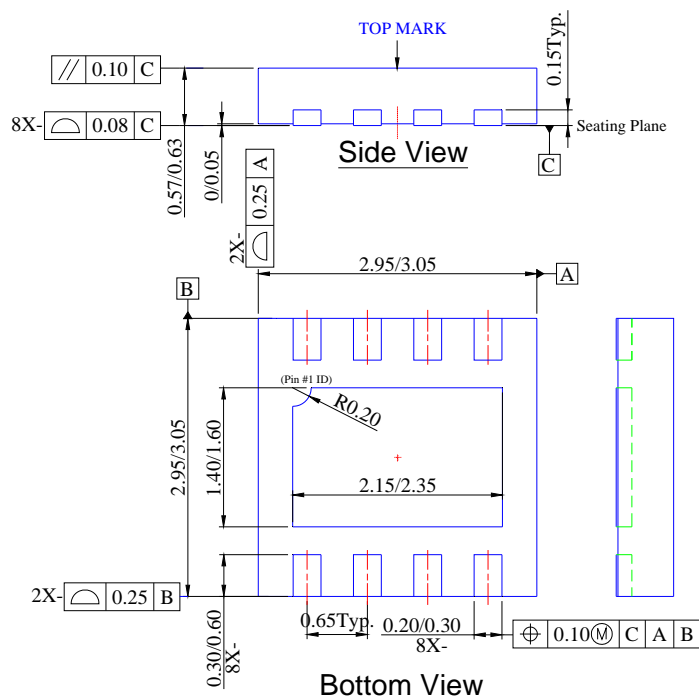
X : A~Z : Green

Part Number	Package	Identification Code
AP2162AFGEG-7	DFN3030E-8	AC
AP2172AFGEG-7	DFN3030E-8	AD

### Package Outline Dimensions (All Dimensions in mm)

#### (1) Package type: SO-8



**Package Outline Dimensions (Continued)****(2) Package type: MSOP-8-EP****(3) Package type: DFN3030E-8**

**Taping Orientation (Note 8)**

For DFN3030E-8



Notes: 8. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>



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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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