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FAIRCHILD SEMICONDUCTOR®

July 2010

FAN6982
CCM Power Factor Correction Controller

Features

- Continuous Conduction Mode
- Innovative Switching-Charge Multiplier-Divider
- Average-Current-Mode for Input-Current Shaping
- TriFault Detect™ Prevent Abnormal Operation for Feedback Loop
- Power-On Sequence Control
- Soft-Start Capability
- Brownout Protection
- Cycle-by-Cycle Peak Current Limiting.
- Improves Light-Load Efficiency
- Fulfills Class-D Requirements of IEC 1000-3-2
- Wide Range Universal AC Input Voltage
- Maximum Duty Cycle 97%
- V_{DD} Under-Voltage Lockout (UVLO)

Applications

- Desktop PC Power Supply
- Internet Server Power Supply
- LCD TV/Monitor Power Supply
- DC Motor Power Supply

Description

The FAN6982 is a 14-pin, Continuous Conduction Mode (CCM) PFC controller IC intended for Power Factor Correction (PFC) pre-regulators. The FAN6982 includes circuits for the implementation of leading edge, average current, “boost”-type power factor correction, and results in a power supply that fully complies with the IEC1000-3-2 specification.

A TriFault Detect™ function helps reduce external components and provides full protection for feedback loops such as open, short, and over voltage. An over-voltage comparator shuts down the PFC stage in the event of a sudden load decrease. The RDY signal can be used for power-on sequence control. The EN function can choose to enable or disable the range function. FAN6982 also includes PFC soft-start, peak current limiting, and input voltage brownout protection.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6982MY	-40°C to +105°C	14-Pin Small Outline Package (SOP)	Tape & Reel

Application Diagram

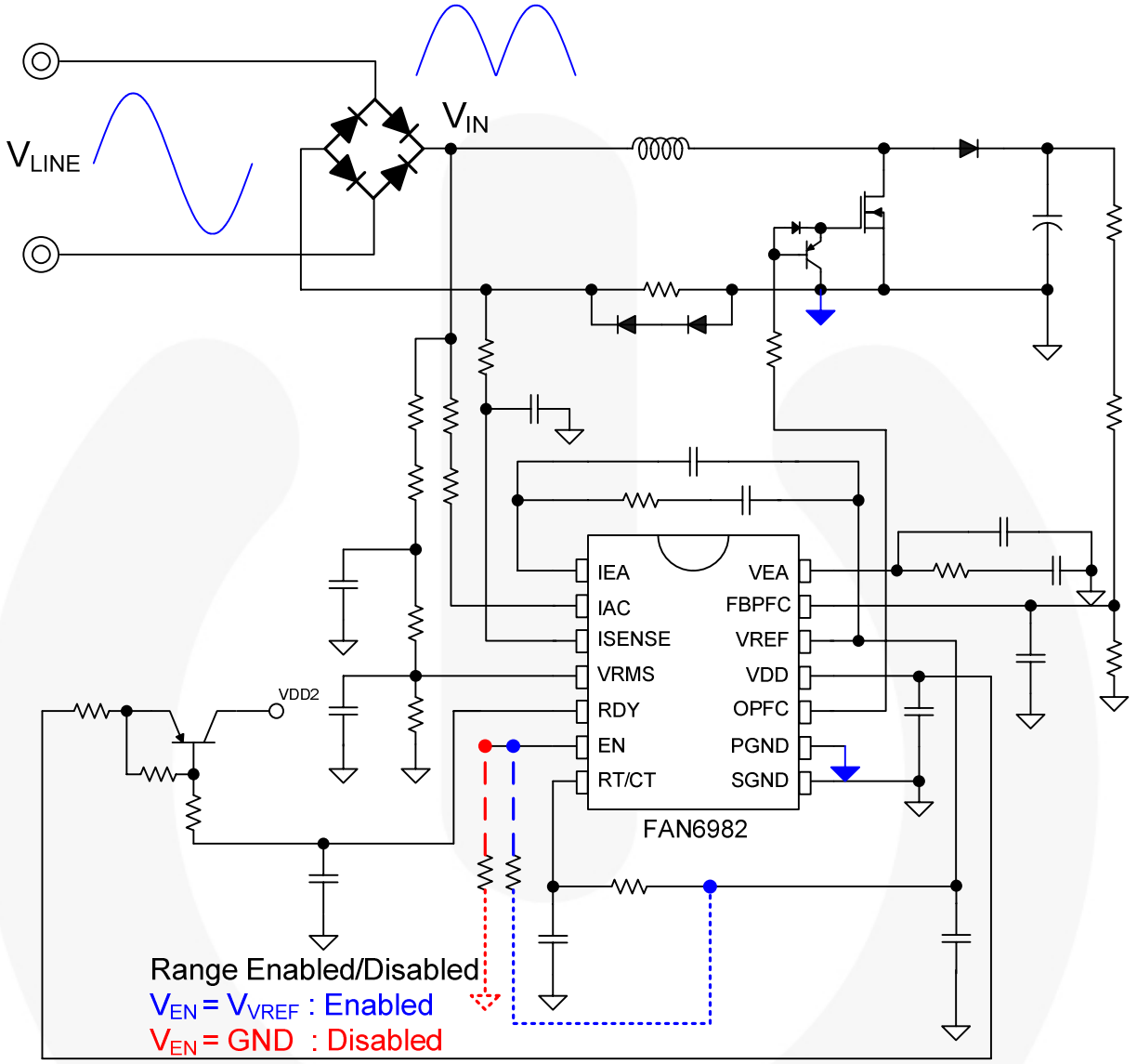


Figure 1. Typical Application

Block Diagram

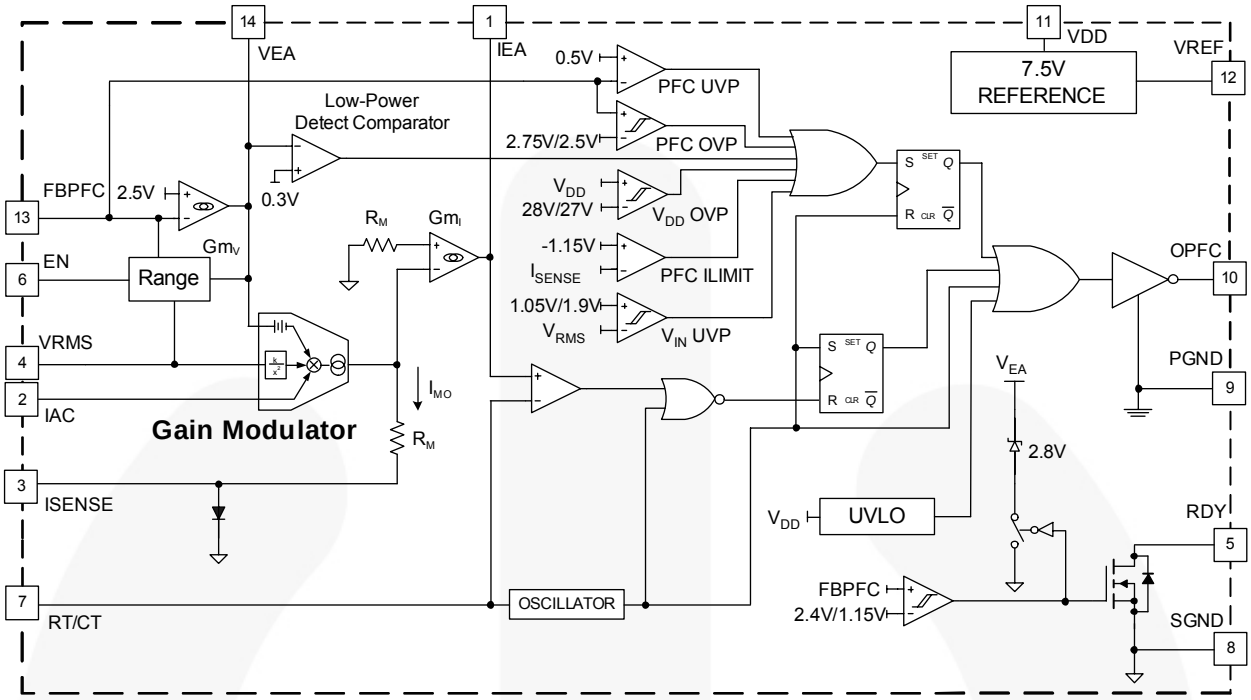
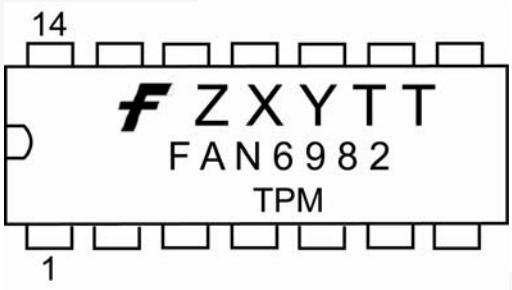


Figure 2. Functional Block Diagram

Marking Information



F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2-Digit Die-Run Code
T – Package Type (M: SOP)
P – Y: Green Package
M – Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

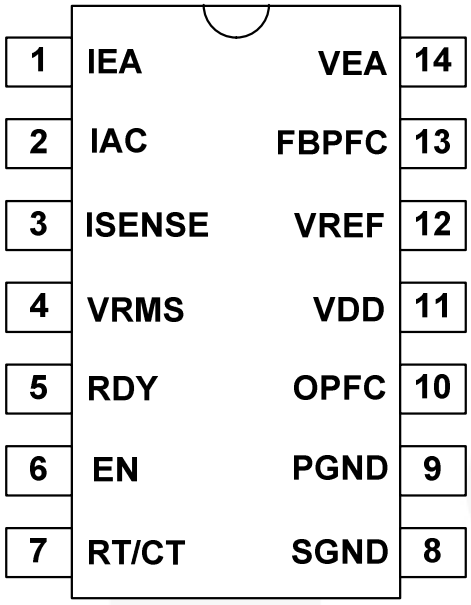


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	IEA	**Output of Current Amplifier**. This is the output of the PFC current amplifier. The signal from this pin is compared with sawtooth and determines the pulsewidth for PFC gate drive.
2	IAC	**Input AC Current**. For normal operation, this input is used to provide current reference for the multiplier. The suggested maximum I_{AC} is 100μA.
3	ISENSE	**Current Sense**. The non-inverting input of the PFC current amplifier and the output of multiplier and PFC I_{LIMIT} comparator.
4	VRMS	**Line-Voltage Detection**. The pin is used for PFC multiplier.
5	RDY	**Ready Signal**. This pin controls the power-on sequence. Once the FAN6982 is turned on and the FBPFC voltage exceeds in 2.4V, the RDY pin pulls LOW impedance. If the FBPFC voltage is lower than 1.15V, the RDY pin pulls HIGH impedance.
6	EN	**Enable Range Function**. The range function is enabled when EN is connected to V_{REF}. The range function is disabled when EN is connected to GND.
7	RT/CT	**Oscillator RC Timing Connection**. Oscillator timing node; timing set by RT and CT.
8	SGND	**Signal Ground**.
9	PGND	**Power Ground**.
10	OPFC	**Gate Drive**. The totem-pole output drive for PFC MOSFET. This pin is internally clamped under 15V to protect the MOSFET.
11	VDD	**Power Supply**. The threshold voltages for startup and turn-off are 11V and 9.3V, respectively. The operating current is lower than 10mA.
12	VREF	**Reference Voltage**. Buffered output for the internal 7.5V reference.
13	FBPFC	**Voltage Feedback Input**. The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
14	VEA	**Output of Voltage Amplifier**. The error-amplifier output for PFC voltage feedback loop. A compensation network is connected between this pin and ground.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			30	V
V_H	OPFC, RDY, EN, VREF		-0.3	30.0	V
V_L	IAC, VRMS, RT/CT, FBPFC, VEA		-0.3	7.0	V
V_{IEA}	IEA		0	V_{VREF}+0.3	V
V_N	ISENSE		-5.0	0.7	V
I_{AC}	Input AC Current			1	mA
I_{REF}	VREF Output Current			5	mA
$I_{PFC-OUT}$	Peak PFC OUT Current, Source or Sink			0.5	A
P_D	Power Dissipation, T_A < 50°C			800	mW
$R_{\Theta j-a}$	Thermal Resistance (Junction-to-Air)			104.10	°C/W
$R_{\Theta j-c}$	Thermal Resistance (Junction-to-Case)			40.61	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Soldering)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4.5	kV
		Charged Device Model, JESD22-C101		1.0	

Notes:
1. All voltage values, except differential voltage, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

Unless otherwise noted; V_{DD}=15V, T_A= 25°C, T_A=T_J, R_T=27kΩ, and C_T=1000pF.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuously Operating Voltage				22	V
$I_{DD\ ST}$	Startup Current	V_{DD}=V_{TH-ON}-0.1V; OPFC Open		30	80	µA
I_{DD-OP}	Operating Current	V_{DD}=13V; OPFC Open	2.0	2.3	3.0	mA
V_{TH-ON}	Turn-on Threshold Voltage		10	11	12	V
$\triangle V_{TH}$	Hysteresis		1.35		1.90	V
V_{DD-OVP}	V_{DD} OVP		27	28	29	V
$\triangle V_{DD-OVP}$	V_{DD} OVP Hysteresis			1		V
Oscillator						
f_{OSC}	PFC Frequency	R_T=27kΩ, C_T=1000pF	60	64	67	kHz
f_{DV}[3]	Voltage Stability	11V ≦ V_{DD} ≦ 22V			2	%
f_{DT}[3]	Temperature Stability	-40°C ~ +105°C			2	%
f_{TV}	Total Variation	Line, Temperature	58		70	kHz
f_{RV}	Ramp Voltage	Valley-to-Peak		2.8		V
$I_{OSC-DIS}$	Discharge Current	V_{RAMP}=0V, $V_{RT/CT}$=2.5V	6.5		15.0	mA
f_{RANGE}	Frequency Range		50		75	kHz
$t_{PFC-DEAD}$	PFC Dead Time	R_T=27kΩ, C_T=1000pF	400	600	800	ns
V_{REF}						
V_{VREF}	Reference Voltage	I_{REF}=0mA, C_{REF}=0.1µF	7.4	7.5	7.6	V
$\triangle V_{VREF1}$	Load Regulation of Reference Voltage	C_{REF}=0.1µF, I_{REF}=0mA to 3.5mA V_{VDD}=14V, Rise/Fall Time > 20µs		30	50	mV
$\triangle V_{VREF2}$	Line Regulation of Reference Voltage	C_{REF}=0.1µF, V_{VDD}=11V to 22V			25	mV
$\triangle V_{VREF-DT}$	Temperature Stability[3]	-40°C ~ +105°C		0.4	0.5	%
$\triangle V_{VREF-TV}$	Total Variation[3]	Line, Load, Temperature	7.35		7.65	V
$\triangle V_{VREF-LS}$	Long-Term Stability[3]	T_J=125°C, 0 ~ 1000HRs	5		25	mV
$I_{REF-MAX}$	Maximum Current	V_{VREF} > 7.35V	5			mA
Brownout						
$V_{RMS-UVL}$	V_{RMS} Threshold Low	When V_{RMS}=1.05V at 75 V_{RMS}	1.00	1.05	1.10	V
$V_{RMS-UVH}$	V_{RMS} Threshold High	When V_{RMS}=1.9V at 85 • 1.414	1.85	1.90	1.95	V
$\triangle V_{RMS-UVP}$	Hysteresis		750	850	950	mV
t_{UVP}	Under-Voltage Protection Debounce Time		340	410	480	ms
RDY Section						
$V_{FBPFC-RD}$	FBPFC Voltage Level to Pull Low Impedance with RDY Pin		2.3	2.4	2.5	V
$\triangle V_{FBPFC-RD}$	Hysteresis		1.15	1.25	1.35	V
$I_{RDY-LEK}$	Leakage Current of RDY High Impedance	V_{FBPFC}<2.4V			500	nA
V_{RDY-L}	RDY Low Voltage	I_{SINK}=2mA			0.5	V

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise noted; V_{DD}=15V, T_A= 25°C, T_A=T_J, R_T=27kΩ, and C_T=1000pF.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Error Amplifier						
V_{REF}	Reference Voltage		2.45	2.50	2.55	V
A_V	Open-Loop Gain(3)	At T_A=25°C	35	42		dB
Gm_V	Transconductance	V_{NONINV}=V_{INV}, V_{VEA}=3.75V at T_A=25°C	50	70	90	μmho
$I_{FBPFC-L}$	Maximum Source Current	V_{FBPFC}=2V, V_{VEA}=1.5V	40	50		μA
$I_{FBPFC-H}$	Maximum Sink Current	V_{FBPFC}=3V, V_{VEA}=6V		-50	-40	μA
I_{BS}	Input Bias Current		-1		1	μA
V_{VEA-H}	Output High Voltage on V_{VEA}		5.8	6.0		V
V_{VEA-L}	Output Low Voltage on V_{VEA}			0.1	0.4	V
Current Error Amplifier						
V_{ISENSE}	Input Voltage Range		-1.5		0.7	V
A_I	Open-Loop Gain(3)	At T_A=25°C	40	50		dB
Gm_I	Transconductance	V_{NONINV}=V_{INV}, V_{IEA}=3.75V	75	88	100	μmho
V_{OFFSET}	Input Offset Voltage	V_{VEA}=0V, I_{AC} Open	-10		10	mV
V_{IEA-H}	Output High Voltage		6.8	7.4	8.0	V
V_{IEA-L}	Output Low Voltage			0.1	0.4	V
I_L	Source Current	V_{ISENSE}= -0.6V, V_{IEA}=1.5V	35	50		μA
I_H	Sink Current	V_{ISENSE}= +0.6V, V_{IEA}=4.0V		-50	-35	μA
PFC OVP Comparator						
$V_{FBPFC-OVP}$	Over Voltage Protection		2.70	2.75	2.80	V
$\triangle V_{FBPFC-OVP}$	PFC OVP Hysteresis		200	250	300	mV
Low-Power Detect Comparator						
$V_{VEA-OFF}$	VEA Voltage Off OPFC		0.2	0.3	0.4	V
PFC Soft-Start						
V_{VEA_CLAMP}	PFC Soft-Start	V_{FBPFC} < 2.4V	2.2	2.8	3.3	V
EN Section						
V_{EN-H}	High Voltage Level of V_{EN}	V_{EN}=V_{VREF}	7.4	7.5	7.6	V
V_{EN-L}	Low Voltage Level of V_{EN}	V_{EN}=GND		0		V
Range						
V_{VRMS-L}	RMS AC Voltage Low	When V_{VRMS}=1.95V at 132V_{RMS}	1.90	1.95	20.00	V
V_{VRMS-H}	RMS AC Voltage High	When V_{VRMS}=2.45V at 150 V_{RMS}	2.40	2.45	2.50	V
V_{VEA-L}	VEA Low	When V_{VEA}=1.95V at 30% Loading	1.90	1.95	2.00	V
V_{VEA-H}	VEA High	When V_{VEA}=2.45V at 40% Loading	2.40	2.45	2.50	V
I_{TC}	Source Current from FBPFC		18	20	22	μA

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise noted; V_{DD}=15V, T_A= 25°C, T_A=T_J, R_T=27kΩ, and C_T=1000pF.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Gain Modulator						
I_{AC}	Input for AC Current	Multiplier Linear Range	0		100	µA
GAIN	Gain Modulator(3)(4)	I_{IAC}=17.67µA, V_{VRMS}=1.080V V_{FBPFC}=2.25V, at T_A=25°C	7.500	9.000	10.500	
		I_{IAC}=20µA, V_{VRMS}=1.224V V_{FBPFC}=2.25V, at T_A=25°C	6.367	7.004	7.704	
		I_{IAC}=25.69µA, V_{VRMS}=1.585V V_{FBPFC}=2.25V, at T_A=25°C	3.801	4.182	4.600	
		I_{IAC}=51.62µA, V_{VRMS}=3.169V V_{FBPFC}=2.25V, at T_A=25°C	0.950	1.045	1.149	
		I_{IAC}=62.23µA, V_{VRMS}=3.803V V_{FBPFC}=2.25V, at T_A=25°C	0.660	0.726	0.798	
BW	Bandwidth	I_{IAC}=40µA		2		kHz
$V_{O(GM)}$	Output Voltage=5.7kΩ × (I_{SENSE}-I_{OFFSET})	I_{AC}=20µA, V_{RMS}=1.224V V_{FBPFC}=2.25V, at T_A=25°C	0.710	0.798	0.885	V
PFC I_{LIMIT} Comparator						
$V_{PFC-ILIMIT}$	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit		-1.25	-1.15	-1.05	V
$\triangle V_{pk}$	PFC I_{LIMIT}-Gain Modulator Output	I_{IAC}=17.67µA, V_{VRMS}=1.08V V_{FBPFC}=2.25V, at T_A=25°C	200			mV
PFC Output Driver						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V	13	15	17	V
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V; I_O=100mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=13V; I_O=100mA	8			V
t_R	Gate Rising Time	V_{DD}=15V; C_L=4.7nF; O/P= 2V to 9V	40	70	120	ns
t_F	Gate Falling Time	V_{DD}=15V; C_L=4.7nF; O/P= 9V to 2V	40	60	110	ns
$D_{PFC-MAX}$	Maximum Duty Cycle	V_{IEA}<1.2V	94	97		%
$D_{PFC-MIN}$	Minimum Duty Cycle	V_{IEA}>4.5V			0	%
Tri-Fault Detect						
t_{FBPFC_OPEN}	Time to FBPFC Open	V_{FBPFC}=$V_{FBPFC-OVP}$ to FBPFC OPEN, 470pF from FBPFC to GND		2	4	ms
$V_{PFC-UVP}$	PFC Feedback Under-Voltage Protection		0.4	0.5	0.6	V

Notes:

3. This parameter, although guaranteed by design, is not 100% production tested.
4. This gain is the maximum gain of modulation with a given V_{RMS} voltage when V_{EA} is saturated to high.

Typical Performance Characteristics

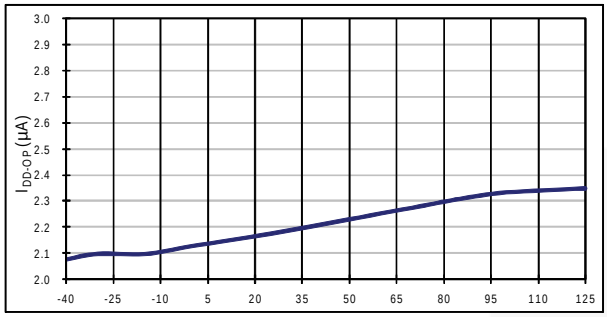


Figure 5. I_{DD-OP} vs. Temperature

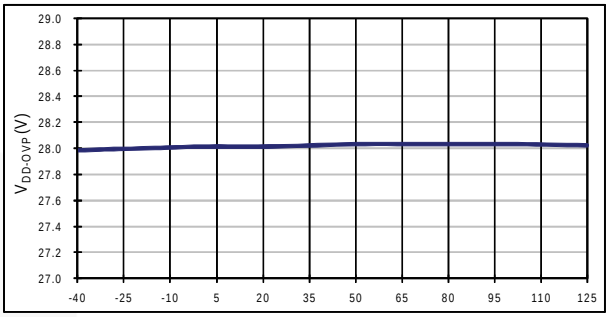


Figure 6. V_{DD-OVP} vs. Temperature

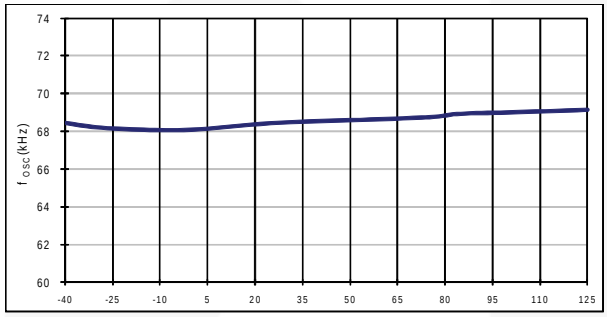


Figure 7. f_{OSC} vs. Temperature

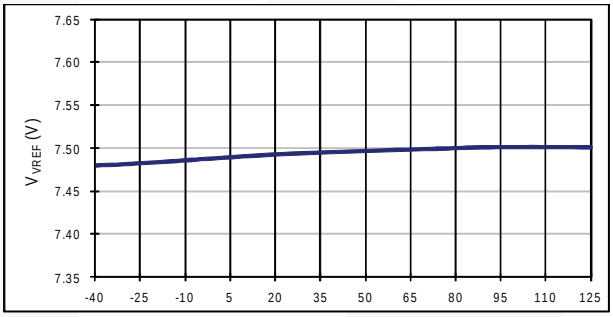


Figure 8. V_{VREF} vs. Temperature

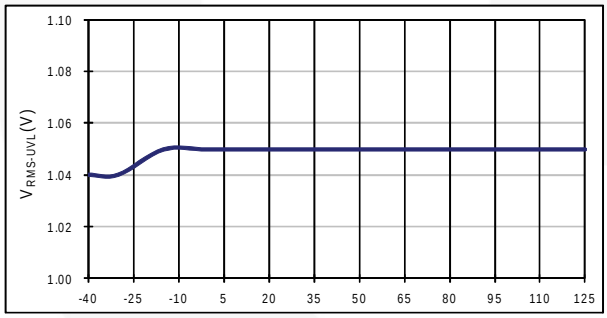


Figure 9. $V_{RMS-UVL}$ vs. Temperature

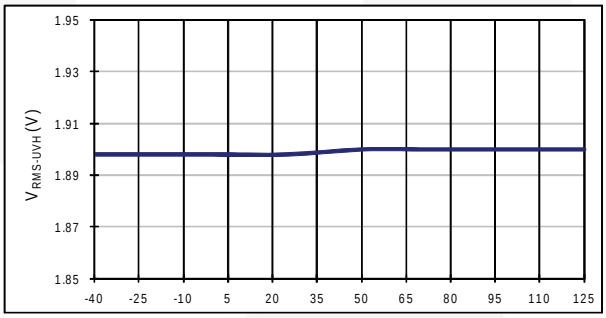


Figure 10. $V_{RMS-UVH}$ vs. Temperature

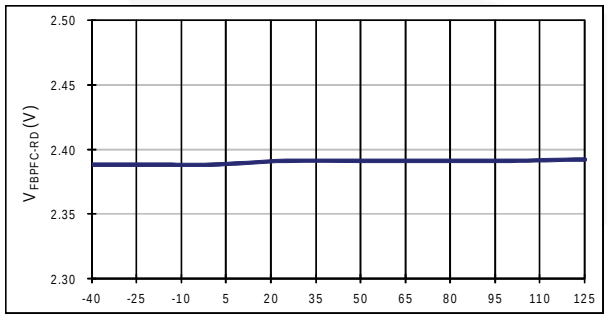


Figure 11. $V_{FBPFC-RD}$ vs. Temperature

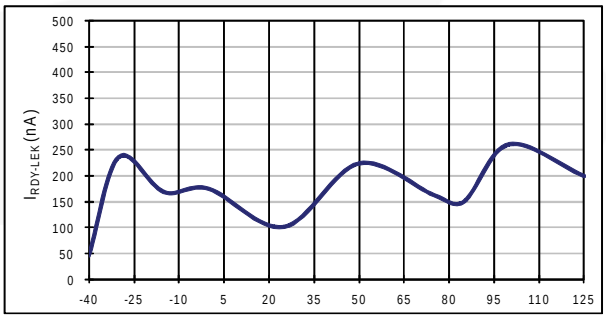


Figure 12. $I_{RDY-LEK}$ vs. Temperature

Typical Performance Characteristics (Continued)

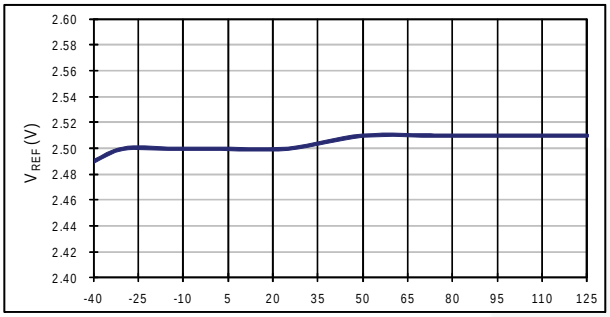


Figure 13. V_{REF} vs. Temperature

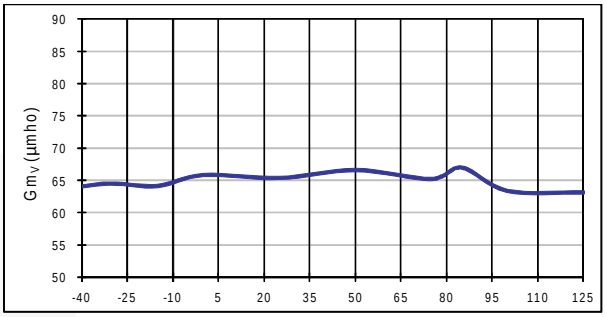


Figure 14. Gm_V vs. Temperature

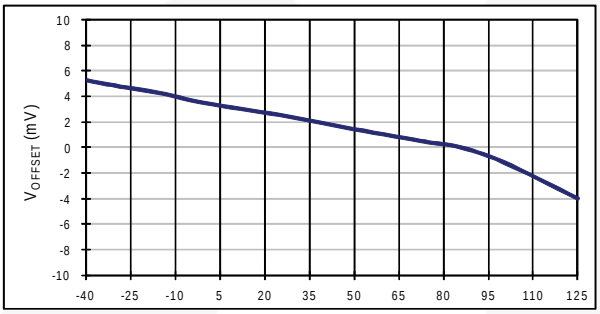


Figure 15. V_{OFFSET} vs. Temperature

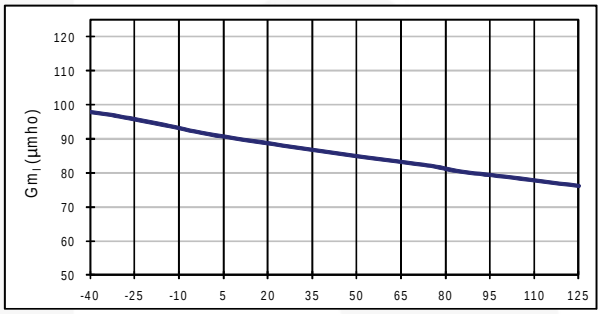


Figure 16. Gm_I vs. Temperature

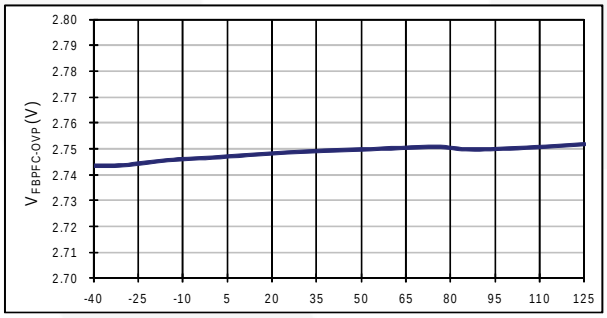


Figure 17. $V_{FBPFC-OVP}$ vs. Temperature

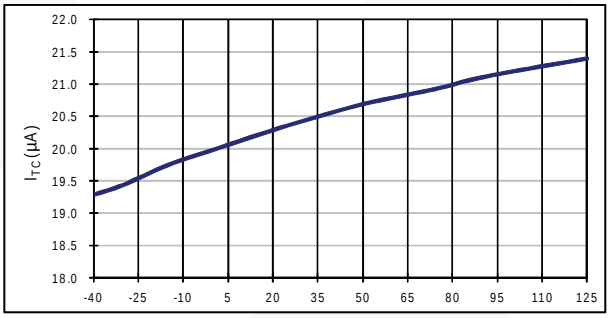


Figure 18. I_{TC} vs. Temperature

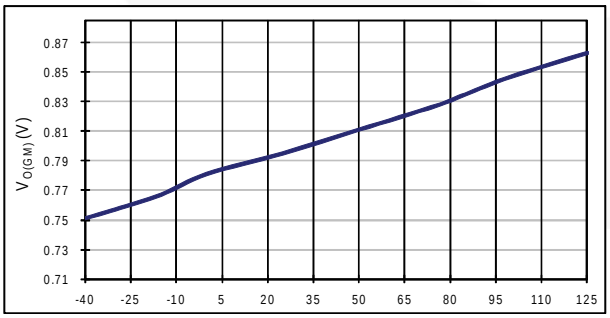


Figure 19. $V_{O(GM)}$ vs. Temperature

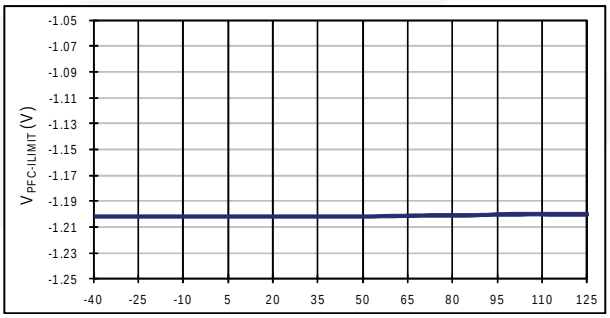


Figure 20. $V_{PFC-ILIMIT}$ vs. Temperature

Typical Performance Characteristics (Continued)

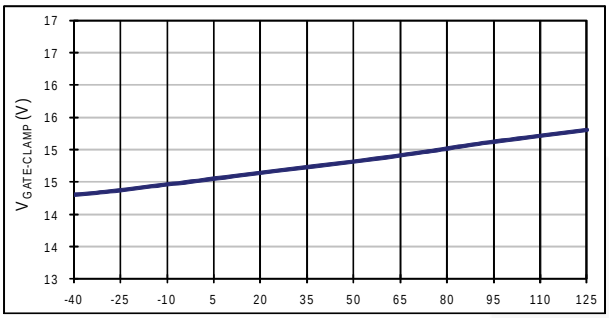


Figure 21. $V_{GATE-CLAMP}$ vs. Temperature

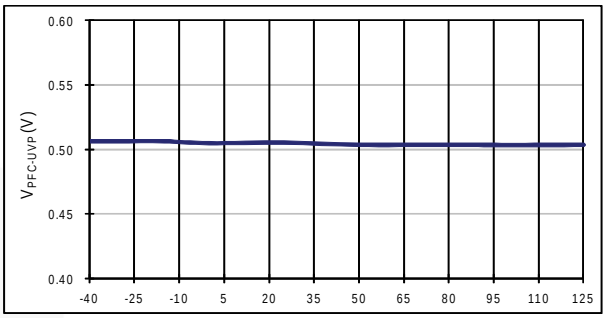


Figure 22. $V_{PFC-UVP}$ vs. Temperature

Functional Description

Oscillator

The internal oscillator frequency of FAN6982 is determined by the timing resistor and capacitor on the RT/CT pin, but note that the optimum operation for FAN6982 is between 50 and 75kHz. The frequency of the internal oscillator is given by:

$$f_{OSC} = \frac{1}{0.56 \cdot R_T \cdot C_T + 360 C_T} \quad (1)$$

The dead time for the PFC gate drive signal is determined by

$$t_{DEAD} = 360 C_T \quad (2)$$

The dead time should be smaller than 2% of switching period to minimize line current distortion around line zero crossing.

Gain Modulator

Gain modulator is the key block for PFC stage because it provides the reference to the current control error amplifier for the input current shaping, as shown in Figure 23. The output current of gain modulator is a function of V_{EA}, I_{AC} and V_{RMS}. The gain of the gain modulator is given as a ratio between I_{MO} and I_{AC} with a given V_{RMS} when V_{EA} is saturated to high. The gain is inversely proportional to V_{RMS}^2, as shown in Figure 24, to implement line feed-forward. This automatically adjusts the reference of current control error amplifier according to the line voltage such that the input power of PFC converter is not changed with line voltage, as shown in, Figure 25.

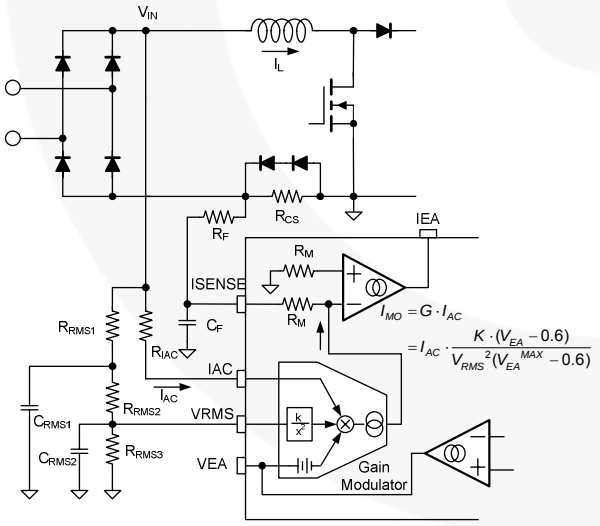


Figure 23. Gain Modulator Block

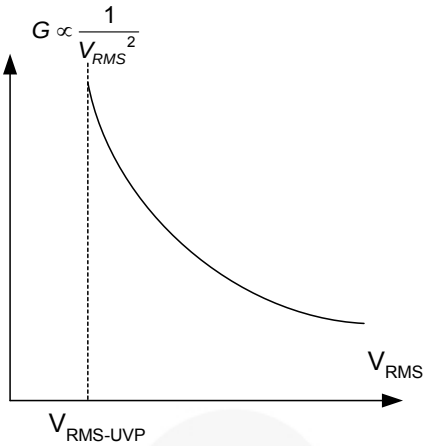


Figure 24. Modulation Gain Characteristics

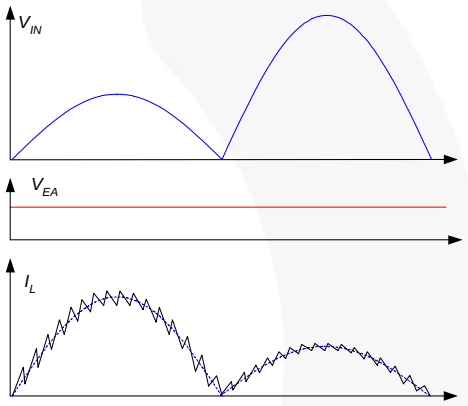


Figure 25. Line Feed-Forward Operation

To sense the RMS value of the line voltage, an averaging circuit with two poles is typically employed as shown in Figure 23. Notice that the input voltage of PFC is clamped at the peak of the line voltage once PFC stops switching since the junction capacitance of bridge diode is not discharged, as shown in Figure 26.

Therefore, the voltage divider for V_{RMS} should be designed considering the brownout protection trip point and minimum operation line voltage.

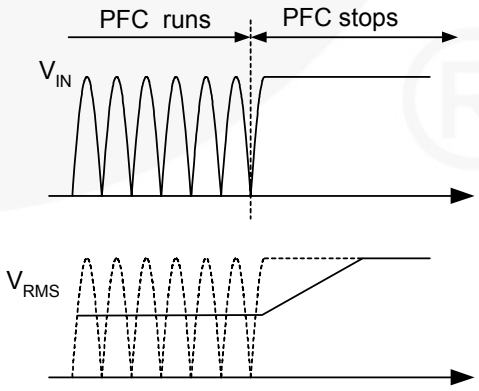


Figure 26. V_{RMS} According to the PFC Operation

The rectified sinusoidal signal is obtained by the current flowing into the IAC pin. The resistor R_{IAC} should be large enough to prevent saturation of the gain modulator as:

$$\frac{\sqrt{2}V_{LINE.BO}}{R_{IAC}} \cdot G^{MAX} < 159\mu A \quad (3)$$

where $V_{LINE.BO}$ is the line voltage that trips brownout protection, G^{MAX} is the maximum modulator gain when V_{RMS} is 1.08V, and 159μA is the maximum output current of the gain modulator.

Current-Control of Boost Stage

As shown in Figure 27 the FAN6982 employs two control loops for power factor correction, a current-control loop and a voltage-control loop. The current-control loop shapes inductor current, as shown in Figure 28, based on the reference signal obtained at IAC pin as:

$$I_L \cdot R_{CS1} = I_{MO} \cdot R_M = I_{AC} \cdot G \cdot R_M \quad (4)$$

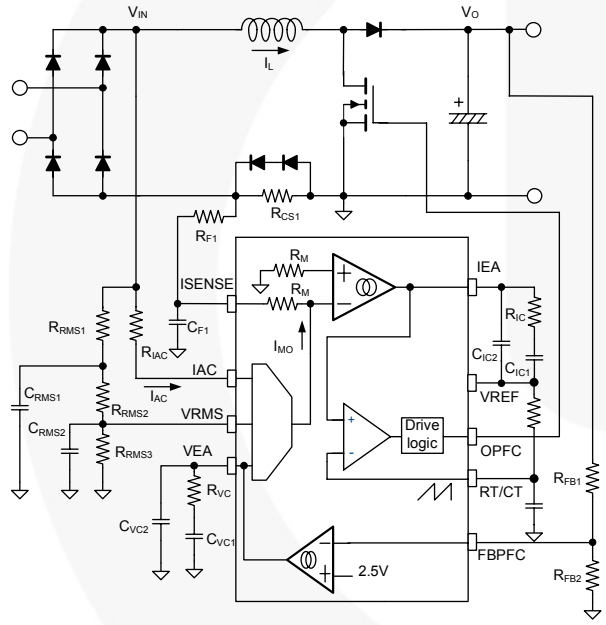


Figure 27. Gain Modulation Block

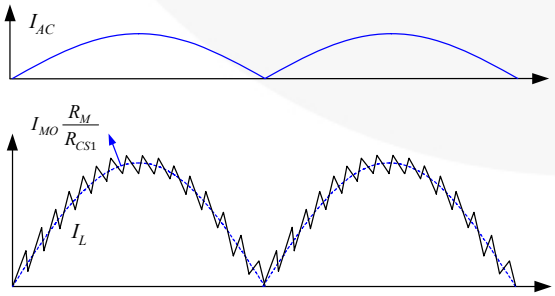


Figure 28. Inductor Current Shaping

The current-control feedback loop also has a pulse-by-pulse current limit comparator that forces the PFC switch to turn off if the ISENSE pin voltage drops below -1.15V until the next switching cycle.

Voltage-Control of Boost Stage

The voltage-control loop regulates PFC output voltage using internal error amplifier such that the FBPFC voltage is same as internal reference of 2.5V.

To improve system efficiency at low AC line voltage and light-load condition, FAN6982 provides adjustable PFC output voltage. As shown in Figure 29, FAN6982 monitors V_{EA} and V_{RMS} to adjust the PFC output voltage. When V_{EA} and V_{RMS} are lower than thresholds, internal current source of 20μA is enabled that flows through R_{FB2}, increasing the voltage of the FBPFC pin. This causes the PFC output voltage to reduce when 20μA is enabled as:

$$V_{OPFC2} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times (2.5 - 20\mu A \times R_{FB2}) \quad (5)$$

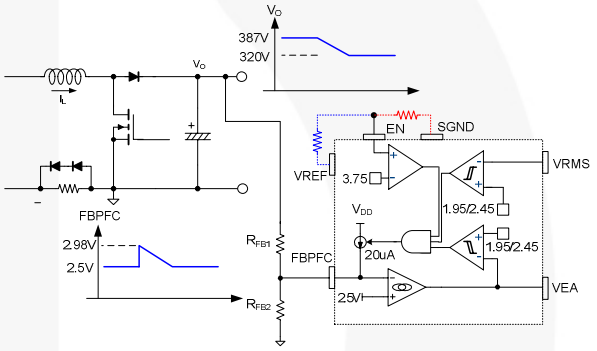


Figure 29. Block of Adjustable PFC Output

Brownout Protection

FAN6982 has a built-in internal brownout protection comparator monitoring the voltage of the VRMS pin. Once the VRMS pin voltage is lower than 1.05V, the PFC stage is shutdown to protect the system from over current. FAN6982 starts up the boost stage once the VRMS voltage increases above 1.9V.

TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards; the FAN6982 includes TriFault Detect technology. This feature monitors FBPFC for certain PFC fault conditions.

In the case of a feedback path failure, the output of the PFC could exceed operating limits. Should FBPFC go too low, or too high, or open; TriFault Detect senses the error and terminates the PFC output drive.

TriFault detect is an entirely internal circuit. It requires no external components to serve its protective function.

PFC Soft-Start Function

The FAN6982 PFC soft-start function is shown in Figure 30. When bulk voltage is under the 96% of setting voltage; V_{EA} clamps to 2.8V, the output current of multiplier cuts half, the rectifier line current is limited by current loop, and PFC output rise time increases.

When bulk voltage is over 96%, the clamping function is disabled, and the bulk voltage can be regulated by voltage error amplifier.

There have two advantages with PFC soft-start: one is the MOSFET experience of current is reduced, which can obtain more de-rating with MOSFET current level. The other one is to reduce the overshoot of PFC bulk voltage at the rising time because the charge current becomes small, the bulk voltage can not exceed to setting voltage easily.

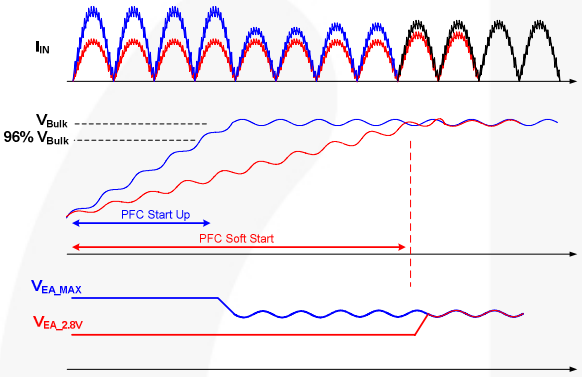


Figure 30. PFC Soft-Start

RDY Function

The FAN6982 RDY function, is shown in Figure 31, is controlled by voltage of FBPFC. If the voltage of FBPFC is over than 96% of 2.5V, the RDY pin is connected to SGND. If the FBPFC is under the 46% of 2.5V, the RDY appears open-drain situation. Usually the capacitor is parallel with the RDY pin to prevent the layout noise.

The PNP transistor can control the AHB LLC or dual-forward controller on the same side or the “op-to” to control the LLC controller on the other side.

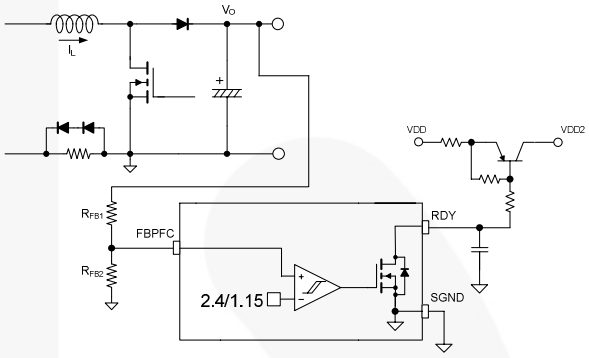
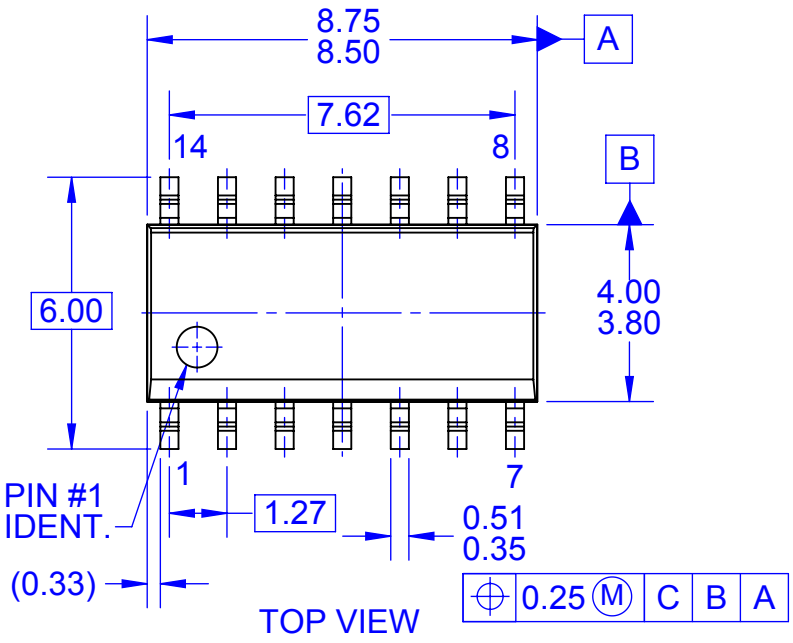
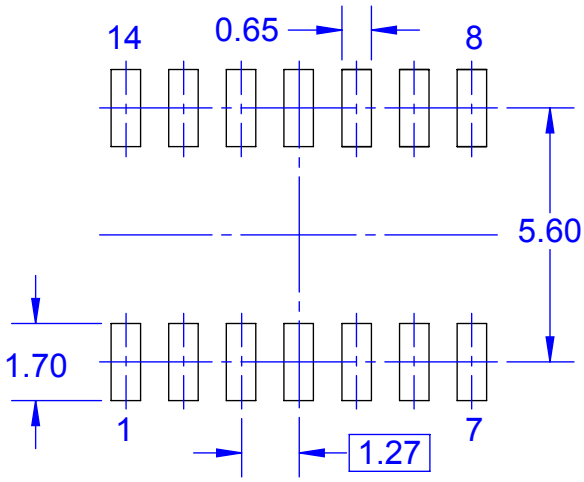


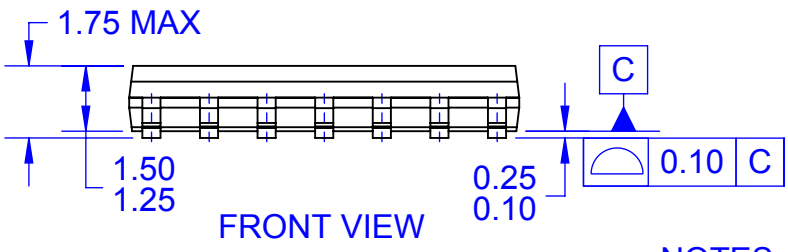
Figure 31. RDY Application Circuit



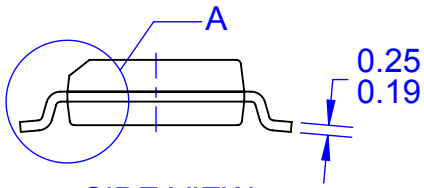
TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
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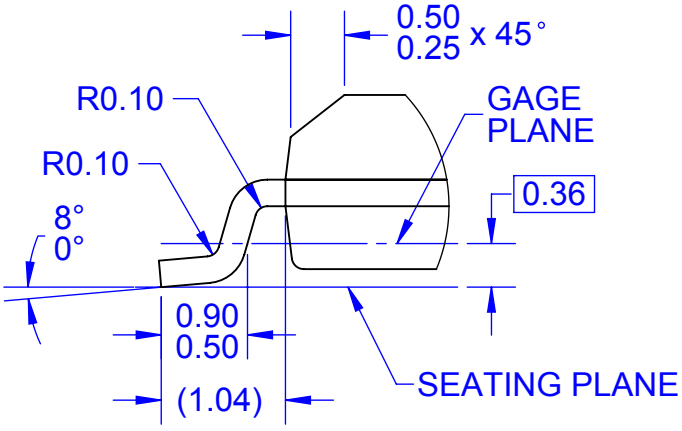
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14



DETAIL A
SCALE 16 : 1

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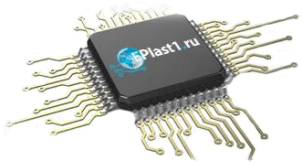

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