LTC4227-1/LTC4227-2/ LTC4227-3/LTC4227-4 Dual Ideal Diode and Single Hot Swap Controller

DESCRIPTION

Demonstration circuit 1625A is intended to demonstrate performance of the LTC4227-1/LTC4227-2/LTC4227-3/ LTC4227-4 dual ideal diode and Hot Swap™ controller. Each rail has an individual ideal diode. Ideal diode outputs are connected to the load through a single Hot Swap circuit.

The DC1625 allows verifying the LTC4227 Hot Swap and ideal diode functionality during individual supply ramp-up and ramp-down transients, during power supply switch-over, steady state, and overcurrent fault conditions.

Each DC1625A rail circuit is assembled to operate over the full operating voltage range of the LTC4227: 2.9V to 18V, with a 7.6A maximum current load.

The board's main components include the LTC4227 controller, two power MOSFETs controlled as ideal diodes and one power MOSFET controlled as a Hot Swap device, two jumpers for enabling the second ideal diode (D2ON_SEL) and Hot Swap controller (HS_ON), two LEDs to indicate power good ($\overline{PWRGD}$) and fault ($\overline{FAULT}$) conditions, seven banana jacks for connecting power supplies and load, many turrets and pads for observing circuit signals.

Table 1. DC1625A Assembly Options

VERSION	PART	OVERCURRENT FAULT	START-UP DELAY
DC1625A-A	LTC4227-1	LATCHOFF	100ms
DC1625A-B	LTC4227-2	RETRY	100ms
DC1625A-C	LTC4227-3	LATCHOFF	1.6ms
DC1625A-D	LTC4227-4	RETRY	1.6ms

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supplies						
V_{IN}	Input Supply Range		2.9		18.0	V
V_{INTVCC}	Internal Regulator Voltage		4.5	5	5.6	V
$V_{INTVCC(UVL)}$	Internal V_{CC} Undervoltage Lockout	$INTV_{CC}$ Rasing	2.1	2.2	2.3	V
Ideal Diode Control						
$\Delta V_{FWD(REG)}$	Forward Regulation Voltage ($V_{INn} - V_{SENSE}$)		10	25	40	mV
ΔV_{DGATE}	External N-Channel Gate Drive (V_{DGATEn} - V_{INn}) (V_{DGATEn} - V_{INn})	IN < 7V, ΔV_{FWD} = 0.1V IN = 7V to 18V, ΔV_{FWD} = 0.1V	5 10	7 12	14 14	V V
$I_{CPO(UP)}$	CPOn Pull-Up Current	CPO = IN = 2.9V CPO = IN = 18V	–60 –50	–95 –85	–120 –110	µA µA
$I_{DGATE(FPU)}$	DGATEn Fast Pull-Up Current	ΔV_{FWD} = 0.2V, ΔV_{DGATE} = 0V, CPO = 17V		–1.5		A
$I_{DGATE(FPD)}$	DGATEn Fast Pull-Down Current	ΔV_{FWD} = –0.2V, ΔV_{DGATE} = 5V		1.5		A
$I_{DGATE2(DN)}$	DGATE2 Off Pull-Down Current	$\overline{D2ON}$ = 2V, ΔV_{DGATE2} = 2.5V	40	100	200	µA
$t_{ON(DGATE)}$	DGATEn Turn-On Delay	ΔV_{FWD} = 0.2V, C_{GATE} = 10nF		0.25	0.5	µs
$t_{OFF(DGATE)}$	DGATEn Turn-Off Delay	ΔV_{FWD} = –0.2V, C_{GATE} = 10nF		0.2	0.5	µs
$t_{PLH(DGATE2)}$	$\overline{D2ON}$ Low to DGATE2 High			40	100	µs

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Hot Swap Control						
$\Delta V_{SENSE(CB)}$	Circuit Breaker Trip Sense Voltage ($V_{SENSE}^+ - V_{SENSE}^-$)		47.5	50	52.5	mV
$\Delta V_{SENSE(ACL)}$	Active Current Limit Sense Voltage ($V_{SENSE}^+ - V_{SENSE}^-$)		60	65	70	mV
ΔV_{HGATE}	External N-Channel Gate Drive ($V_{HGATE} - V_{OUT}$)	IN < 7V, I = 0, –1µA IN = 7V to 18V, I = 0, –1µA	4.8 10	7 12	14 14	V V
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, HGATE = 0V	–7	–10	–13	µA
$I_{HGATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, HGATE = OUT + 5V	150	300	500	µA
$I_{HGATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, HGATE = OUT + 5V	100	200	300	mA
Input/Output Pin						
$V_{SENSE}^+{}_{(UVL)}$	SENSE+ Undervoltage Lockout	SENSE+ Rising	1.75	1.9	2.05	V
$V_{ON(TH)}$	ON Pin Threshold Voltage	ON Rising	1.21	1.235	1.26	V
$V_{ON(RESET)}$	ON Pin Fault Reset Threshold Voltage	ON Falling	0.55	0.6	0.65	V
$V_{\overline{D2ON}(TH)}$	$\overline{D2ON}$ Pin Threshold Voltage	$\overline{D2ON}$ Rising	1.21	1.235	1.26	V
$V_{TMR(TH)}$	TMR Pin Threshold Voltage	TMR Rising TMR Falling	1.198 0.15	1.235 0.2	1.272 0.25	V V
$I_{TMR(UP)}$	TMR Pull-Up Current	TMR = 1V, In Fault Mode	–75	–100	–125	µA
$I_{TMR(DN)}$	TMR Pull-Down Current	TMR = 2V, No Faults	1.4	2	2.6	µA
$I_{TMR(RATIO)}$	TMR Current Ratio $I_{TMR(DN)}/ I_{TMR(UP)}$		1.4	2	2.7	%

OPERATING PRINCIPLES

The LTC4227 is intended to build a combination of two diode-OR circuits (for two rails) and a common single Hot Swap path for inrush current limiting and overcurrent protection.

The LTC4227 regulates the forward voltage drop across the MOSFETs to ensure smooth current transfer from one supply to other without oscillation. A fast turn-on reduces the load voltage droop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse current transients.

The Hot Swap fast acting current limit and internal timed circuit breaker protect circuit components when a short-circuit fault occurs.

The Hot Swap function on the LTC4227 controller has independent on/off control.

Each ideal diode MOSFET is activated from individual charge pump sources and the second ideal diode path has additional on/off control.

The LTC4227-1 and LTC4227-3 feature a latchoff circuit breaker, while the LTC4227-2 and the LTC4227-4 provide automatic retry after a fault.

QUICK START PROCEDURE

Demonstration circuit 1625A is easy to set up to evaluate the performance of the LTC4227. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

The DC1625A test includes independent test of the LTC4227 hot swapping functionality and ideal diode functionality.

HOT SWAP FUNCTIONALITY TEST

This test is performed with singe rail operation, when the rail output is provided through two series connected MOSFETs. One MOSFET functions as an ideal diode and other one as a Hot Swap circuit component.

The parameters of the three transients in different operation modes completely characterize the Hot Swap circuit performance. These actions are:

- A power-up without any additional load
- A current limit operation after successful power-up transient
- A power-up with shorted output

1. Initially, install the jumper heads in the following positions, if the first ideal diode is used in the test:

   JP1 EN_SEL in the position LOW

   JP2 D2ON_SEL in the position OFF

   JP3 ON_SEL in the position OFF

   If the second ideal diode is used:

   JP1 EN_SEL in the position LOW

   JP2 D2ON_SEL in the position ON

   JP3 ON_SEL in the position OFF

   Connect a 12V power supply to the board input turrets IN1 (or IN2) and GND. Do not load the output. Place the current probe on the 12V wire and voltage probes on the OUT turret.

   Provide ON signal at the ON pin by changing the JP3 jumper header position from OFF position to ON. Observe the transient. The output voltage rise time should be in the range of 12ms to 29ms. PWRGD green LED D3 (D5) must turn on. Turn off the rail using the ON jumper.

2. Connect a disabled electronic load to the OUT turret and GND. Turn on the rail and slowly increase the load current up to the circuit breaker threshold level. The current limit range should be from 7.8A to 8.9A.

   The DC1625A-A and DC1625-C circuit feature a latchoff circuit breaker, and DC1625A-B and the DC1625-D provide automatic retry after a fault.

   Turn off the rail with the ON_SEL jumper.

3. Initially short output with external wire. Place the current probe at this external wire. Turn on the rail and record the current shape. The maximum current should be in the 10.1A to 11.8A range.

QUICK START PROCEDURE

IDEAL DIODE FUNCTIONALITY TEST

In this test, both ideal diodes are active and small variations in the input voltage forces one ideal diode to be off and another ideal diode to be on.

Connect input turrets (IN1 and IN2) of each ideal diode with individual independent lab supply. Adjust each input voltage to 12V with maximum possible accuracy. Place one voltmeter between IN1 and IN2 turrets to measure the difference between two input voltages. Connect an electronic load to the output turret. Activate both rail and keep a load around 1A to 3A. Play with input voltage levels and be sure that when the difference between input voltages exceeds 40mV, only one rail feeds the load.

QUICK START PROCEDURE

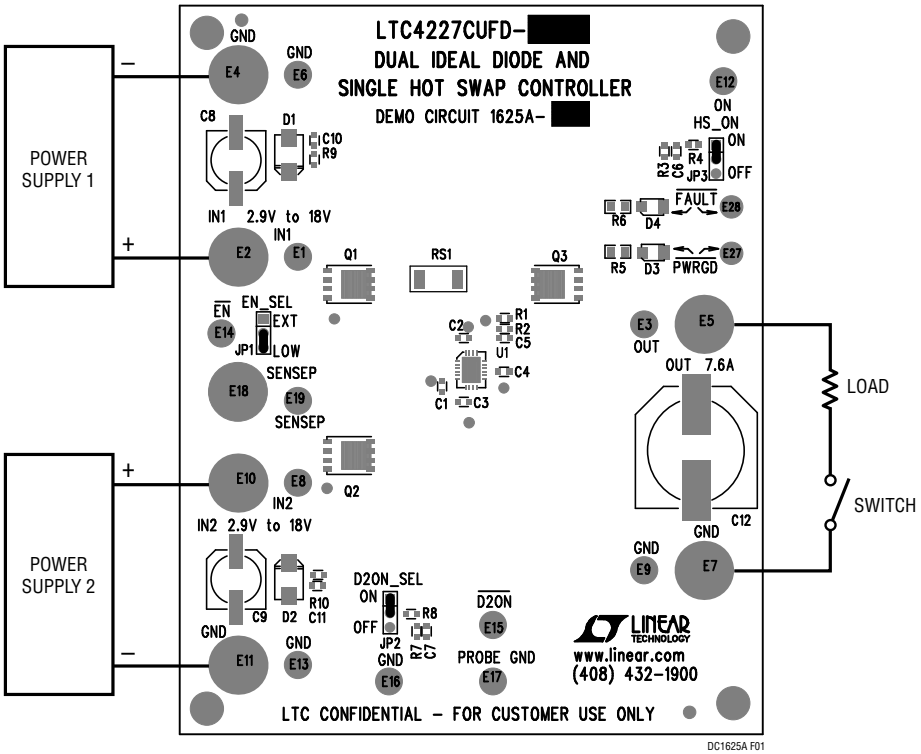
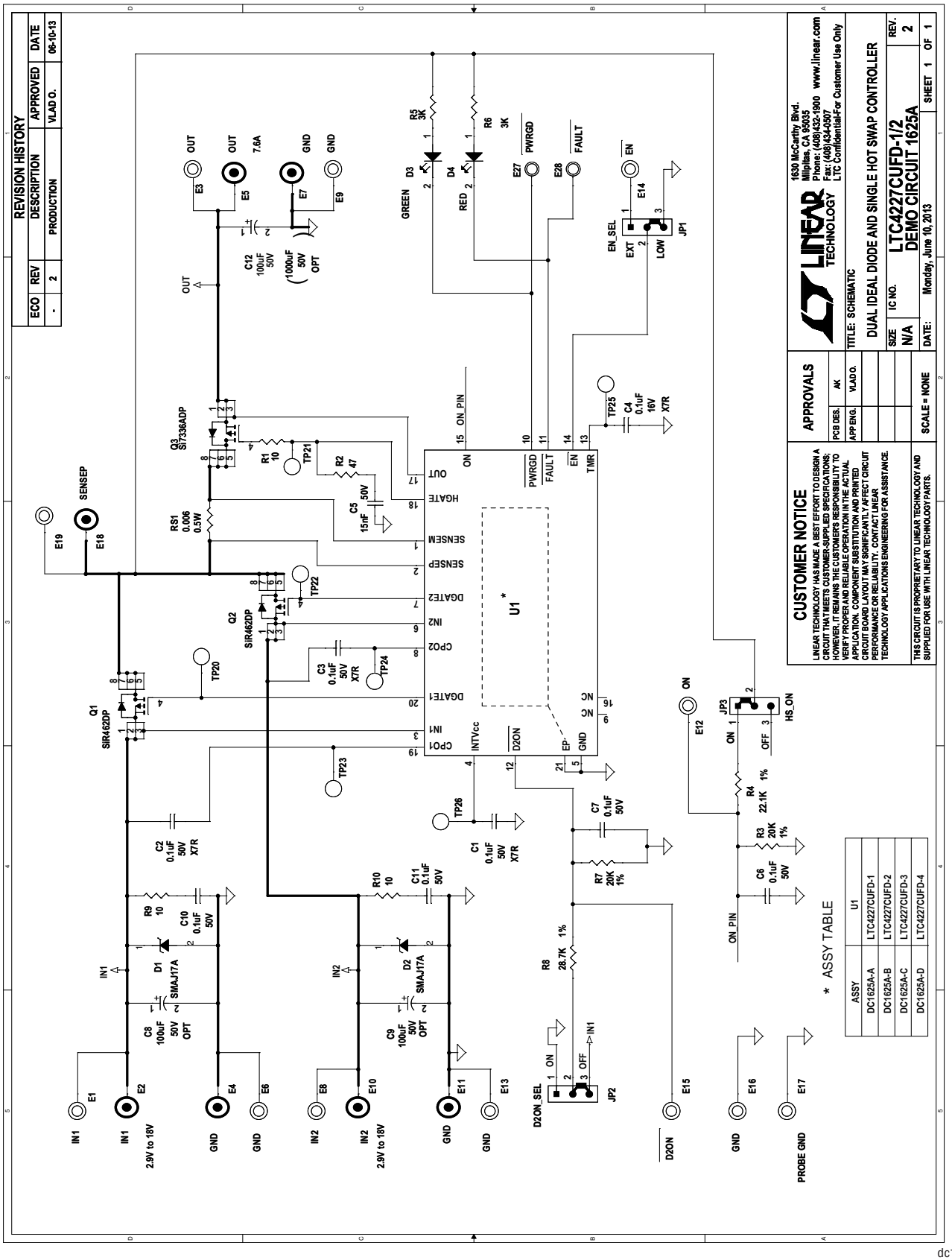


Figure 1. DC1625A Measurement Equipment Setup

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1625A General BOM				
1	8	C1, C2 ,C3, C4, C6, C7, C10, C11	CAP, X7R, 0.1µF, 50V, 0603	TDK, C1608X7R1H104K
2	1	C5	CAP, X7R, 15nF, 50V, 0603	AVX, 06035C153KAT
3	0	C8, C9 OPT	CAP, AL, EI, S/M 100µF, 50V	SUNCON, 50CE100BS
4	1	C12	CAP, AL, EI, S/M 100µF, 50V	SUNCON, 50CE100BS
5	0	C12 OPT	CAP, AL, EI, S/M 1000µF, 50V	NIC, NACEW102M50V16X17TR13F
6	2	D1, D2	DIODE, VOLTAGE SUPPRESSOR, SMA	DIODES, SMAJ17A-13-F
7	1	D3	LED, SMT GREEN	PANASONIC, LN1351CTR
8	1	D4	LED, SMT RED	PANASONIC, LN1261CTR
9	11	E1, E3, E6, E8, E9, E12 to E17	TURRET, TESTPOINT, 2501	MILL-MAX, 2501-2-00-80-00-00-07-0
10	7	E2, E4, E5, E7, E10, E11, E18	JACK BANANA	KEYSTONE, 575-4
11	2	E27, E28	TURRET, TESTPOINT, 2308	MILL-MAX, 2308-2-00-80-00-00-07-0
12	3	JP1, JP2, JP3	HEADERS, 3 PINS 2mm CTRS	SAMTEC TMM-103-02-L-S
13	3	XJP1, XJP2, XJP3	SHUNT, 2mm CTRS	SAMTEC 2SN-BK-G
14	2	Q1, Q2	MOSFET, N-CHANNEL, 30V	VISHAY, SiR462DP-T1-GE3
15	1	Q3	MOSFET, N-CHANNEL, 30V	VISHAY, Si7336ADP-T1-GE3
16	1	RS1	RES, CHIP, 0.006, 1/2W, 1%, 2010	KOA, TLR2HDBK6L00F75
17	3	R1, R9, R10	RES, CHIP, 10, 1%, 0603	VISHAY, CRCW060310R0FKEA
18	1	R2	RES, CHIP, 47, 1%, 0603	VISHAY, CRCW060347R0FKEA
19	2	R3, R7	RES, CHIP, 20k, 1%, 0603	VISHAY, CRCW060320K0FKEA
20	1	R4	RES, CHIP, 22.1k, 1%, 0603	VISHAY, CRCW060322K1FKEA
21	2	R5, R6	RES, CHIP, 3k, 1%, 0805	VISHAY, CRCW08053K00FKEA
22	1	R8	RES, CHIP, 28.7k, 1%, 0603	VISHAY, CRCW060328K7FKEA
23	4	STAND-OFF	STAND-OFF, NYLON 0.5"	KEYSTONE, 8833 (SNAP ON)
24	1		STENCIL	STENCIL 1625A
DC1625A-A				
1	1	DC1625A	General BOM	
2	1	U1	I.C. LTC4227CUFD-1, QFN20-4x5	LINEAR TECHNOLOGY, LTC4227CUFD-1
DC1625A-B				
1	1	DC1625A	General BOM	
2	1	U1	I.C. LTC4227CUFD-2, QFN20-4x5	LINEAR TECHNOLOGY, LTC4227CUFD-2
DC1625A-C				
1	1	DC1625A	General BOM	
2	1	U1	I.C. LTC4227CUFD-3, QFN20-4x5	LINEAR TECHNOLOGY, LTC4227CUFD-3
DC1625A-D				
1	1	DC1625A	General BOM	
2	1	U1	I.C. LTC4227CUFD-4, QFN20-4x5	LINEAR TECHNOLOGY, LTC4227CUFD-4

SCHEMATIC DIAGRAM



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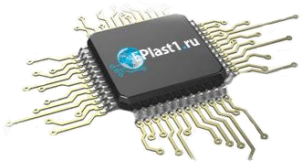

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