MCP7951X/MCP7952X

Battery-Backed SPI Real-Time Clock/Calendar

Device Selection Table

Part Number	SRAM (Bytes)	EEPROM (Kbits)	Unique ID
MCP79510	64	1	Blank
MCP79520	64	2	Blank
MCP79511	64	1	EUI-48™
MCP79521	64	2	EUI-48™
MCP79512	64	1	EUI-64™
MCP79522	64	2	EUI-64™

Timekeeping Features

- Real-Time Clock/Calendar (RTCC):
  - Hours, minutes, seconds, hundredth of seconds, day of week, date, month, year
  - Leap year compensated to 2399
  - 12/24-hour modes
- Oscillator for 32.768 kHz Crystals:
  - Optimized for 6-9 pF crystals
- On-Chip Digital Trimming/Calibration:
  - ±1 ppm resolution
  - ±259 ppm range
- Dual Programmable Alarms
- Clock Output Function with Selectable Frequency
- Power-Fail Timestamp:
  - Time logged on switchover to and from Battery mode

Low-Power Features

- Wide Voltage Range:
  - Operating voltage range of 1.8V to 3.6V
  - Backup voltage range of 1.3V to 3.6V
- Low Typical Timekeeping Current:
  - Operating from VCC: 1.2 µA at 3.0V
  - Operating from VBAT: 1.0 µA at 3.0V
- Automatic Switchover to Battery Backup

User Memory

- 64-Byte Battery-Backed SRAM
- 1 Kbit or 2 Kbit EEPROM:
  - Software write-protect
  - Page write up to 8 bytes
  - Endurance: one million erase/write cycles
- 128-Bit Protected EEPROM Area:
  - Robust write unlock sequence
  - EUI-48™ MAC address (MCP795X1)
  - EUI-64™ MAC address (MCP795X2)

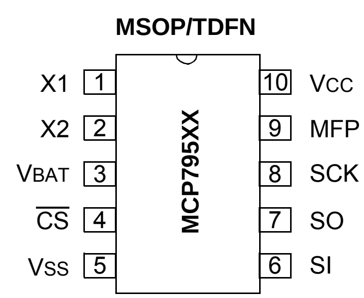
Operating Ranges

- SPI Serial Interface:
  - SPI clock rate up to 5 MHz
- Temperature Range:
  - Industrial (I): -40°C to +85°C

Packages

- 10-Lead MSOP and TDFN

Package Types (not to scale)



Note: MCP795XX is used in this document as a generic part number for the MCP7951X and MCP7952X devices.

Description

The MCP795XX Real-Time Clock/Calendar (RTCC) tracks time using internal counters for hours, minutes, seconds, hundredth of seconds, days, months, years and day of week. Alarms can be configured on all counters up to and including months. For usage and configuration, the MCP795XX supports SPI communications up to 5 MHz.

The MCP795XX is designed to operate using a 32.768 kHz tuning fork crystal with external crystal load capacitors. On-chip digital trimming can be used to adjust for frequency variance caused by crystal tolerance and temperature.

SRAM and timekeeping circuitry are powered from the backup supply when main power is lost, allowing the device to maintain accurate time and the SRAM contents. The times when the device switches over to the backup supply and when primary power returns are both logged by the power-fail timestamp.

The MCP795XX features 128 bits of EEPROM which is only writable after an unlock sequence, making it ideal for storing a unique ID or other critical information. The MCP795X1 and MCP795X2 are preprogrammed with EUI-48 and EUI-64 addresses, respectively. Custom programming is also available.

The MCP795XX has a shared pin for outputting a selectable frequency square wave or alarm signals.

FIGURE 1-1: TYPICAL APPLICATION SCHEMATIC

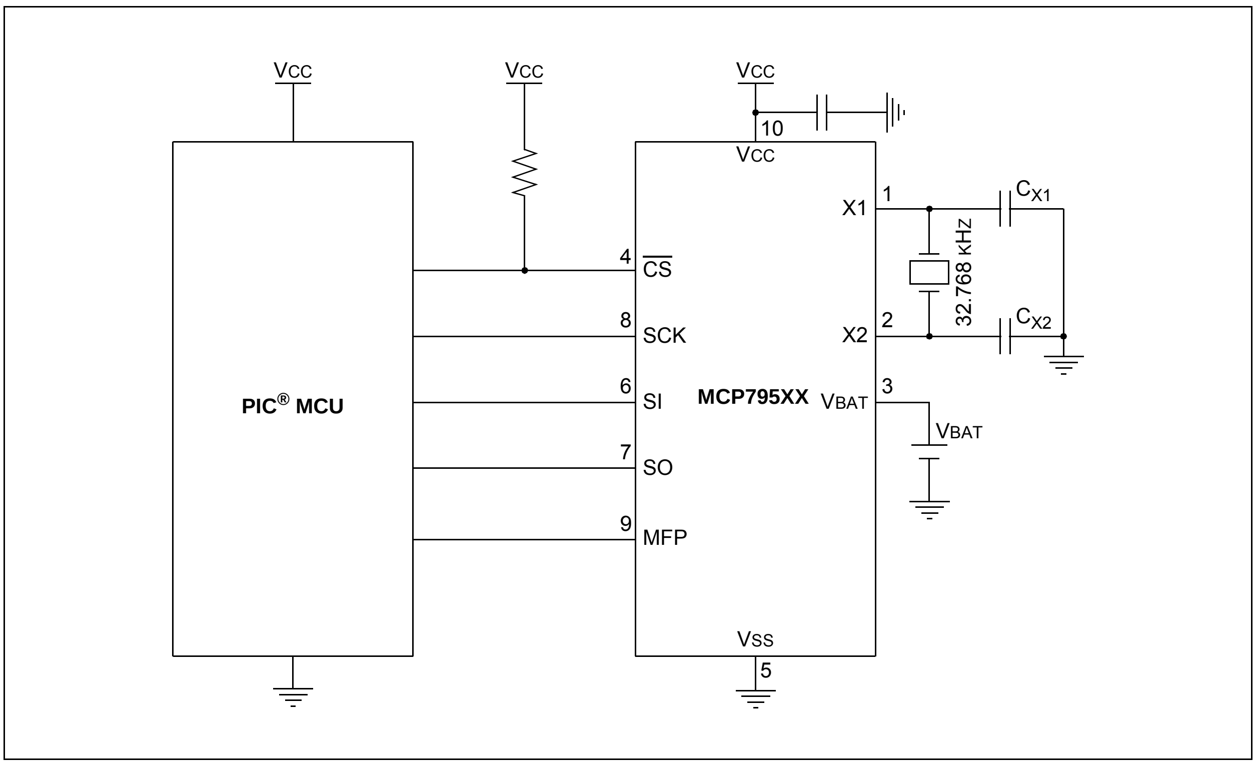
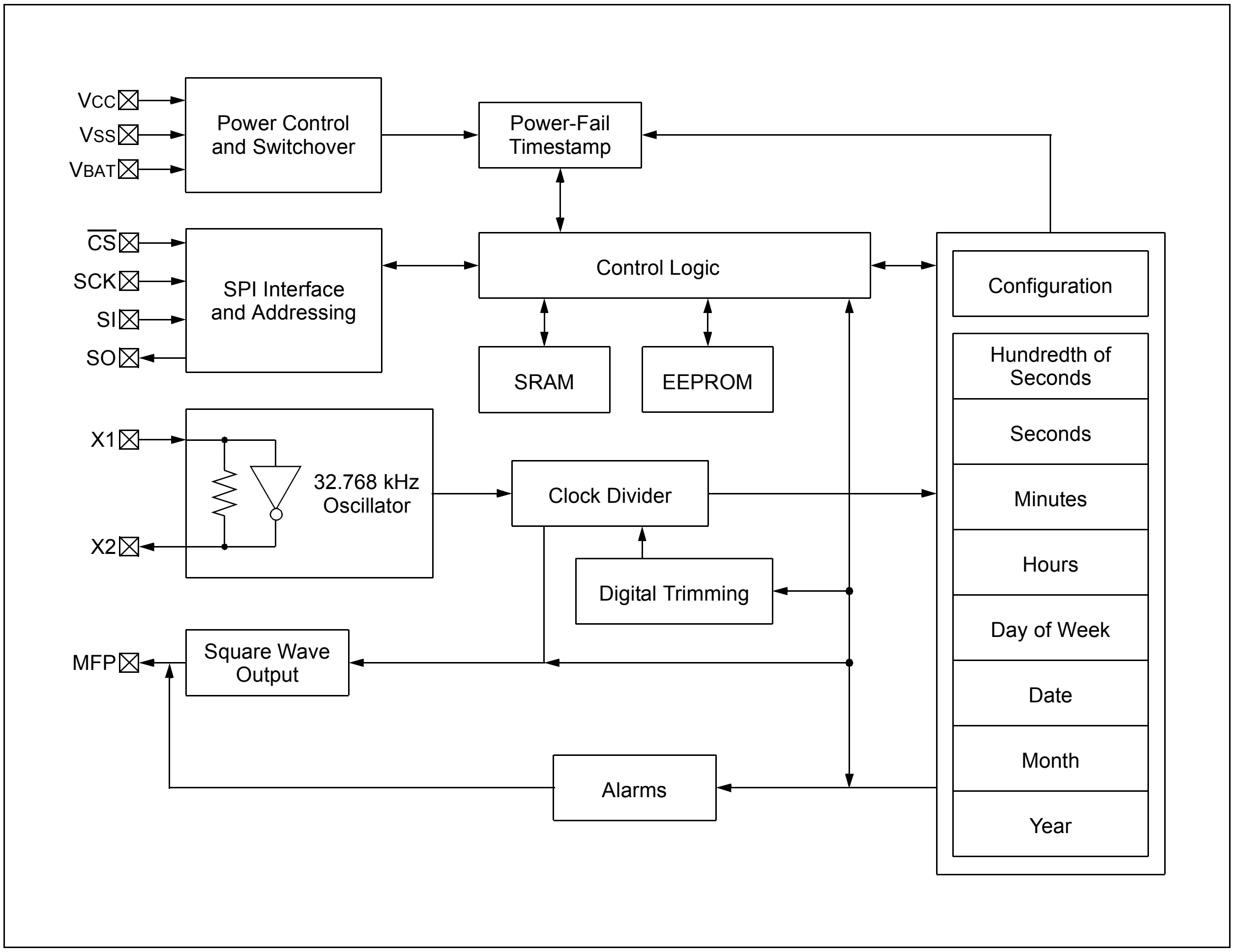


FIGURE 1-2: BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 6.5V

All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{CC}+1.0V

Storage temperature .... -65°C to +150°C

Ambient temperature under bias .... -40°C to +85°C

ESD protection on all pins .... 4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 3.6V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Test Conditions**
D1	V_{IH}	High-Level Input Voltage	0.7 V_{CC}	—	V_{CC} + 1	V	
D2	V_{IL}	Low-Level Input Voltage	-0.3	—	0.3V_{CC}	V	V_{CC} ≥ 2.5V
			-0.3	—	0.2V_{CC}		V_{CC} < 2.5V
D3	V_{OL}	Low-Level Output Voltage	—	—	0.4	V	I_{OL} = 2.1 mA, V_{CC} ≥ 2.5V
			—	—	0.2		I_{OL} = 1.0 mA, V_{CC} < 2.5V
D4	V_{OH}	High-Level Output Voltage	V_{CC} - 0.5	—	—	V	I_{OH} = -400 µA
D5	I_{LI}	Input Leakage Current	—	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
D6	I_{LO}	Output Leakage Current	—	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}
D7	C_{INT}	Pin Capacitance (all inputs and outputs)	—	—	7	pF	V_{CC} = 3.6V (**Note 1**) T_A = 25°C, f = 1 MHz
D8	C_{OSC}	Oscillator Pin Capacitance (X1, X2 pins)	—	3	—	pF	**Note 1**
D9	I_{CCEERD}	EEPROM Operating Current	—	—	3	mA	V_{CC} = 3.6V, F_{CLK} = 5 MHz SO = Open
	I_{CCEEWR}		—	—	5	mA	V_{CC} = 3.6V
D10	I_{CCREAD}	SRAM/RTCC Operating Current	—	—	3	mA	V_{CC} = 3.6V, F_{CLK} = 5 MHz SO = Open
	$I_{CCWRITE}$		—	—	3	mA	V_{CC} = 3.6V, F_{CLK} = 5 MHz
D11	I_{CCDAT}	Vcc Data Retention Current (oscillator off)	—	—	1	µA	V_{CC} = 3.6V

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

DC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 3.6V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Test Conditions**
D12	I_{CCT}	Timekeeping Current	—	—	1.2	µA	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}, (Note 1)
			—	1.2	1.8	µA	V_{CC} = 3.0V, $\overline{CS}$ = V_{CC}, (Note 1)
			—	—	2.6	µA	V_{CC} = 3.6V, $\overline{CS}$ = V_{CC}, (Note 1)
D13	V_{TRIP}	Power-Fail Switchover Voltage	1.3	1.5	1.7	V	
D14	V_{BAT}	Backup Supply Voltage Range	1.3	—	3.6	V	
D15	I_{BATT}	Timekeeping Backup Current	—	—	850	nA	V_{BAT} = 1.3V, V_{CC} = V_{SS} (Note 1)
			—	1000	1200	nA	V_{BAT} = 3.0V, V_{CC} = V_{SS} (Note 1)
			—	—	2300	nA	V_{BAT} = 3.6V, V_{CC} = V_{SS} (Note 1)
D16	I_{BATDAT}	V_{BAT} Data Retention Current (oscillator off)	—	—	850	nA	V_{BAT} = 3.6V, V_{CC} = V_{SS}

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 3.6V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	—	—	5	MHz	2.5V ≤ Vcc < 3.6V
			—	—	3	MHz	1.8V ≤ Vcc < 2.5V
2	TCSS	$\overline{CS}$ Setup Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
3	TCSH	$\overline{CS}$ Hold Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	—	ns	
5	TSU	Data Setup Time	20	—	—	ns	2.5V ≤ Vcc < 3.6V
			30	—	—	ns	1.8V ≤ Vcc < 2.5V
6	THD	Data Hold Time	40	—	—	ns	2.5V ≤ Vcc < 3.6V
			50	—	—	ns	1.8V ≤ Vcc < 2.5V
7	TR	SCK Rise Time	—	—	100	ns	**Note 1**
8	TF	SCK Fall Time	—	—	100	ns	**Note 1**
9	THI	Clock High Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
10	TLO	Clock Low Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
11	TCLD	Clock Delay Time	50	—	—	ns	
12	TCLE	Clock Enable Time	50	—	—	ns	
13	TV	Output Valid from Clock Low	—	—	100	ns	2.5V ≤ Vcc < 3.6V
			—	—	160	ns	1.8V ≤ Vcc < 2.5V
14	THO	Output Hold Time	0		—	ns	**Note 1**
15	TDIS	Output Disable Time	—	—	80	ns	2.5V ≤ Vcc < 3.6V (**Note 1**)
			—	—	160	ns	1.8V ≤ Vcc < 2.5V (**Note 1**)
16	TWC	Internal Write Cycle Time	—	—	5	ms	**Note 2**
17	TFVCC	VCC Fall Time	300	—	—	µs	**Note 1**
18	TRVCC	VCC Rise Time	0	—	—	µs	**Note 1**
19	FOSC	Oscillator Frequency	—	32.768	—	kHz	
20	TOSF	Oscillator Timeout Period	—	1	—	ms	**Note 1**
21		Endurance	1M	—	—	E/W cycles	Page Mode, 25°C VCC = 3.6V (**Note 1**)

Note 1: This parameter is not tested but ensured by characterization.

2: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

FIGURE 1-1: SERIAL INPUT TIMING

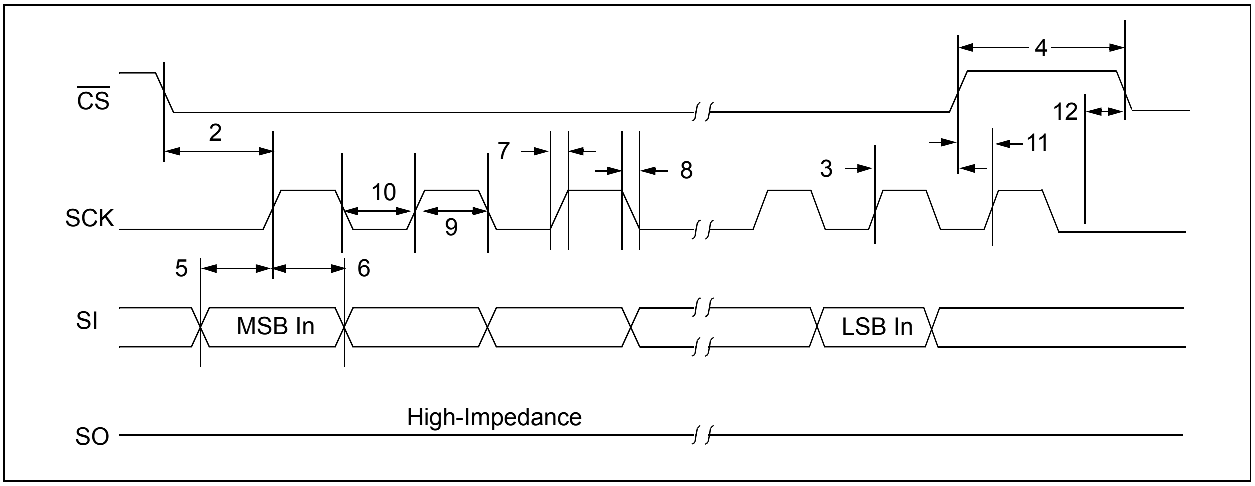


FIGURE 1-2: SERIAL OUTPUT TIMING

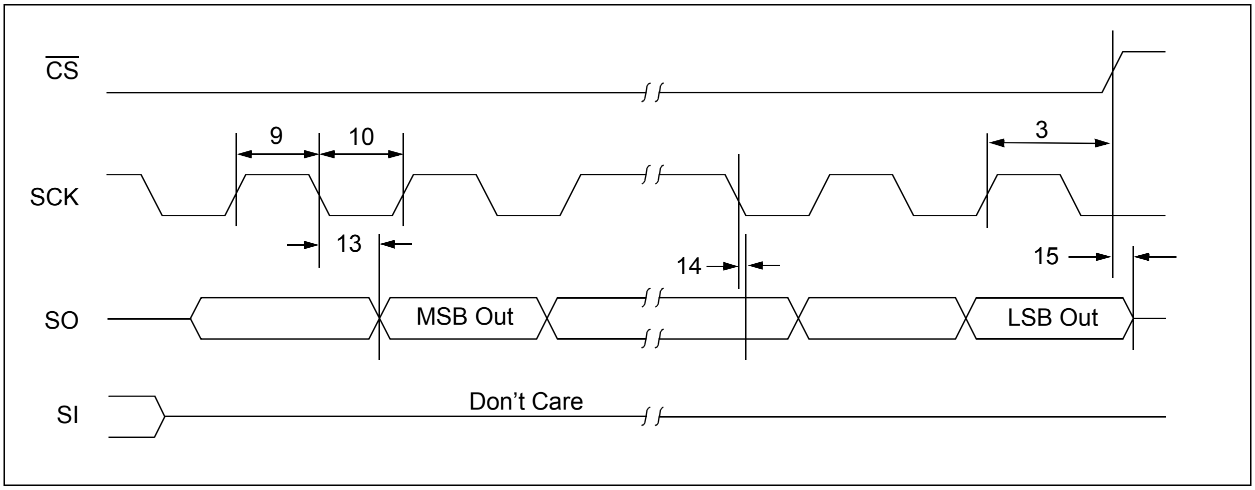
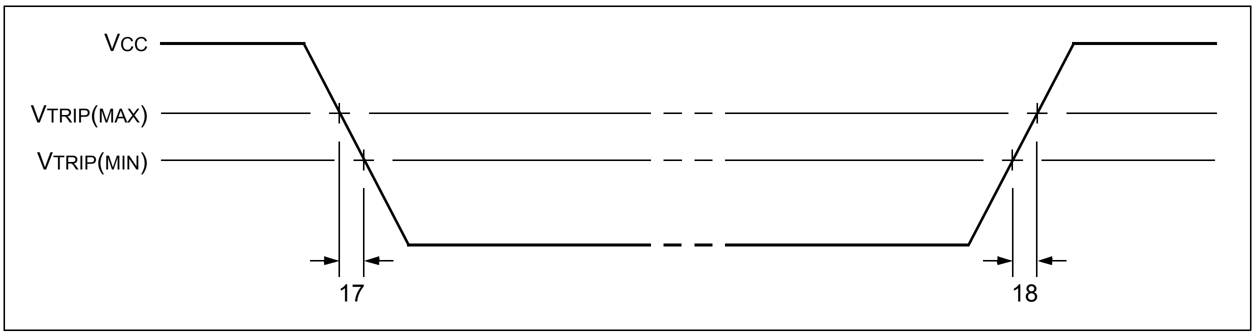


FIGURE 1-3: POWER SUPPLY TRANSITION TIMING



2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data represented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 2-1: TIMEKEEPING BACKUP CURRENT VS. BACKUP SUPPLY VOLTAGE

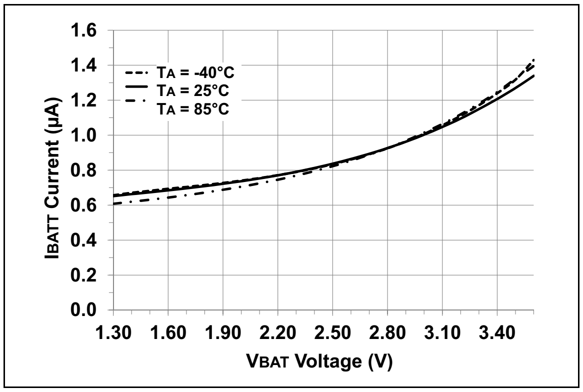
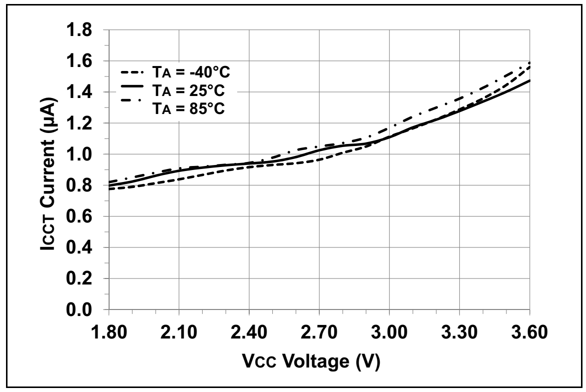


FIGURE 2-2: TIMEKEEPING CURRENT VS. SUPPLY VOLTAGE



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	10-Pin MSOP	10-Pin TDFN	Pin Function
X1	1	1	Quartz Crystal Input, External Oscillator Input
X2	2	2	Quartz Crystal Output
VBAT	3	3	Battery Backup Supply Input
$\overline{\text{CS}}$	4	4	Chip Select Input
VSS	5	5	Ground
SI	6	6	Serial Data Input
SO	7	7	Serial Data Output
SCK	8	8	Serial Clock Input
MFP	9	9	Multifunction Pin
VCC	10	10	Primary Power Supply

3.1 Oscillator Input/Output (X1, X2)

These pins are used as the connections for an external 32.768 kHz quartz crystal and load capacitors. X1 is the crystal oscillator input and X2 is the output. The MCP795XX is designed to allow for the use of external load capacitors in order to provide additional flexibility when choosing external crystals. The MCP795XX is optimized for crystals with a specified load capacitance of 6-9 pF.

X1 also serves as the external clock input when the MCP795XX is configured to use an external oscillator.

3.2 Backup Supply (VBAT)

This is the input for a backup supply to maintain the RTCC and SRAM registers during the time when VCC is unavailable.

Power should be applied to VCC before VBAT.

If the battery backup feature is not being used, the VBAT pin should be connected to VSS.

3.3 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device, whereas a high level deselects the device. A nonvolatile memory programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. When the device is deselected, SO goes into the high-impedance state, allowing multiple parts to share the same SPI bus. After power-up, a high-to-low transition on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

3.4 Serial Input (SI)

This pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.5 Serial Output (SO)

This pin is used to transfer data out of the MCP795XX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.6 Serial Clock (SCK)

This pin is used to synchronize the communication between a master and the MCP795XX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.7 Multifunction Pin (MFP)

The MFP pin is shared with the clock divider and the alarms. This pin requires an external pull-up to VCC or VBAT. The pin remains low until such time that the interrupt flag in the register is cleared by software. This pin has a maximum sink current of 10 mA.

4.0 SPI BUS OPERATION

The MCP795XX is designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

The MCP795XX contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low for the entire operation.

Table 4-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low.

TABLE 4-1: INSTRUCTION SET SUMMARY

Instruction Name	Instruction Format	Description
EEREAD	0000 0011	Read data from EEPROM array beginning at selected address
EEWRITE	0000 0010	Write data to EEPROM array beginning at selected address
EEWRDI	0000 0100	Reset the write enable latch (disable write operations)
EEWREN	0000 0110	Set the write enable latch (enable write operations)
SRREAD	0000 0101	Read STATUS register
SRWRITE	0000 0001	Write STATUS register
READ	0001 0011	Read data from RTCC/SRAM array beginning at selected address
WRITE	0001 0010	Write data to RTCC/SRAM array beginning at selected address
UNLOCK	0001 0100	Unlock the protected EEPROM block for a write operation
IDWRITE	0011 0010	Write data to the protected EEPROM block beginning at selected address
IDREAD	0011 0011	Read data from the protected EEPROM block beginning at the selected address
CLRRAM	0101 0100	Clear all SRAM data to '0'

5.0 FUNCTIONAL DESCRIPTION

The MCP795XX is a highly-integrated Real-Time Clock/Calendar (RTCC). Using an on-board, low-power oscillator, the current time is maintained in hundredths of seconds, seconds, minutes, hours, day of week, date, month, and year. The MCP795XX also features 64 bytes of general purpose SRAM, either 2 Kbits (MCP7952X) or 1 Kbit (MCP7951X) of EEPROM, and 16 bytes of protected EEPROM. Two alarm modules allow interrupts to be generated at specific times with flexible comparison options. Digital trimming can be used to compensate for inaccuracies inherent with crystals. Using the backup supply input and an integrated power switch, the MCP795XX will automatically switch to backup power when primary power is unavailable, allowing the current time and the SRAM contents to be maintained. The timestamp module captures the time when primary power is lost and when it is restored.

The RTCC configuration and STATUS registers are used to access all of the modules featured on the MCP795XX.

5.1 Memory Organization

The MCP795XX features four different blocks of memory: the RTCC registers, general purpose SRAM, 2 Kbit EEPROM (1 Kbit for the MCP7951X) with software write-protect, and protected EEPROM. The RTCC registers and SRAM share the same address space and are accessed through the `READ` and `WRITE` instructions. The EEPROM region is accessed using the `EEREAD` and `EEWRITE` instructions, and the protected EEPROM is accessed using the `IDREAD` and `IDWRITE` instructions. Unused locations are not accessible. The MCP795XX will not return valid data if the address is out of range, as shown in the shaded region of the memory maps in Figure 5-1 and Figure 5-2.

The RTCC registers are contained in addresses 0x00-0x1F. Table 5-1 shows the detailed RTCC register map. There are 64 bytes of user-accessible SRAM, located in the address range 0x20-0x5F. The SRAM is a separate block from the RTCC registers. All RTCC registers and SRAM locations are maintained while operating from backup power.

FIGURE 5-1: MEMORY MAP FOR MCP7951X

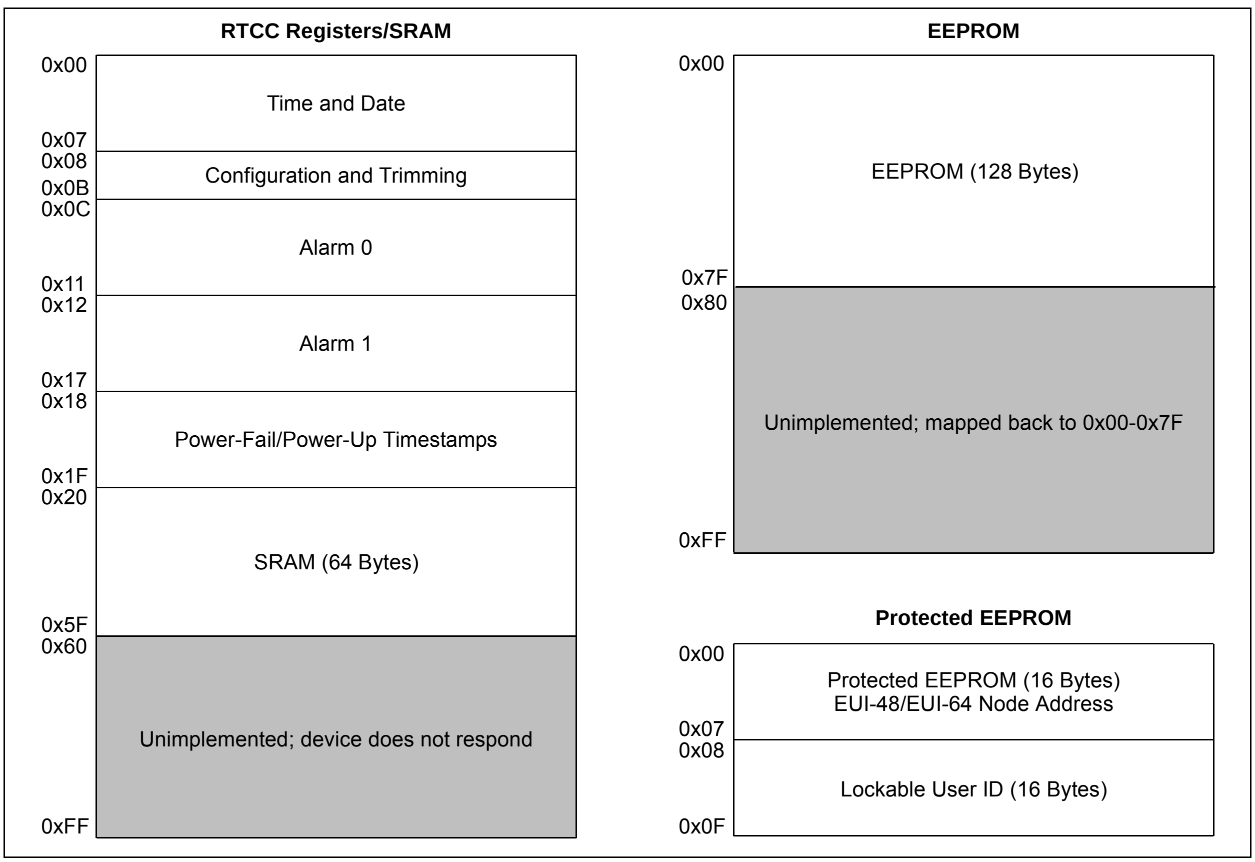


FIGURE 5-2: MEMORY MAP FOR MCP7952X

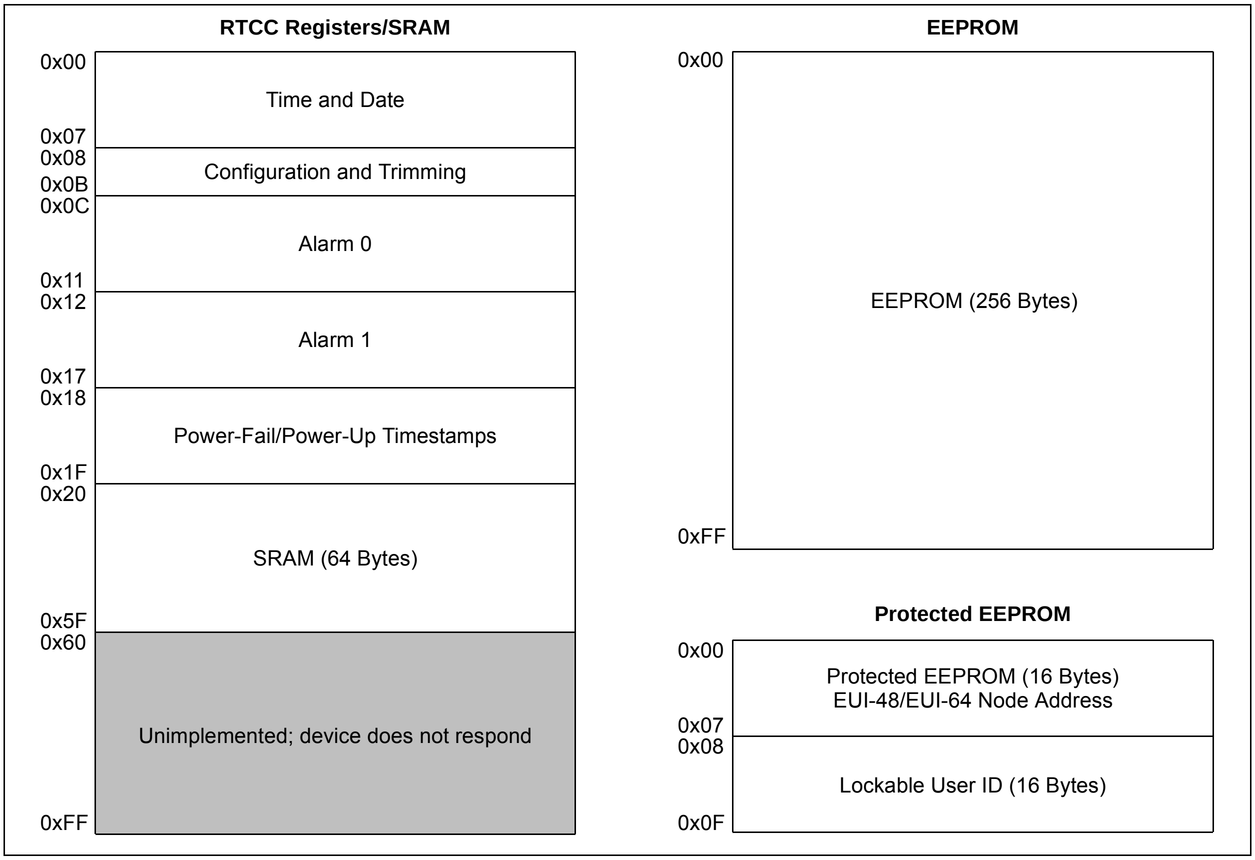


TABLE 5-1: DETAILED RTCC REGISTER MAP

Addr.	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Section 5.3 “Timekeeping”									
00h	RTCHSEC	HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
01h	RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
02h	RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
03h	RTCHOUR	TRIMSIGN	$12/\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
04h	RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
05h	RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
06h	RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
07h	RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
08h	CONTROL	—	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
09h	OSCTRIM	TRIMVAL7	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
Section 5.4 “Alarms”									
0Ch	ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
0Dh	ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
0Eh	ALM0HOUR	—	$12/\overline{24}$[2]	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
0Fh	ALM0WKDAY	ALM0PIN	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0
10h	ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
11h	ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
Section 5.4 “Alarms”									
12h	ALM1HSEC	HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
13h	ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
14h	ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
15h	ALM1HOUR	—	$12/\overline{24}$[2]	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
16h	ALM1WKDAY	ALM1PIN	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0
17h	ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
Section 5.7.1 “Power-Fail Timestamp”									
Power-Down Timestamp									
18h	PWRDNMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
19h	PWRDNHOUR	—	$12/\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Ah	PWRDNDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Bh	PWRDNMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
Power-Up Timestamp									
1Ch	PWRUPMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
1Dh	PWRUPHOUR	—	$12/\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Eh	PWRUPDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Fh	PWRUPMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0

Note 1: Grey areas are unimplemented.

2: The $12/\overline{24}$ bits in the ALMxHOUR registers are read-only and reflect the value of the $12/\overline{24}$ bit in the RTCHOUR register.

5.2 Oscillator Configurations

The MCP795XX can be operated in two different oscillator configurations: using an external crystal or using an external clock input.

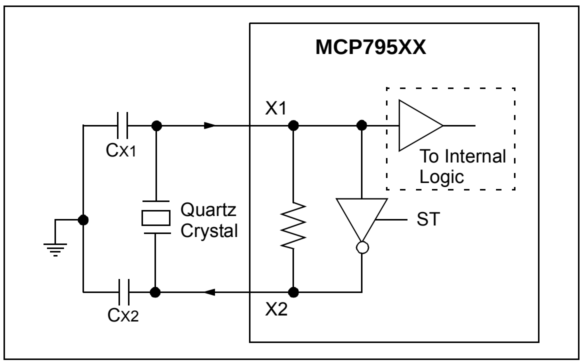
5.2.1 EXTERNAL CRYSTAL

The crystal oscillator circuit on the MCP795XX is designed to operate with a standard 32.768 kHz tuning fork crystal and matching external load capacitors.

By using external load capacitors, the MCP795XX allows for a wide selection of crystals. Suitable crystals have a load capacitance (C_L) of 6-9 pF. Crystals with a load capacitance of 12.5 pF are not recommended.

Figure 5-3 shows the pin connections when using an external crystal.

FIGURE 5-3: CRYSTAL OPERATION



Note 1: The ST bit must be set to enable the crystal oscillator circuit.

2: Always verify oscillator performance over the voltage and temperature range that is expected for the application.

5.2.1.1 Choosing Load Capacitors

C_L is the effective load capacitance as seen by the crystal, and includes the physical load capacitors, pin capacitance, and stray board capacitance. Equation 5-1 can be used to calculate C_L.

C_{X1} and C_{X2} are the external load capacitors. They must be chosen to match the selected crystal's specified load capacitance.

Note: If the load capacitance is not correctly matched to the chosen crystal's specified value, the crystal may give a frequency outside of the crystal manufacturer's specifications.

EQUATION 5-1: LOAD CAPACITANCE CALCULATION

$$C_L = \frac{C_{X1} \times C_{X2}}{C_{X1} + C_{X2}} + C_{STRAY}$$

Where:

C_L = Effective load capacitance

C_{X1} = Capacitor value on X1 + C_{OSC}

C_{X2} = Capacitor value on X2 + C_{OSC}

C_{STRAY} = PCB stray capacitance

5.2.1.2 Layout Considerations

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

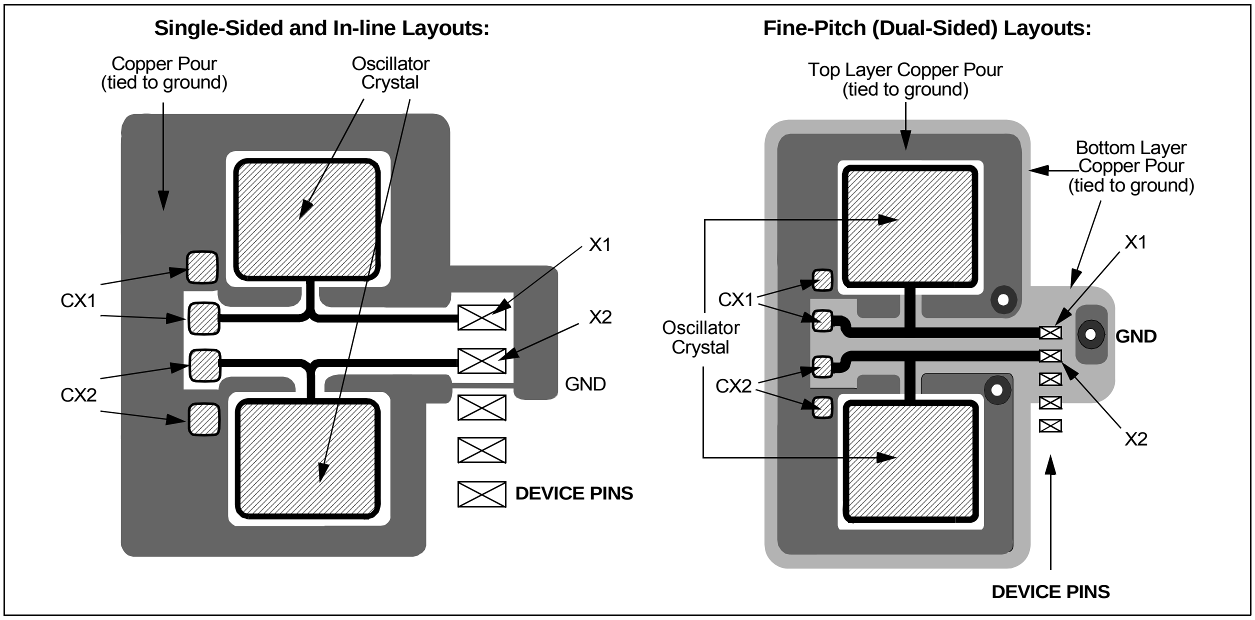
Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to V_{SS}. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 5-4. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- AN1365 – *"Recommended Usage of Microchip Serial RTCC Devices"* (DS00001365)
- AN1519 – *"Recommended Crystals for Microchip Stand-Alone Real-Time Clock Calendar Devices"* (DS00001519)

FIGURE 5-4: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

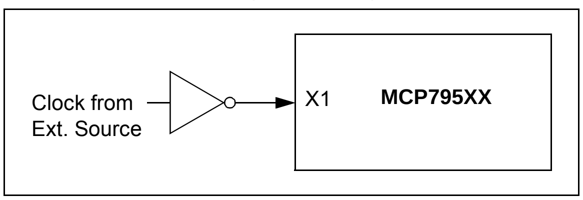


5.2.2 EXTERNAL CLOCK INPUT

A 32.768 kHz external clock source can be connected to the X1 pin (Figure 5-5). When using this configuration, the X2 pin should be left floating.

Note:	The EXTOSC bit must be set to enable an external clock source.

FIGURE 5-5: EXTERNAL CLOCK INPUT OPERATION



5.2.3 OSCILLATOR FAILURE STATUS

The MCP795XX features an oscillator failure flag, OSCRUN, that indicates whether or not the oscillator is running. The OSCRUN bit is automatically set after 32 oscillator cycles are detected. If no oscillator cycles are detected for more than TOSF, then the OSCRUN bit is automatically cleared (Figure 5-6). This can occur if the oscillator is stopped by clearing the ST bit or due to oscillator failure.

FIGURE 5-6: OSCILLATOR FAILURE STATUS TIMING DIAGRAM

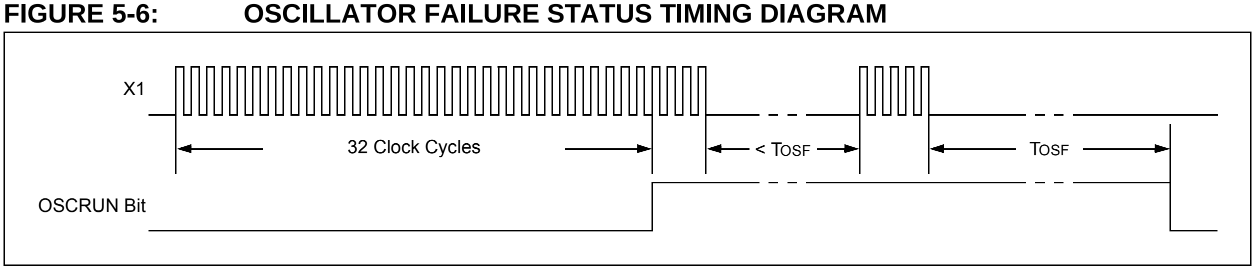


TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH OSCILLATOR CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	17
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	19
CONTROL	—	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	28

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by oscillator configuration.

5.3 Timekeeping

The MCP795XX maintains the current time and date using an external 32.768 kHz crystal or clock source. Separate registers are used for tracking hundredths of seconds, seconds, minutes, hours, day of week, date, month, and year. The MCP795XX automatically adjusts for months with less than 31 days and compensates for leap years from 2001 to 2399. The year is stored as a two-digit value.

Both 12-hour and 24-hour time formats are supported and are selected using the 12/$\overline{24}$ bit.

The day of week value counts from 1 to 7, increments at midnight, and the representation is user-defined (i.e., the MCP795XX does not require 1 to equal Sunday, etc.).

All time and date values are stored in the registers as binary-coded decimal (BCD) values. The MCP795XX will continue to maintain the time and date while operating off the backup supply.

When reading from the timekeeping registers, the registers are buffered to prevent errors due to rollover of counters. The following events cause the buffers to be updated:

- When a read is initiated from the RTCC registers (addresses 0x00 to 0x1F)
- During an RTCC register read operation, when the register address rolls over from 0x1F to 0x00

The timekeeping registers should be read in a single operation to utilize the on-board buffers and avoid rollover issues.

Note 1: Loading invalid values into the time and date registers will result in undefined operation.

2: To avoid rollover issues when loading new time and date values, the oscillator/clock input should be disabled by clearing the ST bit for External Crystal mode and the EXTOSC bit for External Clock Input mode. After waiting for the OSCRUN bit to clear, the new values can be loaded and the ST or EXTOSC bit can then be re-enabled.

5.3.1 DIGIT CARRY RULES

The following list explains which timer values cause a digit carry when there is a rollover:

- Time of day: from 11:59:59.99 PM to 12:00:00.00 AM (12-hour mode) or 23:59:59.99 to 00:00:00.00 (24-hour mode), with a carry to the Date and Weekday fields
- Date: carries to the Month field according to Table 5-3
- Weekday: from 7 to 1 with no carry
- Month: from 12/31 to 01/01 with a carry to the Year field
- Year: from 99 to 00 with no carry

TABLE 5-3: DAY TO MONTH ROLLOVER SCHEDULE

Month	Name	Maximum Date
01	January	31
02	February	28 or 29[(1)]
03	March	31
04	April	30
05	May	31
06	June	30
07	July	31
08	August	31
09	September	30
10	October	31
11	November	30
12	December	31

Note 1: 29 during leap years, otherwise 28.

5.3.2 GENERATING HUNDREDTH OF SECONDS

A special algorithm is required to accurately generate hundredth of seconds. The circuitry utilizes the 4.096 kHz clock signal and counts 41 clock pulses each for 24 increments of the hundredth of seconds count. The circuitry then counts 40 clock pulses for the next increment of the hundredth of second count. This results in every 25 hundredth of seconds increments equaling exactly 250 ms. Long term, the hundredth of seconds frequency will average the desired 100 Hz, while jitter is minimized short term.

EQUATION 5-2: HUNDREDTH OF SECONDS GENERATION

$$\frac{(41 \text{ clocks} \cdot 24 \text{ counts}) + (40 \text{ clocks} \cdot 1 \text{ count})}{4{,}096 \text{ Hz}} = 250 \text{ ms}$$

REGISTER 5-1: RTCHSEC: TIMEKEEPING HUNDREDTH OF SECONDS VALUE REGISTER (ADDRESS 0x00)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-4 **HSECTEN<3:0>:** Binary-Coded Decimal Value of Hundredth of Second’s Tens Digit
Contains a value from 0 to 9

bit 3-0 **HSECONE<3:0>:** Binary-Coded Decimal Value of Hundredth of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-2: RTCSEC: TIMEKEEPING SECONDS VALUE REGISTER (ADDRESS 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **ST:** Start Oscillator bit
1 = Oscillator enabled
0 = Oscillator disabled

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-3: RTCMIN: TIMEKEEPING MINUTES VALUE REGISTER (ADDRESS 0x02)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-4: RTCHOUR: TIMEKEEPING HOURS VALUE REGISTER (ADDRESS 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIMSIGN	$12/\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

If $12/\overline{24}$ = 1 (12-hour format):

bit 7 **TRIMSIGN:** Trim Sign bit
1 = Add clocks to correct for slow time
0 = Subtract clocks to correct for fast time

bit 6 **$12/\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour’s Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

If $12/\overline{24}$ = 0 (24-hour format):

bit 7 **TRIMSIGN:** Trim Sign bit
1 = Add clocks to correct for slow time
0 = Subtract clocks to correct for fast time

bit 6 **$12/\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour’s Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-5: RTCWKDAY: TIMEKEEPING WEEKDAY VALUE REGISTER (ADDRESS 0x04)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **OSCRUN:** Oscillator Status bit
1 = Oscillator is enabled and running
0 = Oscillator has stopped or has been disabled

bit 4 **PWRFAIL:** Power Failure Status bit[1,2]
1 = Primary power was lost and the power-fail timestamp registers have been loaded (must be cleared in software). Clearing this bit resets the power-fail timestamp registers to ‘0’.
0 = Primary power has not been lost

bit 3 **VBATEN:** External Battery Backup Supply (VBAT) Enable bit
1 = VBAT input is enabled
0 = VBAT input is disabled

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day of Week
Contains a value from 1 to 7. The representation is user-defined.

Note 1: The PWRFAIL bit must be cleared to log new timestamp data. This is to ensure previous timestamp data is not lost.

2: The PWRFAIL bit can be cleared by writing a ‘0’. Once cleared, the PWRFAIL bit cannot be written to a ‘1’ in software.

REGISTER 5-6: RTCDATE: TIMEKEEPING DATE VALUE REGISTER (ADDRESS 0x05)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date’s Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-7: RTCMTH: TIMEKEEPING MONTH VALUE REGISTER (ADDRESS 0x06)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **LPYR:** Leap Year bit
1 = Year is a leap year
0 = Year is not a leap year

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month’s Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-8: RTCYEAR: TIMEKEEPING YEAR VALUE REGISTER (ADDRESS 0x07)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-4 **YRTEN<3:0>:** Binary-Coded Decimal Value of Year’s Tens Digit
Contains a value from 0 to 9

bit 3-0 **YRONE<3:0>:** Binary-Coded Decimal Value of Year’s Ones Digit
Contains a value from 0 to 9

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMEKEEPING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCHSEC	HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0	17
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	17
RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	17
RTCHOUR	TRIMSIGN	12/$\overline{24}$	$\overline{\text{AM}}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	18
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	19
RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	19
RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	20
RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0	20

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used in timekeeping.

5.4 Alarms

The MCP795XX features two independent alarms. Each alarm can be used to either generate an interrupt at a specific time in the future, or to generate a periodic interrupt every second (Alarm 1 only), minute, hour, day, day of week, or month.

There is a separate interrupt flag, ALMxIF, for each alarm. The interrupt flags are set by hardware when the chosen alarm mask condition matches (Table 5-5 and Table 5-6). The interrupt flags must be cleared in software.

For alarm outputs to function, the Square Wave Output function must be disabled. Each of the two independent alarm signals are assigned to the MFP pin where either can pull it low. The pin will stay low until both the alarm flags are cleared. The alarm output to the MFP pin is available while operating from the backup supply.

All time and date values are stored in the registers as binary-coded decimal (BCD) values.

Note: Throughout this section, references to the register and bit names for the alarm modules are referred to generically by the use of 'x' in place of the specific module number. Thus, "ALMxSEC" might refer to the seconds register for Alarm 0 or Alarm 1.

TABLE 5-5: ALARM 0 MASKS

ALM0MSK<2:0>	Alarm 0 Asserts on Match of
`000`	Seconds
`001`	Minutes
`010`	Hours
`011`	Day of Week
`100`	Date
`101`	Reserved
`110`	Reserved
`111`	Seconds, Minutes, Hours, Day of Week, Date, and Month

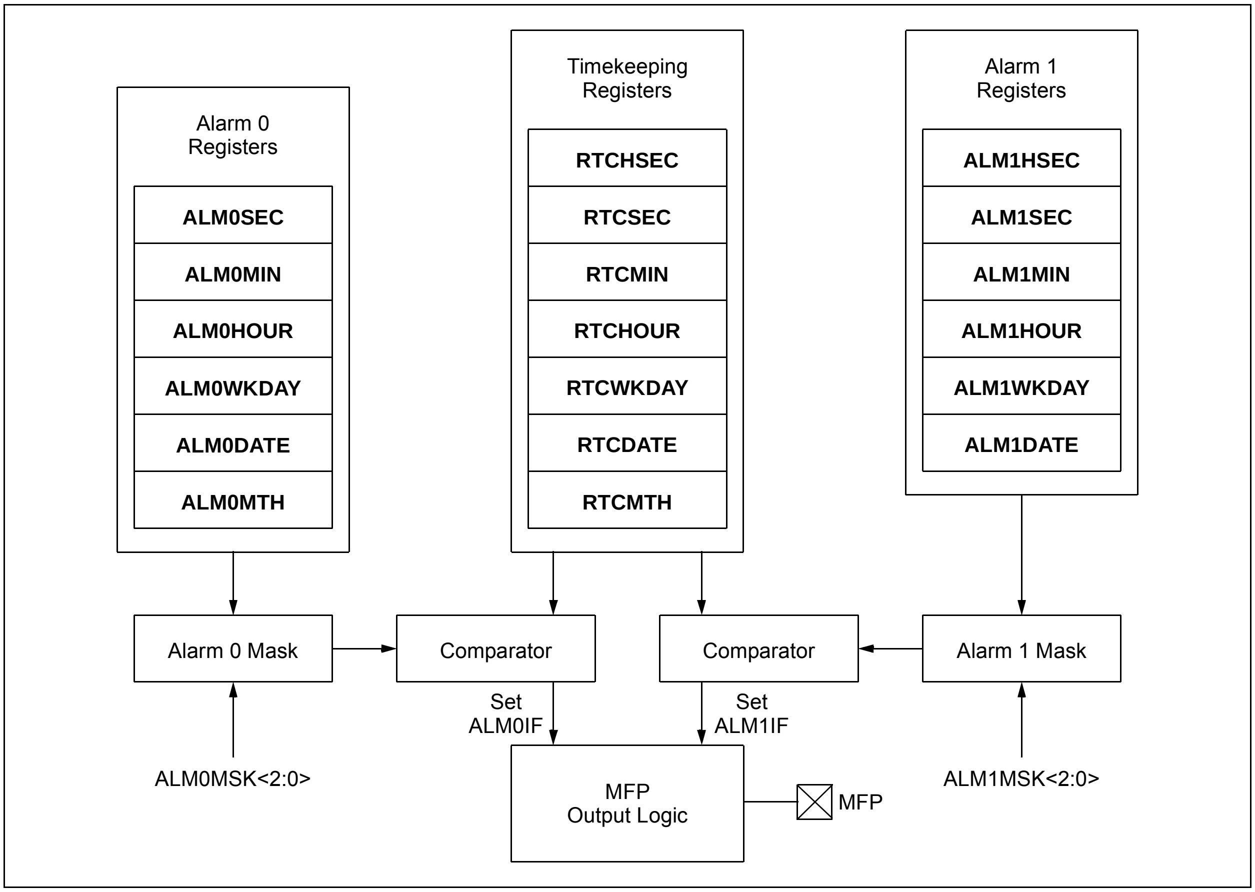
TABLE 5-6: ALARM 1 MASKS

ALM1MSK<2:0>	Alarm 1 Asserts on Match of
`000`	Seconds
`001`	Minutes
`010`	Hours
`011`	Day of Week
`100`	Date
`101`	Hundredth of Seconds
`110`	Reserved
`111`	Seconds, Minutes, Hours, Day of Week, and Date

Note 1: The alarm interrupt flags must be cleared by the user.

2: Loading invalid values into the alarm registers will result in undefined operation.

FIGURE 5-7: ALARM BLOCK DIAGRAM



5.4.1 CONFIGURING THE ALARM

In order to configure the alarm modules, the following steps need to be performed:

1. Load the timekeeping registers and enable the oscillator.
2. Configure the ALMxMSK<2:0> bits to select the desired alarm mask.
3. Ensure the ALMxIF flag is cleared.
4. Based on the selected alarm mask, load the alarm match value into the appropriate register(s).
5. Enable the alarm module by setting the ALMxEN bit.

REGISTER 5-9: ALM1HSEC: ALARM 1 HUNDREDTHS OF SECONDS VALUE REGISTER (ADDRESS 0x12)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-4 **HSECTEN<3:0>:** Binary-Coded Decimal Value of Hundredth of Second’s Tens Digit
Contains a value from 0 to 9

bit 3-0 **HSECONE<3:0>:** Binary-Coded Decimal Value of Hundredth of Second’s Ones Digit
Contains a value from 0 to 9

Note 1: Hundredth of seconds matching is only available on Alarm 1.

REGISTER 5-10: ALMxSEC: ALARM 0/1 SECONDS VALUE REGISTER (ADDRESSES 0x0C/0x13)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-11: ALMxMIN: ALARM 0/1 MINUTES VALUE REGISTER (ADDRESSES 0x0D/0x14)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-12: ALMxHOUR: ALARM 0/1 HOURS VALUE REGISTER (ADDRESSES 0x0E/0x15)

U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	$12/\overline{24}$	$\overline{\text{AM}}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

If $12/\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **$12/\overline{24}$:** 12 or 24 Hour Time Format bit[(1)]
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{\text{AM}}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour’s Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

If $12/\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **$12/\overline{24}$:** 12 or 24 Hour Time Format bit[(1)]
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour’s Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

Note 1: This bit is read-only and reflects the value of the $12/\overline{24}$ bit in the RTCHOUR register.

REGISTER 5-13: ALMxWKDAY: ALARM 0/1 WEEKDAY VALUE REGISTER (ADDRESSES 0x0F/0x16)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	ALMxMSK2	ALMxMSK1	ALMxMSK0	ALMxIF	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **ALMxMSK<2:0>:** Alarm Mask bits
000 = Seconds match
001 = Minutes match
010 = Hours match (logic takes into account 12-/24-hour operation)
011 = Day of week match
100 = Date match
101 = Hundredth of Seconds[1]
110 = Reserved; do not use
111 = Seconds, Minutes, Hour, Day of Week, Date and Month[2]

bit 3 **ALMxIF:** Alarm Interrupt Flag bit[3]
1 = Alarm match occurred (must be cleared in software)
0 = Alarm match did not occur

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits
Contains a value from 1 to 7. The representation is user-defined.

Note 1: Hundredth of seconds matching is available on Alarm 1 only. This setting is reserved on Alarm 0.
2: Month matching is available on Alarm 0 only.
3: The ALMxIF bit can be cleared by writing a ‘0’. Once cleared, the ALMxIF bit cannot be written to a ‘1’ in software.

REGISTER 5-14: ALMxDATE: ALARM 0/1 DATE VALUE REGISTER (ADDRESSES 0x10/0x17)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date’s Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-15: ALM0MTH: ALARM 0 MONTH VALUE REGISTER (ADDRESS 0x11)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month’s Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value from 0 to 9

Note 1: Month matching is only available on Alarm 0.

TABLE 5-7: SUMMARY OF REGISTERS ASSOCIATED WITH ALARMS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	23
ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	24
ALM0HOUR	—	$12/\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	24
ALM0WKDAY	ALM0PIN	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0	25
ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	25
ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	26
ALM1HSEC	HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0	23
ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	23
ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	24
ALM1HOUR	—	$12/\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	24
ALM1WKDAY	ALM1PIN	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0	25
ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	25
CONTROL	—	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	28

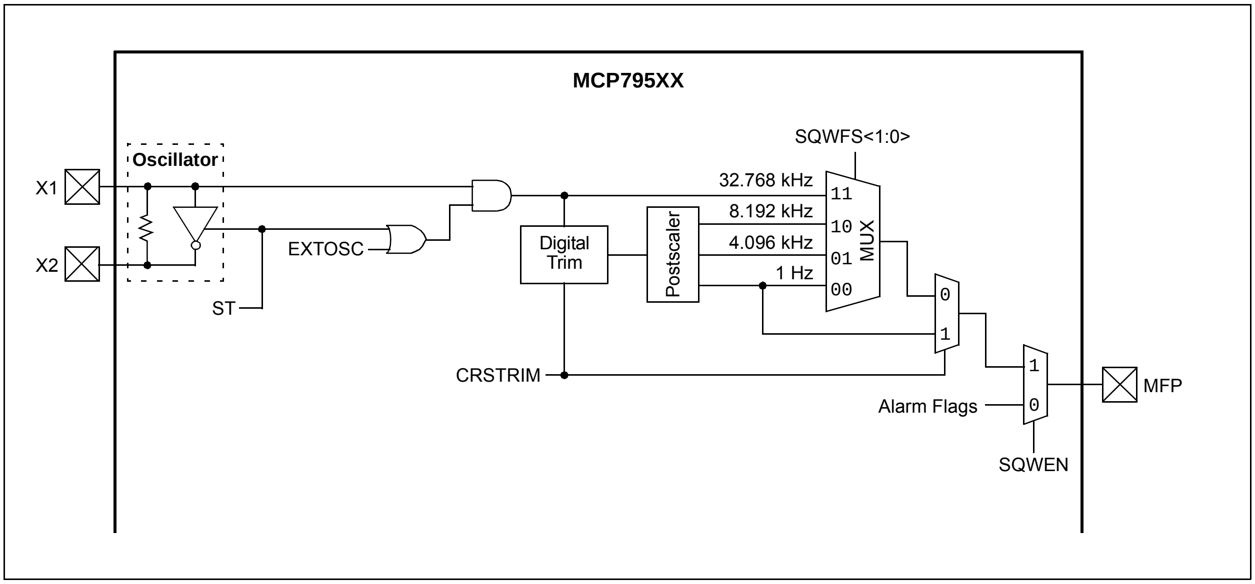
Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by alarms.

5.5 MFP Output

The MCP795XX features Square Wave Clock Output and Alarm Interrupt Output modes through the MFP pin. If the SQWEN bit is set, then MFP operates in Square Wave Clock Output mode.

The alarm outputs will remain active on the MFP pin while operating from the backup power supply. The Square Wave Clock Output is disabled while operating from the backup power supply.

FIGURE 5-8: CLKOUT OUTPUT BLOCK DIAGRAM



5.5.1 SQUARE WAVE OUTPUT MODE

The MCP795XX can be configured to generate a square wave clock signal on MFP. The input clock frequency, FOSC, is divided according to the SQWFS<1:0> bits as shown in Table 5-8.

The square wave output is not available when operating from the backup power supply, but the square wave settings can be retained by the backup power supply so that the square wave output can continue when VCC is restored.

Note:	All of the clock output rates are affected by digital trimming except for the 1:1 postscaler value (SQWFS<1:0> = 11).

TABLE 5-8: CLOCK OUTPUT RATES

SQWFS<1:0>	Postscaler	Nominal Frequency
00	1:32,768	1 Hz
01	1:8	4.096 kHz
10	1:4	8.192 kHz
11	1:1	32.768 kHz

Note 1: Nominal frequency assumes FOSC is 32.768 kHz.

REGISTER 5-16: CONTROL: RTCC CONTROL REGISTER (ADDRESS 0x08)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘1’

bit 6 **SQWEN:** Square Wave Output Enable bit
1 = Enable Square Wave Clock Output mode
0 = Disable Square Wave Clock Output mode

bit 5 **ALM1EN:** Alarm 1 Module Enable bit
1 = Alarm 1 enabled
0 = Alarm 1 disabled

bit 4 **ALM0EN:** Alarm 0 Module Enable bit
1 = Alarm 0 enabled
0 = Alarm 0 disabled

bit 3 **EXTOSC:** External Oscillator Input bit
1 = Enable X1 pin to be driven by external 32.768 kHz source
0 = Disable external 32.768 kHz input

bit 2 **CRSTRIM:** Coarse Trim Mode Enable bit
Coarse Trim mode results in the MCP795XX applying digital trimming every second.
1 = Enable Coarse Trim mode. If SQWEN = 1, CLKOUT will output trimmed 1 Hz[(1)] nominal clock signal.
0 = Disable Coarse Trim mode
See **Section 5.6 “Digital Trimming”** for details

bit 1-0 **SQWFS<1:0>:** Square Wave Clock Output Frequency Select bits
If SQWEN = 1 and CRSTRIM = 0:
Selects frequency of clock output on CLKOUT
00 = 1 Hz[(1)]
01 = 4.096 kHz[(1)]
10 = 8.192 kHz[(1)]
11 = 32.768 kHz
If SQWEN = 0 or CRSTRIM = 1:
Unused

Note 1: The 8.192 kHz, 4.096 kHz, and 1 Hz square wave clock output frequencies are affected by digital trimming.

TABLE 5-9: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK OUTPUT CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONTROL	—	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	28

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used in clock output configuration.

5.6 Digital Trimming

The MCP795XX features digital trimming to correct for inaccuracies of the external crystal or clock source, up to roughly ±259 ppm when CRSTRIM = `0`. In addition to compensating for intrinsic inaccuracies in the clock, this feature can also be used to correct for error due to temperature variation. This can enable the user to achieve high levels of accuracy across a wide temperature operating range.

Digital trimming consists of the MCP795XX periodically adding or subtracting clock cycles, resulting in small adjustments in the internal timing.

The adjustment occurs once per minute when CRSTRIM = `0`. The TRIMSIGN bit specifies whether to add cycles or to subtract them. The TRIMVAL<7:0> bits are used to specify by how many clock cycles to adjust. Each step in the TRIMVAL<7:0> value equates to adding or subtracting two clock pulses to or from the 32.768 kHz clock signal. This results in a correction of roughly 1.017 ppm per step when CRSTRIM = `0`. Setting TRIMVAL<7:0> to 0x00 disables digital trimming.

Digital trimming also occurs while operating off the backup supply.

REGISTER 5-17: OSCTRIM: OSCILLATOR DIGITAL TRIM REGISTER (ADDRESS 0x09)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIMVAL7	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-0 **TRIMVAL<7:0>:** Oscillator Trim Value bits

When CRSTRIM = `0`:
`11111111` = Add or subtract 510 clock cycles every minute
`11111110` = Add or subtract 508 clock cycles every minute
•
•
•
`00000010` = Add or subtract 4 clock cycles every minute
`00000001` = Add or subtract 2 clock cycles every minute
`00000000` = Disable digital trimming

When CRSTRIM = `1`:
`11111111` = Add or subtract 510 clock cycles every second
`11111110` = Add or subtract 508 clock cycles every second
•
•
•
`00000010` = Add or subtract 4 clock cycles every second
`00000001` = Add or subtract 2 clock cycles every second
`00000000` = Disable digital trimming

5.6.1 CALIBRATION

In order to perform calibration, the number of error clock pulses per minute must be found and the corresponding trim value must be loaded into TRIMVAL<7:0>.

There are two methods for determining the trim value. The first method involves measuring an output frequency directly and calculating the deviation from ideal. The second method involves observing the number of seconds gained or lost over a period of time.

Once the OSCTRIM register has been loaded, digital trimming will automatically occur every minute (CRSTRIM = 0).

5.6.1.1 Calibration by Measuring Frequency

To calibrate the MCP795XX by measuring the output frequency, perform the following steps:

1. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
2. Ensure TRIMVAL<7:0> is reset to 0x00.
3. Select an output frequency by setting SQWFS<1:0>.
4. Set SQWEN to enable the square wave output.
5. Measure the resulting output frequency using a calibrated measurement tool, such as a frequency counter.
6. Calculate the number of error clocks per minute (see Equation 5-3).

EQUATION 5-3: CALCULATING TRIM VALUE FROM MEASURED FREQUENCY

$$\text{TRIMVAL}\langle 7:0\rangle = \frac{(F_{IDEAL} - F_{MEAS}) \cdot \frac{32768}{F_{IDEAL}} \cdot 60}{2}$$

Where:

F_{IDEAL} = Ideal frequency based on SQWFS<1:0>

F_{MEAS} = Measured frequency

- If the number of error clocks per minute is negative, then the oscillator is *faster* than ideal and the TRIMSIGN bit must be cleared.
- If the number of error clocks per minute is positive, then the oscillator is *slower* than ideal and the TRIMSIGN bit must be set.

7. Load the correct value into TRIMVAL<7:0>.

Note: Using a lower output frequency and/or averaging the measured frequency over a number of clock pulses will reduce the effects of jitter and improve accuracy.

5.6.1.2 Calibration by Observing Time Deviation

To calibrate the MCP795XX by observing the deviation over time, perform the following steps:

1. Ensure TRIMVAL<7:0> is reset to 0x00.
2. Load the timekeeping registers to synchronize the MCP795XX with a known-accurate reference time.
3. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
4. Observe how many seconds are gained or lost over a period of time (larger time periods offer more accuracy).
5. Calculate the PPM deviation (see Equation 5-4).

EQUATION 5-4: CALCULATING ERROR PPM

$$PPM = \frac{SecDeviation}{ExpectedSec} \cdot 1000000$$

Where:

$ExpectedSec$ = Number of seconds in chosen period

$SecDeviation$ = Number of seconds gained or lost

- If the MCP795XX has gained time relative to the reference clock, then the oscillator is *faster* than ideal and the TRIMSIGN bit must be cleared.
- If the MCP795XX has lost time relative to the reference clock, then the oscillator is *slower* than ideal and the TRIMSIGN bit must be set.

6. Calculate the trim value (see Equation 5-5).

EQUATION 5-5: CALCULATING TRIM VALUE FROM ERROR PPM

$$\text{TRIMVAL}\langle 7:0\rangle = \frac{PPM \cdot 32768 \cdot 60}{1000000 \cdot 2}$$

7. Load the correct value into TRIMVAL<7:0>.

Note 1: Choosing a longer time period for observing deviation will improve accuracy.

2: Large temperature variations during the observation period can skew results.

5.6.2 COARSE TRIM MODE

When CRSTRIM = 1, Coarse Trim mode is enabled. While in this mode, the MCP795XX will apply trimming every second. If SQWEN is set, the CLKOUT pin will output a trimmed 1 Hz nominal clock signal.

Because trimming is applied every second rather than every minute, each step of the TRIMVAL<7:0> value has a larger effect on the resulting time deviation and output clock frequency.

By monitoring the CLKOUT output frequency while in this mode, the user can easily observe the TRIMVAL<7:0> value affecting the clock timing.

> **Note 1:** The 1 Hz Coarse Trim mode square wave output is not available while operating from the backup power supply.
>
> **2:** With Coarse Trim mode enabled, the TRIMVAL<7:0> value has a larger effect on timing. Leaving the mode enabled during normal operation will likely result in inaccurate time.

TABLE 5-10: SUMMARY OF REGISTERS ASSOCIATED WITH DIGITAL TRIMMING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCHOUR	TRIMSIGN	12/$\overline{24}$	$\overline{\text{AM}}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	18
CONTROL	—	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	28
OSCTRIM	TRIMVAL7	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0	29

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by digital trimming.l

5.7 Battery Backup

The MCP795XX features a backup power supply input (VBAT) that can be used to provide power to the time-keeping circuitry, RTCC registers, and SRAM while primary power is unavailable. The MCP795XX will automatically switch to backup power when VCC falls below VTRIP, and back to VCC when it is above VTRIP.

The VBATEN bit must be set to enable the VBAT input.

The following functionality is maintained while operating on backup power:

- Timekeeping
- Alarms
- Alarm Outputs
- Digital Trimming
- RTCC Register and SRAM Contents

The following features are not available while operating on backup power:

- SPI Communication
- Watchdog Timer
- Event Detect
- Square Wave Clock Output

Note:	If VCC is lost while VBAT voltage is applied, but where VBATEN is not set to '1', it could result in undetermined behavior. If a backup supply is not used, the VBAT pin should be connected to VSS.

5.7.1 POWER-FAIL TIMESTAMP

The MCP795XX includes a power-fail timestamp module that stores the minutes, hours, date, and month when primary power is lost and when it is restored (Figure 5-9). The PWRFAIL bit is also set to indicate that a power failure occurred.

Note:	Throughout this section, references to the register and bit names for the Power-Fail Timestamp module are referred to generically by the use of 'x' in place of the specific module name. Thus, "PWRxxMIN" might refer to the minutes register for power-down or power-up.

To utilize the power-fail timestamp feature, a backup power supply must be available with the VBAT input enabled, and the oscillator should also be running to ensure accurate functionality.

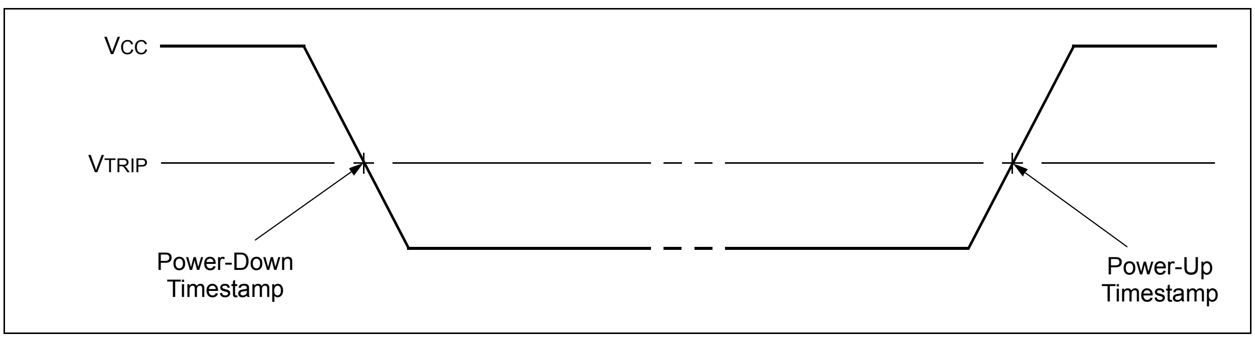
Note 1:	The PWRFAIL bit must be cleared to log new timestamp data. This is to ensure previous timestamp data is not lost.
2:	Clearing the PWRFAIL bit will clear all timestamp registers.

5.7.1.1 Configuring Battery Backup

In order to configure the battery backup feature, the following steps need to be performed:

1. Enable the oscillator.
2. Wait for the OSCRUN bit to be set, indicating the oscillator has started.
3. Enable battery backup by setting the VBATEN bit.

FIGURE 5-9: POWER-FAIL TIMESTAMP TIMING



REGISTER 5-18: PWRxxMIN: POWER-DOWN/POWER-UP TIMESTAMP MINUTES VALUE REGISTER (ADDRESSES 0x18/0x1C)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-19: PWRxxHOUR: POWER-DOWN/POWER-UP TIMESTAMP HOURS VALUE REGISTER (ADDRESSES 0x19/0x1D)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{\text{AM}}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{\text{AM}}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour’s Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour’s Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-20: PWRxxDATE: POWER-DOWN/POWER-UP TIMESTAMP DATE VALUE REGISTER (ADDRESSES 0x1A/0x1E)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date’s Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-21: PWRxxMTH: POWER-DOWN/POWER-UP TIMESTAMP MONTH VALUE REGISTER (ADDRESSES 0x1B/0x1F)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7-5 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits
Contains a value from 1 to 7. The representation is user-defined.

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value from 0 to 9

TABLE 5-11: SUMMARY OF REGISTERS ASSOCIATED WITH BATTERY BACKUP

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	19
PWRDNMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	33
PWRDNHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	33
PWRDNDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	34
PWRDNMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	34
PWRUPMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	33
PWRUPHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	33
PWRUPDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	34
PWRUPMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	34

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used with battery backup.

6.0 ON-BOARD MEMORY

The MCP7952X has 2 Kbits (256 bytes) of EEPROM, while the MCP7951X has 1 Kbit (128 bytes) of EEPROM. In addition, the devices have 16 bytes of protected EEPROM for storing crucial information, and 64 bytes of SRAM for general purpose usage. The SRAM is retained when the primary power supply is removed if a backup supply is present and enabled. Since the EEPROM is nonvolatile, it does not require a supply for data retention.

Although the SRAM is a separate block from the RTCC registers, they are accessed using the same instructions, `READ` and `WRITE`. The EEPROM is accessed using the `EEREAD` and `EEWRITE` instructions, and the protected EEPROM is accessed using the `IDREAD` and `IDWRITE` instructions. RTCC and SRAM can be accessed for reads or writes immediately after starting an EEPROM write cycle.

6.1 SRAM/RTCC Registers

The RTCC registers are located at addresses 0x00 to 0x1F, and the SRAM is located at addresses 0x20 to 0x5F. The SRAM can be accessed while the RTCC registers are being internally updated. The SRAM is not initialized by a Power-on Reset (POR).

Neither the RTCC registers nor the SRAM can be accessed when the device is operating off the backup power supply.

6.1.1 SRAM/RTCC REGISTER WRITE SEQUENCE

The device is selected by pulling $\overline{CS}$ low. The 8-bit `WRITE` instruction is transmitted to the MCP795XX followed by an 8-bit address. Next, the data to be written is transmitted.

There is no limit to the number of bytes that can be written in a single command. However, because the RTCC registers and SRAM are separate blocks, writing past the end of each block will cause the internal Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

Each data byte is latched into memory as it is received. Once all data bytes have been transmitted, $\overline{CS}$ is driven high to end the operation (Figure 6-1).

6.1.2 SRAM/RTCC REGISTER READ SEQUENCE

The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the MCP795XX followed by an 8-bit address.

After the `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. The Address Pointer allows the entire memory block to be serially read during one operation. The read operation is terminated by driving $\overline{CS}$ high (Figure 6-2).

Because the RTCC registers and SRAM are separate blocks, reading past the end of each block will cause the Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

FIGURE 6-1: SRAM/RTCC WRITE SEQUENCE

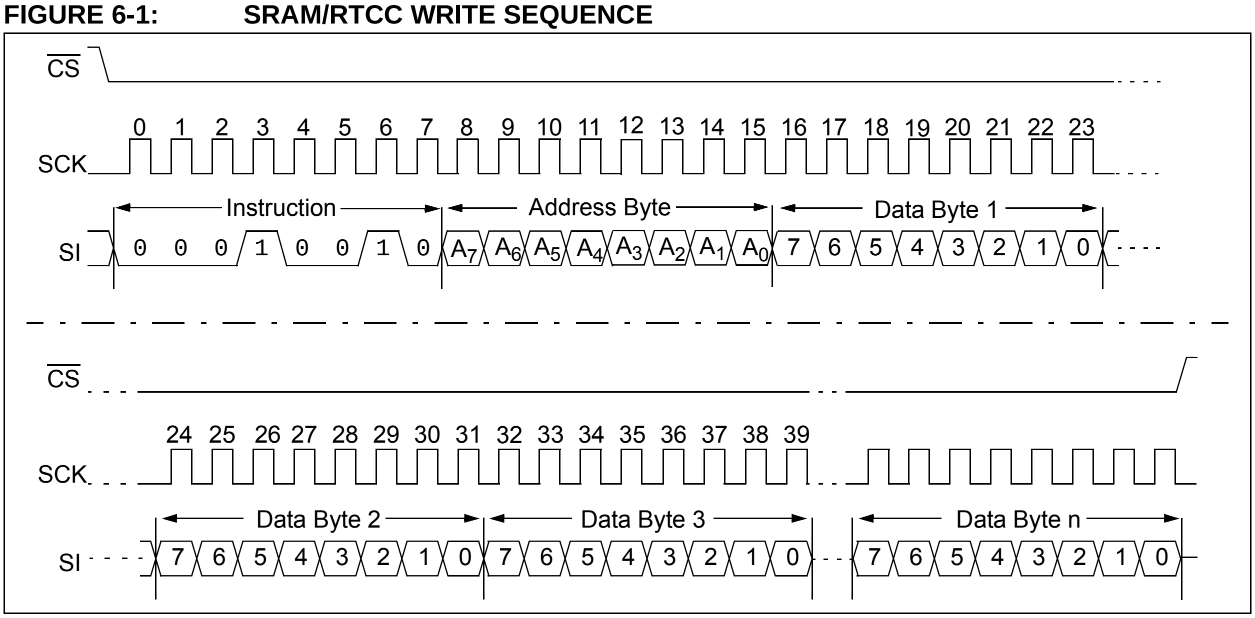
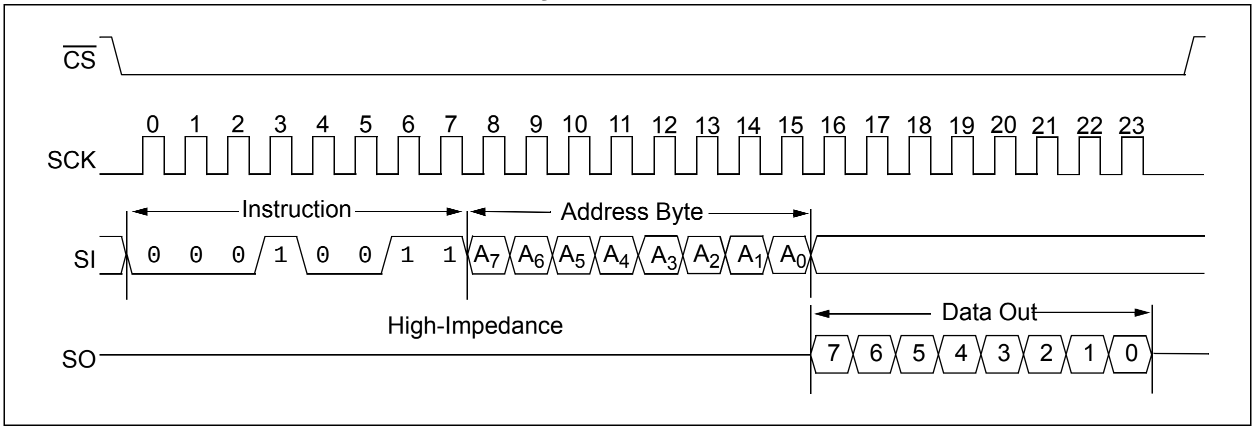


FIGURE 6-2: SRAM/RTCC READ SEQUENCE

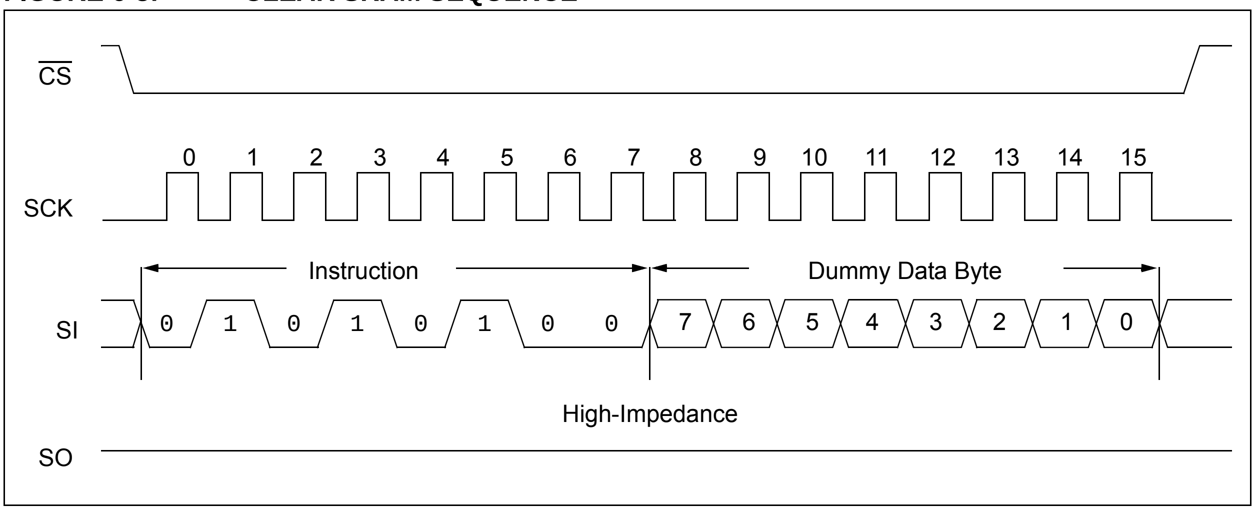


6.1.3 CLEAR SRAM INSTRUCTION

The CLRRAM instruction can be used to quickly clear the contents of SRAM to 0x00. The RTCC registers are not affected.

The device is selected by pulling $\overline{CS}$ low. The 8-bit CLRRAM instruction is transmitted to the MCP795XX followed by an 8-bit dummy data byte. $\overline{CS}$ is driven high to end the operation (Figure 6-3). The value of the data byte is ignored.

FIGURE 6-3: CLEAR SRAM SEQUENCE



6.2 Status Register

The STATUS register contains the BP<1:0>, WEL and WIP bits. The STATUS register is accessed using the SRREAD and SRWRITE instructions.

The Block Protection (BP<1:0>) bits are used to set the block write protection for the EEPROM array according to Table 6-1. These bits are set by the user issuing the SRWRITE instruction. These bits are nonvolatile.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the nonvolatile memory, when set to a '0', the latch prohibits writes to the nonvolatile memory. The state of this bit can be updated via the EEWREN or EEWRDI instructions. This bit is read-only.

The WIP bit indicates whether the MCP795XX is busy with a nonvolatile memory write operation. When set to a '1', a write is in progress. When set to a '0', no write is in progress. This bit is read-only.

TABLE 6-1: BLOCK PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	None
0	1	Upper 1/4 60h-7Fh (MCP7951X) C0h-FFh (MCP7952X)
1	0	Upper 1/2 40h-7Fh (MCP7951X) 80h-FFh (MCP7952X)
1	1	All

REGISTER 6-1: STATUS: EEPROM WRITE PROTECTION REGISTER

U-0	U-0	U-0	U-0	R/W	R/W	R-0	R-0
—	—	—	—	BP1	BP0	WEL	WIP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **BP<1:0>:** EEPROM Array Block Protection bits
Selects which EEPROM region is write-protected
00 = None
01 = Upper 1/4
10 = Upper 1/2
11 = All

bit 1 **WEL:** Write Enable Latch bit
Indicates whether or not nonvolatile memory writes are enabled. It is automatically cleared at the end of a nonvolatile memory write cycle.
0 = Writes to nonvolatile memory are not enabled
1 = Writes to nonvolatile memory are enabled

bit 0 **WIP:** Write-In-Process bit
Indicates whether or not a nonvolatile memory write cycle is in process
0 = Nonvolatile write cycle is not in process
1 = Nonvolatile write cycle is in process

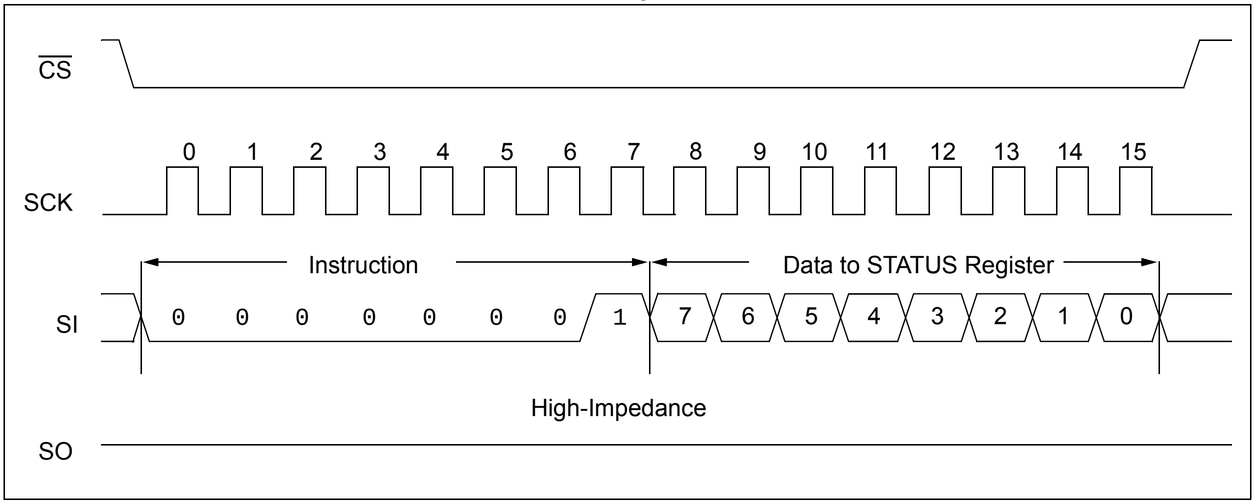
6.2.1 STATUS REGISTER WRITE SEQUENCE

The Write Status Register instruction (SRWRITE) allows the user to write to the nonvolatile bits in the STATUS register.

Prior to any attempt to write data to the STATUS register, the write enable latch must be set by issuing the EEWREN instruction. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the MCP795XX.

After all eight bits of the instruction are transmitted, $\overline{CS}$ must be driven high to set the write enable latch. If the write operation is initiated immediately after the EEWREN instruction without $\overline{CS}$ driven high, data will not be written to the array since the write enable latch was not properly set. The device is selected by pulling $\overline{CS}$ low. The 8-bit SRWRITE instruction is transmitted to the MCP795XX followed by the 8-bit data byte. $\overline{CS}$ is driven high to end the operation and initiate the nonvolatile write cycle (Figure 6-4).

FIGURE 6-4: WRITE STATUS REGISTER SEQUENCE

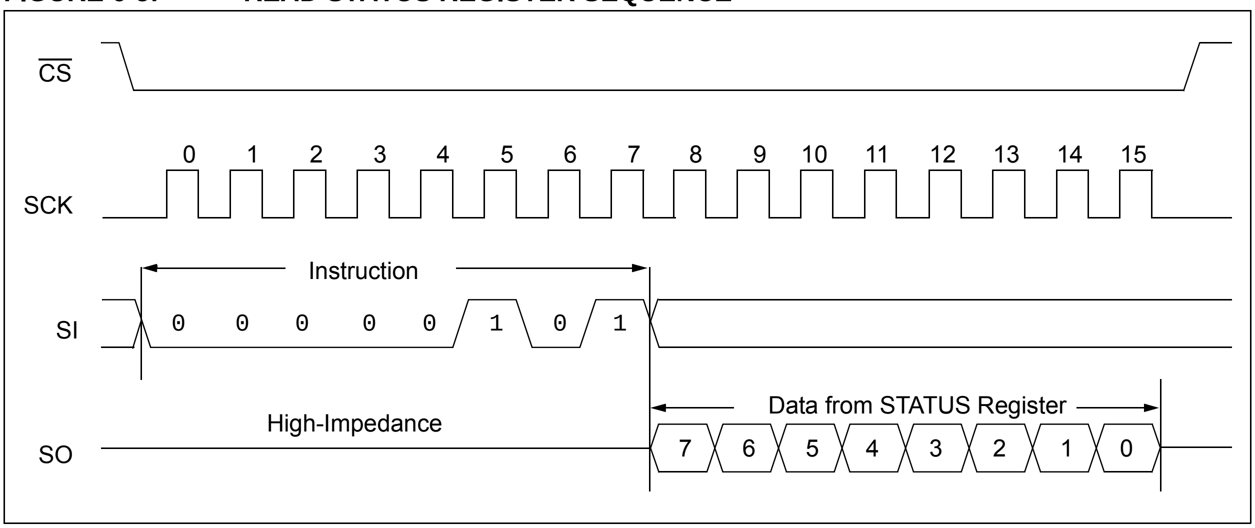


6.2.2 STATUS REGISTER READ SEQUENCE

The Read Status Register instruction (SRREAD) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. This allows the user to poll the WIP bit to determine when a write cycle is complete.

The device is selected by pulling $\overline{CS}$ low. The 8-bit SRREAD instruction is transmitted to the MCP795XX. The STATUS register value is then shifted out on the SO pin. The read operation is terminated by driving $\overline{CS}$ high (Figure 6-5).

FIGURE 6-5: READ STATUS REGISTER SEQUENCE



6.3 EEPROM

The MCP7952X features 2 Kbits of EEPROM, and the MCP7951X features 1 Kbit of EEPROM. It is organized in 8-byte pages with software write protection configurable through the STATUS register.

6.3.1 WRITE ENABLE AND WRITE DISABLE

The MCP795XX contains a write enable latch. This latch must be set before any write operation will be completed internally. The `EEWREN` instruction will set the latch, and the `EEWRDI` instruction will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- `WRDI` instruction successfully executed
- `EEWRITE` instruction successfully executed
- `SRWRITE` instruction successfully executed
- `IDWRITE` instruction successfully executed
- Unlock sequence for protected EEPROM not followed correctly

FIGURE 6-6: WRITE ENABLE SEQUENCE

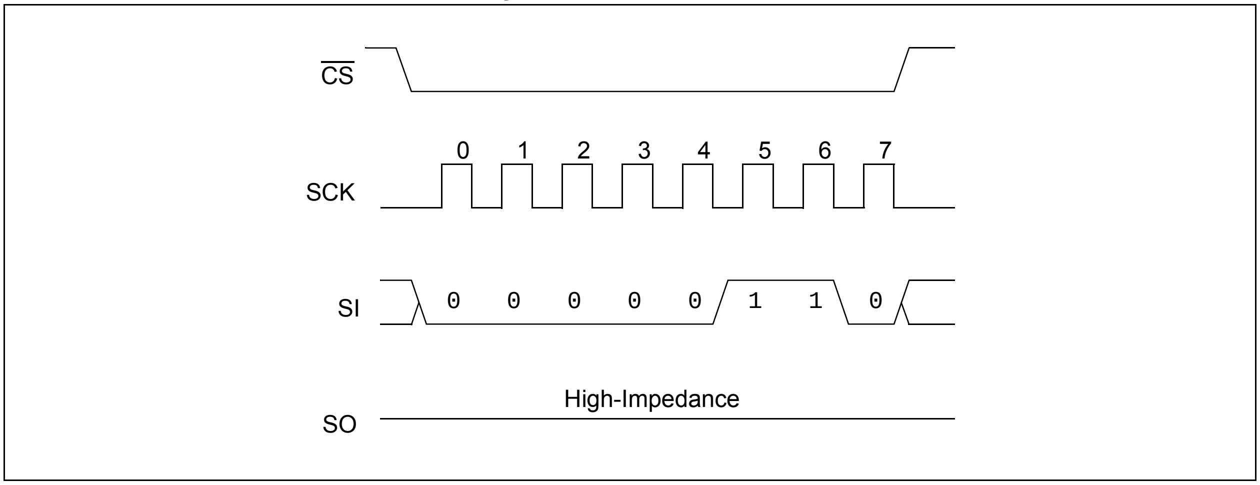
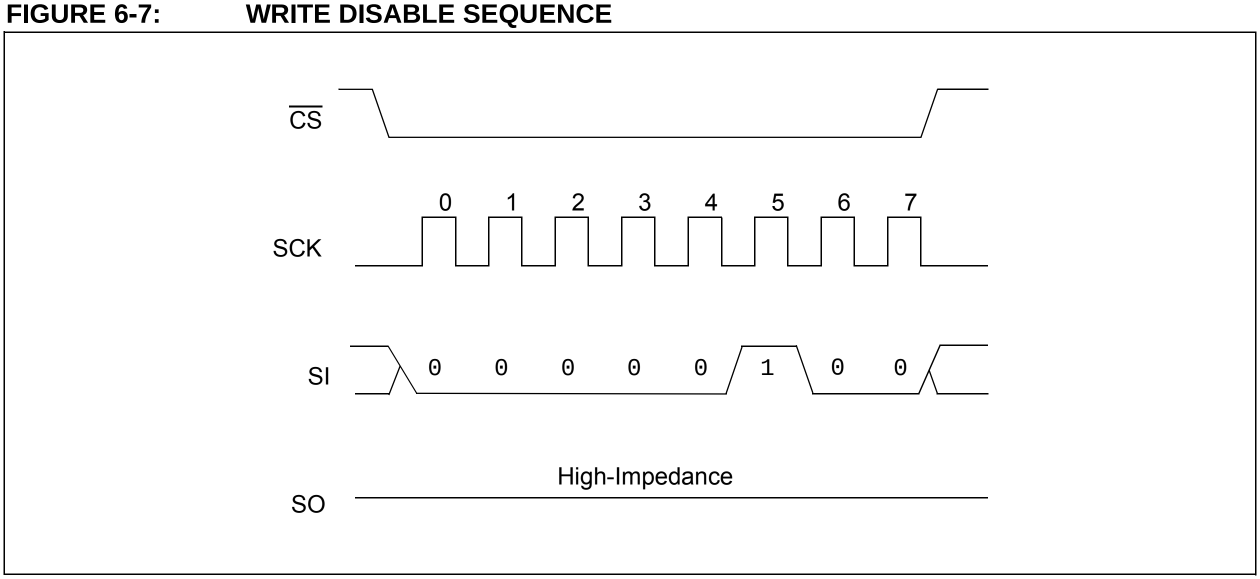


FIGURE 6-7: WRITE DISABLE SEQUENCE



6.3.2 EEPROM READ SEQUENCE

The device is selected by pulling $\overline{CS}$ low. The 8-bit `EEREAD` instruction is transmitted to the MCP795XX followed by an 8-bit address. See Figure 6-8 for more details.

After the correct `EEREAD` instruction and address are sent, the data stored in the EEPROM at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 00h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 6-8).

6.3.3 EEPROM WRITE SEQUENCE

Prior to any attempt to write data to the MCP795XX EEPROM, the write enable latch must be set by issuing the `EEWREN` instruction. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the MCP795XX. After all eight bits of the instruction are transmitted, $\overline{CS}$ must be driven high to set the write enable latch. If the write operation is initiated immediately after the `EEWREN` instruction without $\overline{CS}$ driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving $\overline{CS}$ low, issuing an `EEWRITE` instruction, followed by the address, and then the data to be written. Up to 8 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Additionally, a page address begins with `XXXX x000` and ends with `XXXX x111`. If the internal address counter reaches `XXXX x111` and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and over-write any data that previously existed in those locations.

> **Note:** EEPROM write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size – 1. If an `EEWRITE` command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent EEPROM write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is driven high at any other time, the write operation will not be completed. Refer to Figure 6-9 and Figure 6-10 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits. Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

FIGURE 6-8: EEPROM READ SEQUENCE

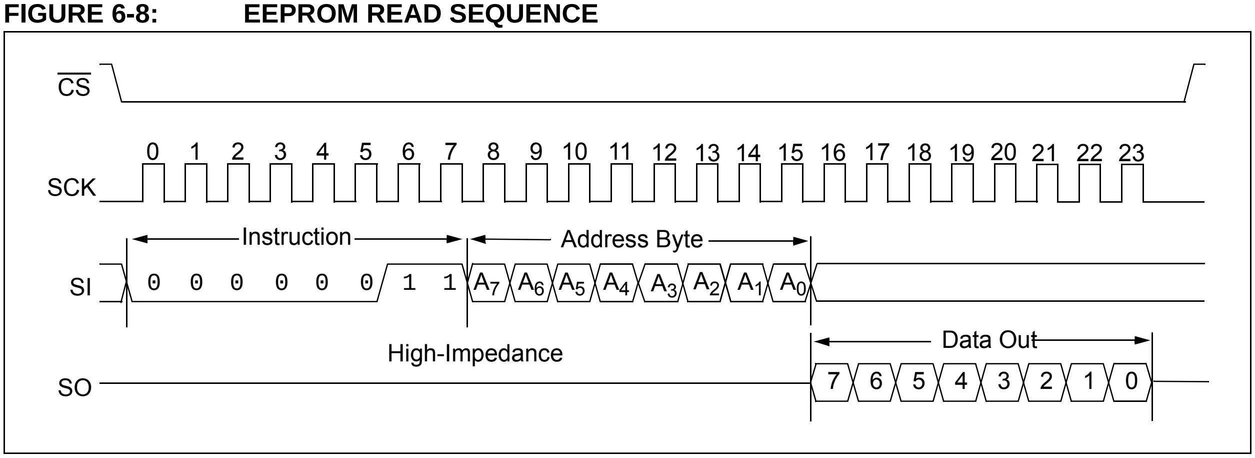


FIGURE 6-9: EEPROM BYTE WRITE SEQUENCE

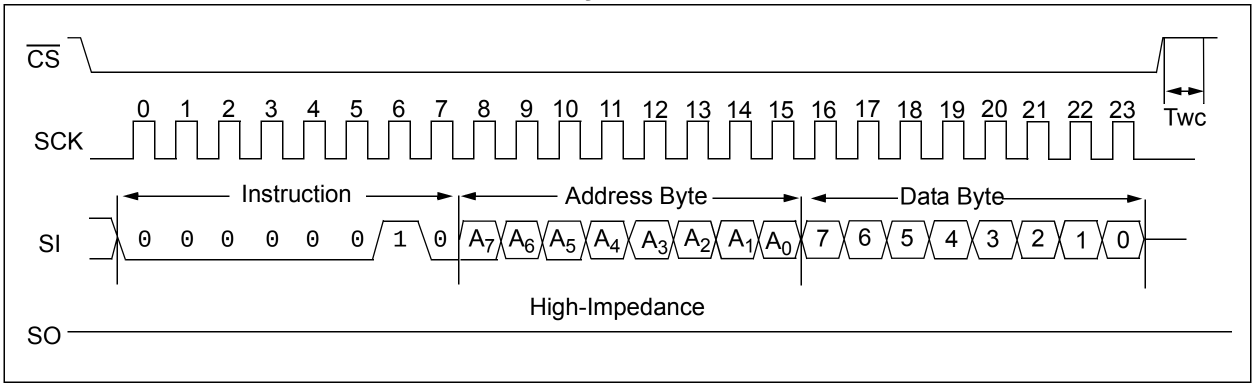
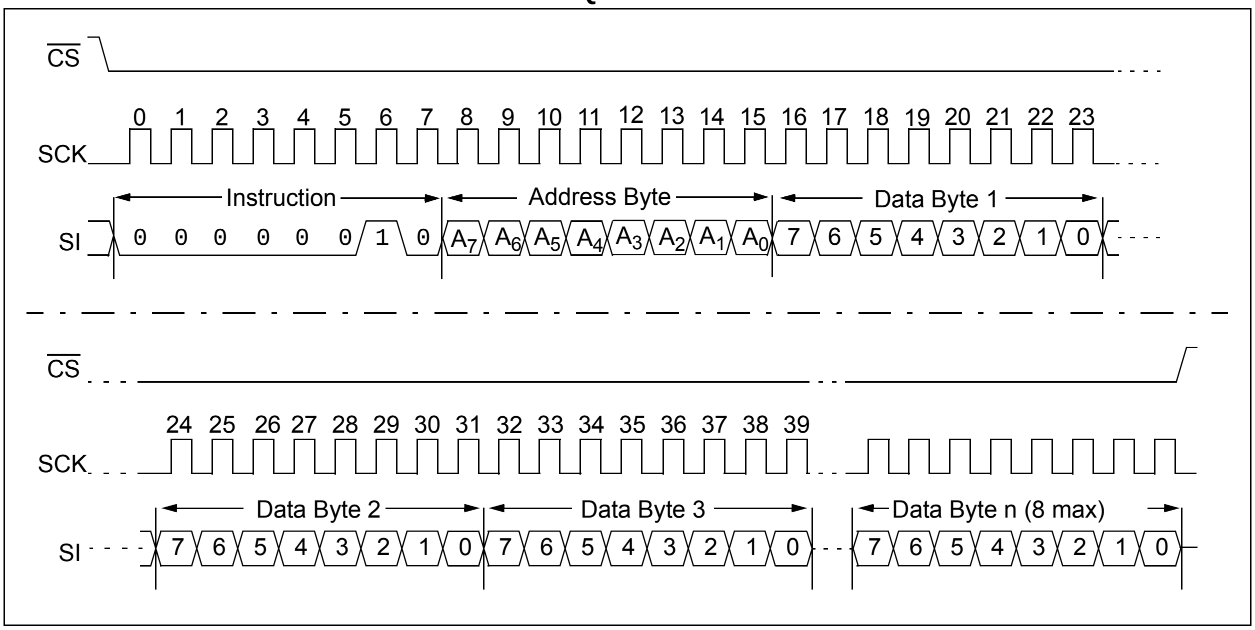


FIGURE 6-10: EEPROM PAGE WRITE SEQUENCE



6.4 Protected EEPROM

The MCP795XX features a 128-bit protected EEPROM block, organized as two 8-byte pages, that requires a special unlock sequence to be followed in order to write to the memory. The protected EEPROM can be used for storing crucial information such as a unique serial number. The MCP795X1 and MCP795X2 include an EUI-48 and EUI-64 node address, respectively, preprogrammed into the protected EEPROM block. Custom programming is also available.

The protected EEPROM block is located at addresses 0x00 to 0x0F and is accessed using the `IDREAD` and `IDWRITE` instructions.

Note:	Attempts to access addresses outside of 0x00 to 0x0F will result in the MCP795XX ignoring the instruction.

6.4.1 PROTECTED EEPROM READ SEQUENCE

The device is selected by pulling $\overline{\text{CS}}$ low. The 8-bit `IDREAD` instruction is transmitted to the MCP795XX followed by an 8-bit address. See Figure 6-11 for more details.

After the correct `IDREAD` instruction and address are sent, the data stored in the protected EEPROM at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 00h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{\text{CS}}$ pin.

6.4.2 PROTECTED EEPROM UNLOCK SEQUENCE

The protected EEPROM block requires a special unlock sequence to prevent unintended writes, utilizing the `UNLOCK` instruction.

Before performing the unlock sequence, the WEL bit must first be set by executing an `EEWREN` instruction (see **Section 6.3.1 "Write Enable and Write Disable"** for details).

To unlock the block, the following sequence must be followed after setting the WEL bit:

1. Execute an `UNLOCK` instruction with a data byte of 0x55
2. Execute an `UNLOCK` instruction with a data byte of 0xAA
3. Write the desired data bytes to the protected EEPROM using the `IDWRITE` instruction

Figure 6-12 illustrates the sequence.

> **Note 1:** Diverging from any step of the unlock sequence may result in the EEPROM remaining locked, the write operation being ignored, and the WEL bit being reset.
>
> **2:** Unlocking the EEPROM is not required in order to read from the memory.

An entire protected EEPROM page does not have to be written in a single operation. However, the block is locked after each write operation and must be unlocked again to start a new Write command.

6.4.3 PROTECTED EEPROM WRITE SEQUENCE

Prior to any attempt to write data to the MCP795XX protected EEPROM block, the write enable latch must be set by issuing the `EEWREN` instruction, and then the protected EEPROM unlock sequence must be performed. The `EEWREN` instruction is issued by setting $\overline{\text{CS}}$ low and then clocking out the proper instruction into the MCP795XX. After all eight bits of the instruction are transmitted, $\overline{\text{CS}}$ must be driven high to set the write enable latch.

After setting the write enable latch and performing the unlock sequence, the user may proceed by driving $\overline{\text{CS}}$ low, issuing an `IDWRITE` instruction, followed by the address, and then the data to be written. Up to 8 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with `XXXX x000` and ends with `XXXX x111`. If the internal address counter reaches `XXXX x111` and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and over-write any data that previously existed in those locations.

> **Note:** Protected EEPROM write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size – 1. If an `IDWRITE` command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent protected EEPROM write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{\text{CS}}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{\text{CS}}$ is driven high at any other time, the write operation will not be completed. Refer to Figure 6-12 for more detailed illustrations on the page write sequence. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits. Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

If an attempt is made to write to an address outside of the `0x00` to `0x0F` range, the MCP795XX will not execute the `WRITE` instruction, no data will be written, and the device will immediately accept a new command.

FIGURE 6-11: PROTECTED EEPROM READ SEQUENCE

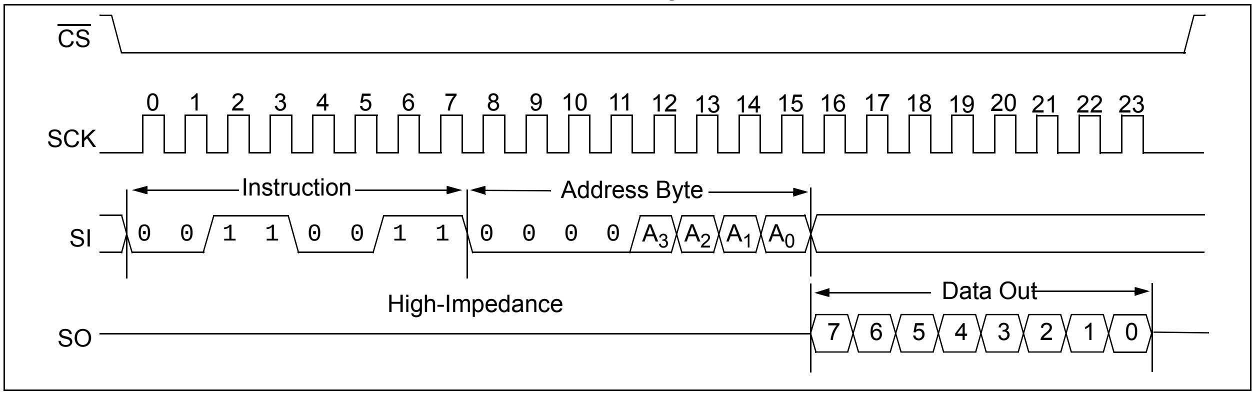
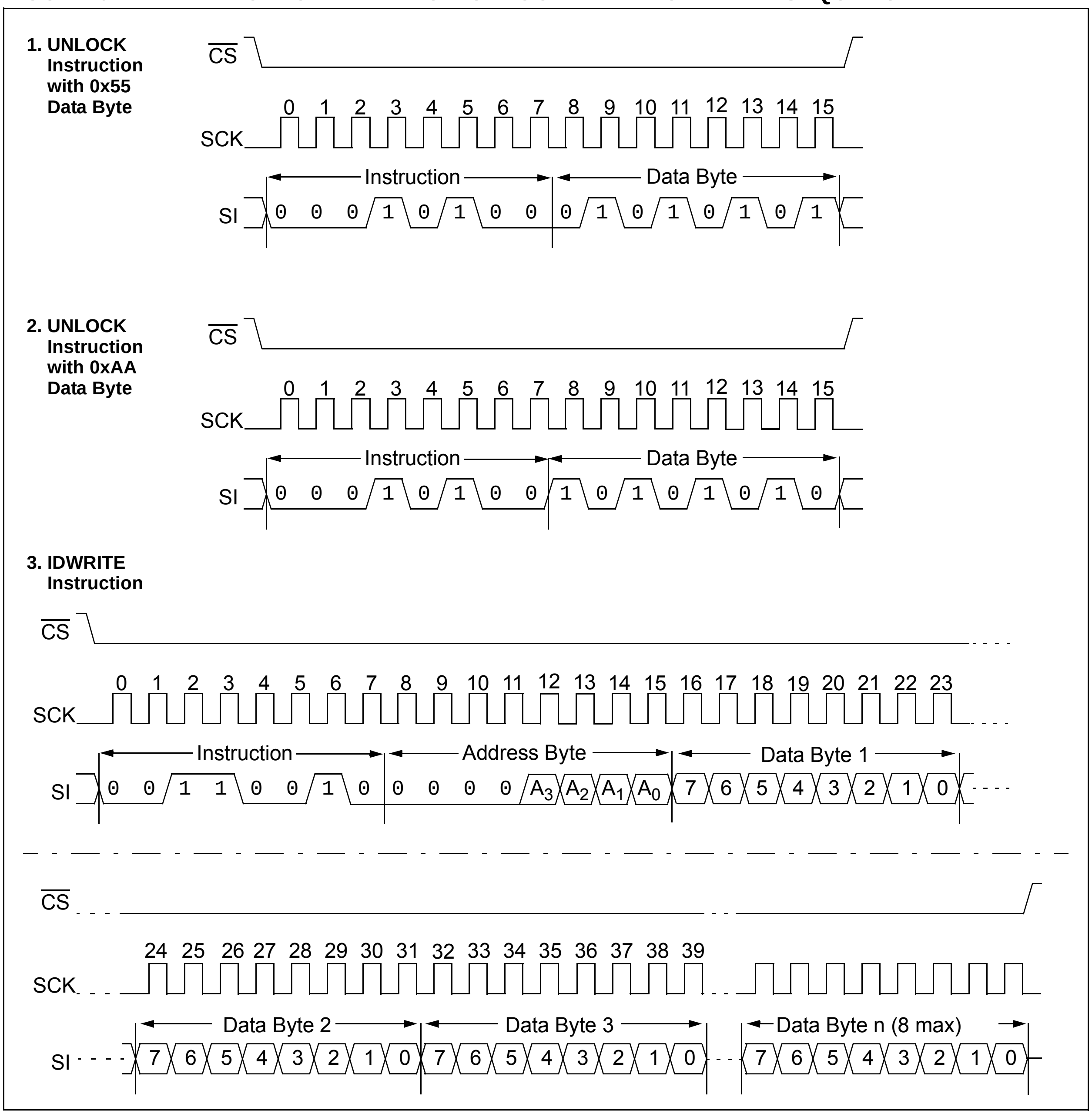


FIGURE 6-12: PROTECTED EEPROM UNLOCK AND PAGE WRITE SEQUENCE



6.5 Preprogrammed EUI-48™ or EUI-64™ Node Address

The MCP795X1 and MCP795X2 are programmed at the factory with a globally unique node address stored in the protected EEPROM block.

6.5.1 EUI-48 NODE ADDRESS (MCP795X1)

The 6-byte EUI-48 node address value of the MCP795X1 is stored in protected EEPROM locations 0x02 through 0x07, as shown in Figure 6-13. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining three bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

6.5.1.1 Organizationally Unique Identifiers (OUIs)

Each OUI provides roughly 16M (2^{24}) addresses. Once the address pool for an OUI is exhausted, Microchip will acquire a new OUI from IEEE to use for programming this model. For more information on past and current OUIs see *"Organizationally Unique Identifiers For Preprogrammed EUI-48 and EUI-64 Address Devices"* Technical Brief (DS90003187).

> **Note:** The OUI will change as addresses are exhausted. Customers are not guaranteed to receive a specific OUI and should design their application to accept new OUIs as they are introduced.

6.5.1.2 EUI-64 Support Using the MCP795X1

The preprogrammed EUI-48 node address of the MCP795X1 can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier, as shown below.

> **Note:** As an alternative, the MCP795X2 features an EUI-64 node address that can be used in EUI-64 applications directly without the need for encapsulation, thereby simplifying system software. See **Section 6.5.2 "EUI-64 Node Address (MCP795X2)"** for details.

6.5.2 EUI-64 NODE ADDRESS (MCP795X2)

The 8-byte EUI-64™ node address value of the MCP795X2 is stored in array locations 0x00 through 0x07, as shown in Figure 6-14. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority.

The remaining five bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 64-bit value..

> **Note:** In conformance with IEEE guidelines, Microchip will not use the values 0xFFFE and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values are specifically reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

FIGURE 6-13: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (MCP795X1)

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
Array Address	02h					07h

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Corresponding EUI-64™ Node Address After Encapsulation: 00-04-A3-FF-FE-12-34-56

FIGURE 6-14: EUI-64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (MCP795X2)

Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	90h
Array Address	00h							07h

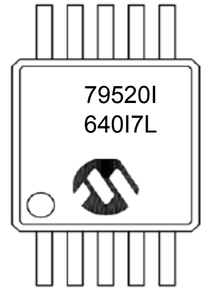
Corresponding EUI-64™ Node Address: 00-04-A3-12-34-56-78-90

7.0 PACKAGING INFORMATION

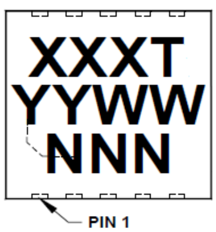
7.1 Package Marking Information

10-Lead MSOP (3x3 mm)

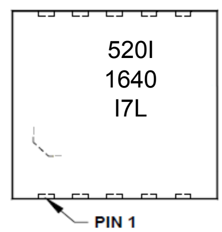
Example



10-Lead TDFN (03x03x0.8 mm)



Example



Part Number	1st Line Marking Codes	
	MSOP	**TDFN**
MCP79510	79510I	510I
MCP79520	79520I	520I
MCP79511	79511I	511I
MCP79521	79521I	521I
MCP79512	79512I	512I
MCP79522	79522I	522I

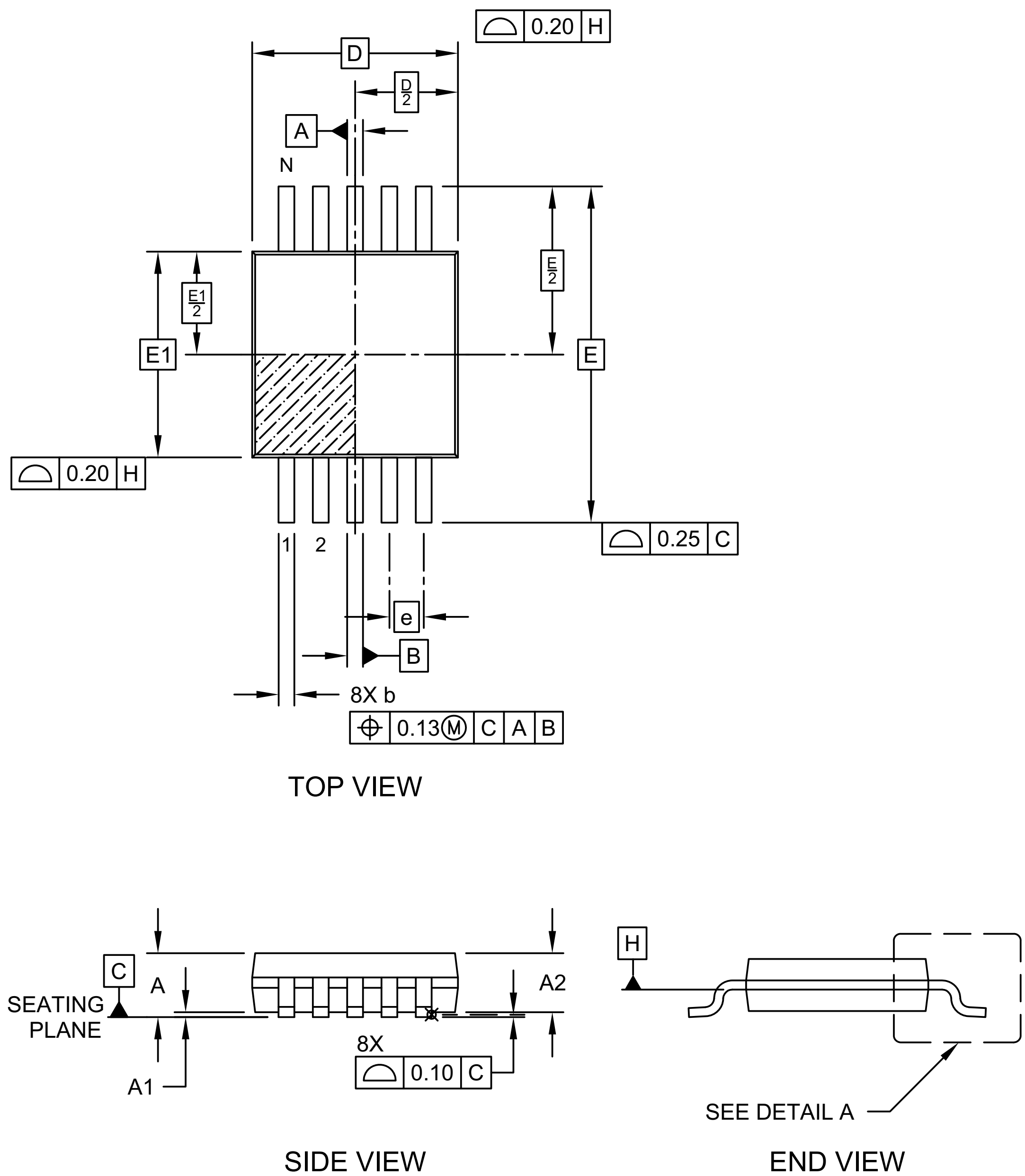
Note: T = Temperature grade
NN = Alphanumeric traceability code

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	JEDEC® designator for Matte Tin (Sn)
	*	This package is RoHS compliant. The JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

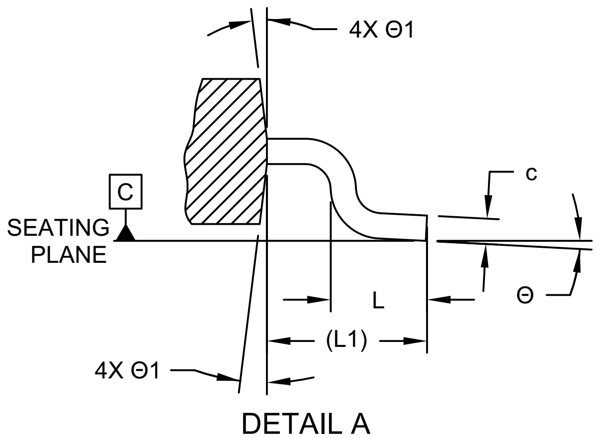
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

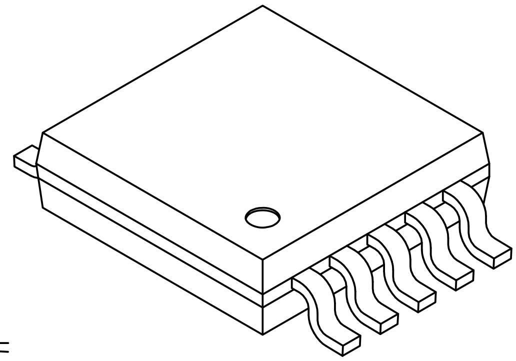


Microchip Technology Drawing C04-021D Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Mold Draft Angle	Θ	0°	-	8°
Foot Angle	Θ1	5°	-	15°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

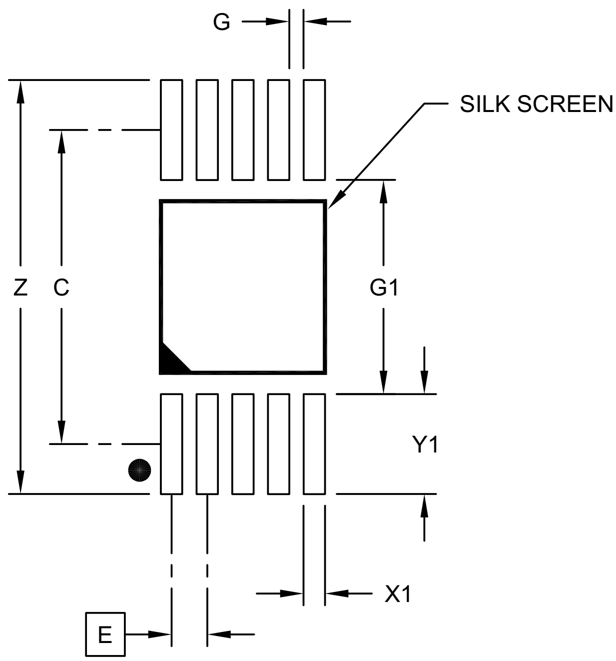
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021D Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

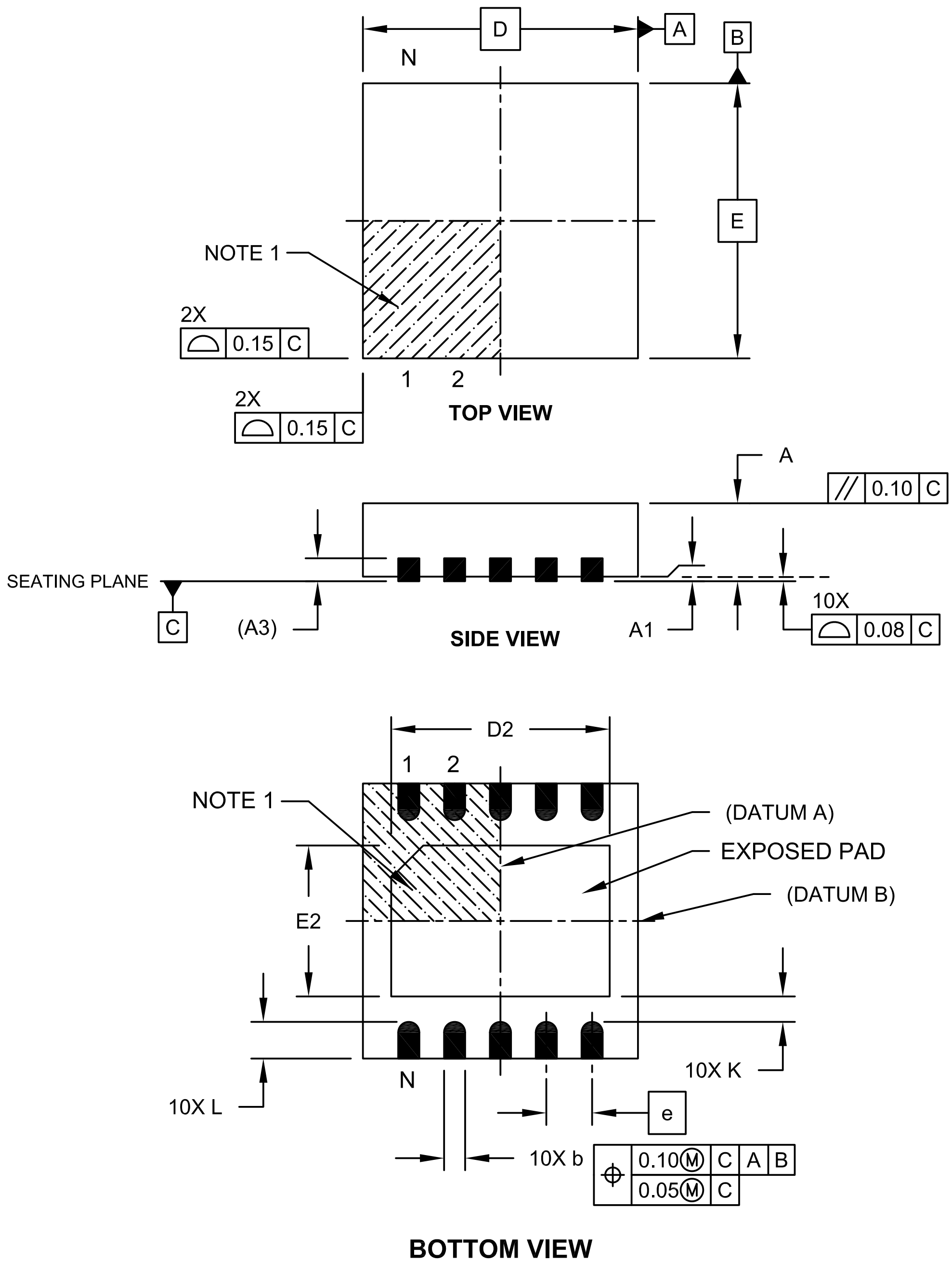
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021B

10-Lead Thin Plastic Dual Flat, No Lead Package (MN) - 3x3x0.8mm Body [TDFN]

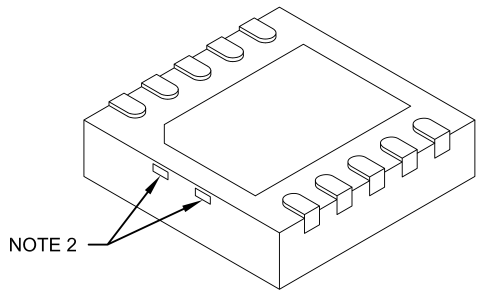
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-185A Sheet 1 of 2

10-Lead Thin Plastic Dual Flat, No Lead Package (MN) - 3x3x0.8mm Body [TDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.30	2.35
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.55	1.65	1.70
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-0185A Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision A (04/2012)

Initial release of this document.

Revision B (12/2016)

General rewrite of document for various corrections and improvements throughout; Removed preliminary status; Updated overall content for improved clarity; Added detailed descriptions of registers; Expanded descriptions of peripheral features; Updated block diagram and application schematic; Defined names for all bits and registers, and renamed the bits shown in Table 1 for clarification; Renamed the DC characteristics shown in Table 2 for clarification.

TABLE 1: BIT NAME CHANGES

Old Bit Name	New Bit Name
CALSGN	TRIMSIGN
OSCON	OSCRUN
VBAT	PWRFAIL
LP	LPYR
SQWE	SQWEN
ALM0	ALM0EN
ALM1	ALM1EN
RS0	SQWFS0
RS1	SQWFS1
RS2	CRSTRIM
CALIBRATION	TRIMVAL<7:0>
ALM0C<2:0>	ALM0MSK<2:0>
ALM1C<2:0>	ALM1MSK<2:0>

TABLE 2: DC CHARACTERISTIC NAME CHANGES

Old Name	Old Symbol	New Name	New Symbol
Operating Current	I_{CC} Read	EEPROM Operating Current	I_{CCEERD}
	I_{DD} Write		I_{CCEEWR}
V_{BAT} Current	I_{BAT}	Timekeeping Backup Current	I_{BATT}
Standby Current	I_{CCS}	V_{CC} Data Retention Current (oscillator off)	I_{CCDAT}

Revision C (02/2018)

Added detailed description of OUIs.

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PART NO.	X	X	[X][(1)] –	X	/XX
Device	Memory	Unique ID	Tape & Reel Option	Temp. Range	Package

Device:	MCP795		3V SPI Serial RTCC with Battery Switchover
Memory:	1	=	1 Kbit EEPROM, 64-Byte SRAM
	2	=	2 Kbit EEPROM, 64-Byte SRAM
ID/MAC Address:	0	=	Blank
	1	=	Preprogrammed EUI-48™ address
	2	=	Preprogrammed EUI-64™ address
Tape & Reel Option:	Blank	=	Tube
	T	=	Tape & Reel
Temperature Range:	I	=	-40°C to +85°C
Package:	MS	=	10-Lead Plastic Small Outline
	MN	=	10-Lead Thin Plastic Dual Flat (3x3x0.8 mm body)

Examples:

a) MCP79510-I/MS: 1 Kbit EEPROM, Industrial Temperature, MSOP Package.

b) MCP79511T-I/MN: 1 Kbit EEPROM, EUI-48™, Tape and Reel, Industrial Temperature, TDFN Package.

c) MCP79512-I/MS: 1 Kbit EEPROM, Preprogrammed EUI-64™ address, Industrial Temperature, MSOP Package.

d) MCP79520-I/MS: 2 Kbit EEPROM, Industrial Temperature, MSOP Package.

e) MCP79521T-I/MN: 2 Kbit EEPROM, EUI-48™, Tape and Reel, Industrial Temperature, TDFN Package.

f) MCP79522-I/MS: 2 Kbit EEPROM, EUI-64™, Industrial Temperature, MSOP Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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ISBN: 978-1-5224-2737-7

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