

## FEATURES

### Low offset voltage (maximum specifications)

B-Grade: 25  $\mu\text{V}$  (SOIC)

A-Grade: 50  $\mu\text{V}$  (SOIC), 90  $\mu\text{V}$  (MSOP)

### Very low offset voltage drift

B-Grade: 0.25  $\mu\text{V}/^\circ\text{C}$  (SOIC)

A-Grade: 0.55  $\mu\text{V}/^\circ\text{C}$  (SOIC) and 1.2  $\mu\text{V}/^\circ\text{C}$  (MSOP), specified over  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , MSL1 rated

### Low input bias current: 1.0 nA maximum

### Low noise: 7 nV/ $\sqrt{\text{Hz}}$ typical

### CMRR, PSRR, and $A_{\text{VO}}$ > 120 dB minimum

### Low supply current: 400 $\mu\text{A}$ per amplifier typical

### Wide bandwidth: 4.0 MHz

### Dual-supply operation: $\pm 5\text{ V}$ to $\pm 15\text{ V}$

### Unity-gain stable

### No phase reversal

## APPLICATIONS

### Process control front-end amplifiers

### Wireless base station control circuits

### Optical network control circuits

### Instrumentation

### Sensors and controls: thermocouples, resistor thermal detectors (RTDs), strain bridges, and shunt current measurements

### Precision filters

## GENERAL DESCRIPTION

The ADA4077-2 is a dual amplifier featuring extremely low offset voltage and drift and low input bias current, noise, and power consumption. Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

Applications for this amplifier include sensor signal conditioning (such as thermocouples, RTDs, strain gauges), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems. The ADA4077-2 is useful in line powered and portable instrumentation, precision filters, and voltage or current measurement and level setting.

Unlike the amplifiers of some competitors, the ADA4077-2 is specified over the extended industrial temperature range for operation from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  with MSL1 rating for the most demanding operating environments. It is available in 8-lead SOIC (including the B-Grade) and MSOP (A-Grade only) packages.

## PIN CONNECTION DIAGRAMS



Figure 1. ADA4077-2 Pin Configuration, 8-Lead MSOP



Figure 2. ADA4077-2 Pin Configuration, 8-Lead SOIC\_N

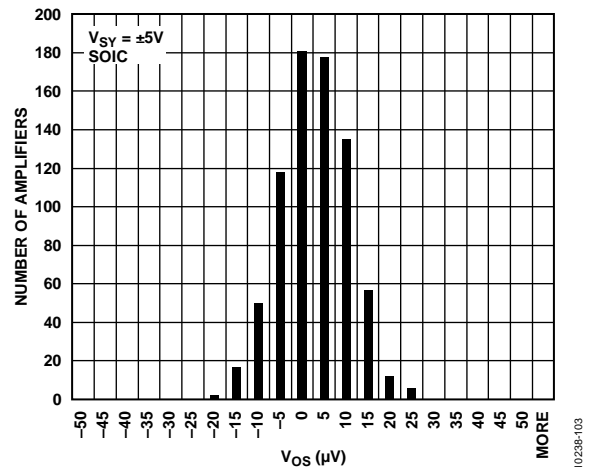


Figure 3. Offset Voltage Distribution

Table 1. Evolution of Precision Devices by Generation

Op Amp	1st	2nd	3rd	4th	5th	6th
Single	OP07	OP77	OP177	OP1177	AD8677	
Dual				OP2177		ADA4077-2
Quad				OP4177		

### Rev. 0

### Document Feedback

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**REVISION HISTORY**

10/12—Revision 0: Initial Version

## SPECIFICATIONS

ELECTRICAL CHARACTERISTICS,  $\pm 5.0$  V

$V_{SY} = \pm 5.0$  V,  $V_{CM} = 0$  V,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade, SOIC)	$V_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	25	$\mu\text{V}$
Offset Voltage Drift (B Grade, SOIC)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	65	$\mu\text{V}/^\circ\text{C}$
Offset Voltage (A Grade) SOIC	$V_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		15	50	$\mu\text{V}$
MSOP					105	$\mu\text{V}$
Offset Voltage Drift (A Grade) SOIC	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	0.55	$\mu\text{V}/^\circ\text{C}$
MSOP				0.5	1.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1	-0.4	+1	nA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.5		+1.5	nA
Input Voltage Range			-3.8		+3	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -3.8$ V to +3V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	122	140		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2$ k $\Omega$ , $V_O = -3.0$ V to +3.0 V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120	130		dB
Input Capacitance	$C_{INDM}$	Differential mode		3		pF
	$C_{INCM}$	Common mode		5		pF
Input Resistance	$R_{IN}$			100		M $\Omega$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$I_L = 1$ mA $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+4.1			V
Output Voltage Low	$V_{OL}$	$I_L = 1$ mA $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+4		-3.5	V
Output Current	$I_{OUT}$	$V_{DROPOUT} < 1.6$ V		$\pm 10$		mA
Short-Circuit Current	$I_{SC}$	$T_A = 25^\circ\text{C}$		22		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1$ kHz, $A_V = +1$		0.05		$\Omega$
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5$ V to $\pm 18$ V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	123	128		dB
Supply Current per Amplifier	$I_{SY}$	$V_O = 0$ V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120	400	450	$\mu\text{A}$
					650	$\mu\text{A}$
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2$ k $\Omega$		1		V/ $\mu\text{s}$
Settling Time to 0.1%	$t_s$	$V_{IN} = 1$ V step, $R_L = 4$ k $\Omega$ , $A_V = -1$		2		$\mu\text{s}$
Gain Bandwidth Product	GBP	$A_V = +1$		4.0		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_n$ p-p	0.1 Hz to 10 Hz		0.25		$\mu\text{V}$ p-p
Voltage Noise Density	$e_n$	$f = 1$ Hz		13		nV/ $\sqrt{\text{Hz}}$
		$f = 100$ Hz		7		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1$ kHz		3		pA/ $\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	$C_S$	$f = 1$ kHz		-120		dB

**ELECTRICAL CHARACTERISTICS, ±15.0 V**

$V_{SY} = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage (B Grade, SOIC)	$V_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	35	$\mu\text{V}$
Offset Voltage Drift (B Grade, SOIC)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.25	$\mu\text{V}/^\circ\text{C}$
Offset Voltage (A Grade) SOIC	$V_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		15	50	$\mu\text{V}$
MSOP					105	$\mu\text{V}$
Offset Voltage Drift (A Grade) SOIC	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	0.55	$\mu\text{V}/^\circ\text{C}$
MSOP				0.5	1.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1	-0.4	+1	nA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.5		+1.5	nA
Input Voltage Range			-0.5	+0.1	+0.5	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13.8\text{ V to }+13\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.0		+1.0	nA
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = -13.0\text{ V to }+13.0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-13.8		+13	V
Input Capacitance	$C_{INDM}$ $C_{INCM}$	Differential mode Common mode		3		pF
Input Resistance	$R_{IN}$			5		pF
				100		M $\Omega$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+14.1			V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+14		-13.5	V
Output Current	$I_{OUT}$	$V_{DROPOUT} < 1.2\text{ V}$		$\pm 10$	-13.2	V
Short-Circuit Current	$I_{SC}$	$T_A = 25^\circ\text{C}$		22		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}$ , $A_V = +1$		0.05		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5\text{ V to } \pm 18\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	123	128		dB
Supply Current per Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120	400	500	dB
					650	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		1		V/ $\mu\text{s}$
Settling Time to 0.01%	$t_s$	$V_{IN} = 10\text{ V p-p}$ , $R_L = 4\text{ k}\Omega$ , $A_V = -1$		9		$\mu\text{s}$
Settling Time to 0.1%	$t_s$	$V_{IN} = 10\text{ V p-p}$ , $R_L = 4\text{ k}\Omega$ , $A_V = -1$		8		$\mu\text{s}$
Gain Bandwidth Product	GBP	$A_V = +1$		3.9		MHz
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		0.25		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ Hz}$		13		nV/ $\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		7		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		3		pA/ $\sqrt{\text{Hz}}$
<b>MULTIPLE AMPLIFIERS CHANNEL SEPARATION</b>						
	$C_S$	$f = 1\text{ kHz}$		-120		dB

**ABSOLUTE MAXIMUM RATINGS**

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$\pm V_{SY}$
Differential Input Voltage	$\pm V_{SY}$
Storage Temperature Range	
MSOP and SOIC_N Packages	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	
R and RM Packages	-65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**THERMAL RESISTANCE**

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC_N	158	43	°C/W

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 4. Pin Configuration, 8-Lead MSOP (RM Suffix)



Figure 5. Pin Configuration, 8-Lead SOIC\_N (R Suffix)

Table 6. ADA4077-2 Pin Function Descriptions, MSOP and SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	-IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V-	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	-IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.

# TYPICAL PERFORMANCE CHARACTERISTICS

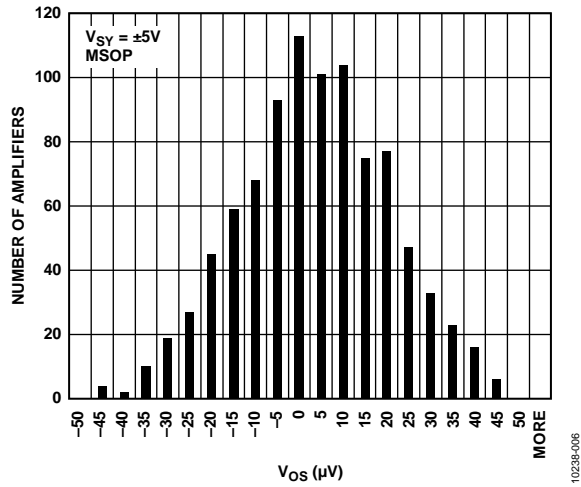


Figure 6. Offset Voltage Distribution

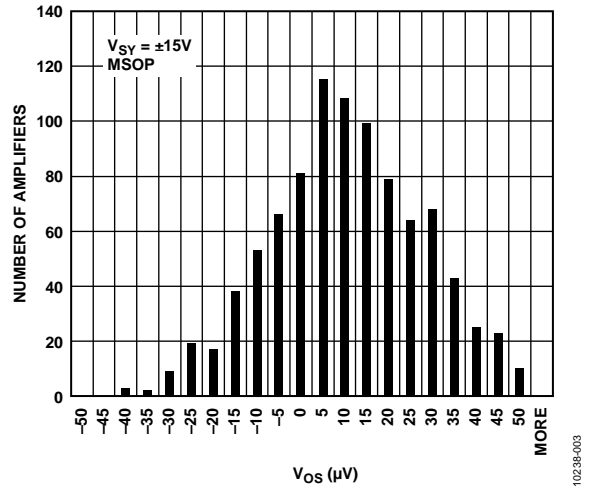


Figure 9. Offset Voltage Distribution

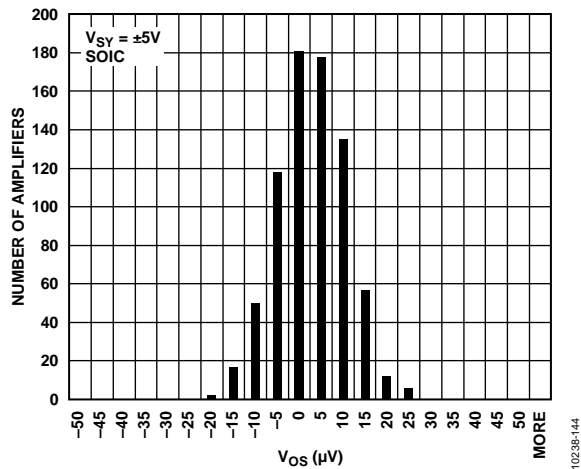


Figure 7. Offset Voltage Distribution

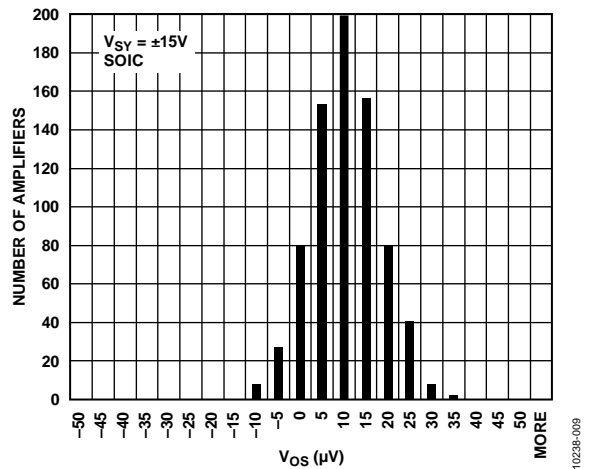


Figure 10. Offset Voltage Distribution



Figure 8. Offset Voltage vs. Temperature

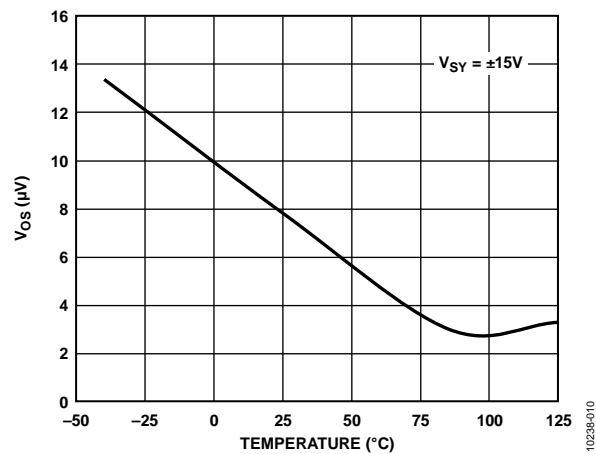


Figure 11. Offset Voltage vs. Temperature



Figure 12.  $TCV_{OS}$ , MSOP

10238-130

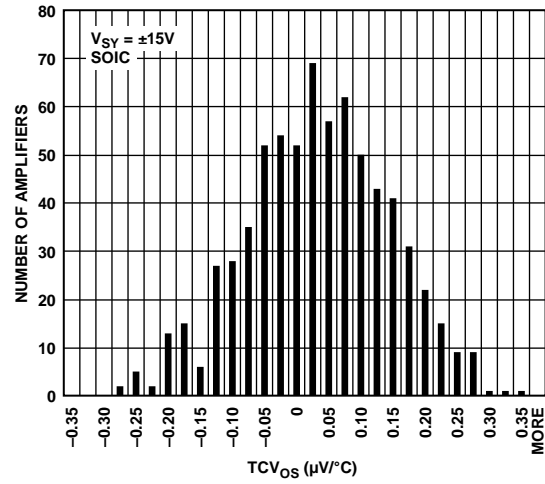


Figure 15.  $TCV_{OS}$ , SOIC

10238-008



Figure 13.  $V_{OS}$  vs. Supplies

10238-134

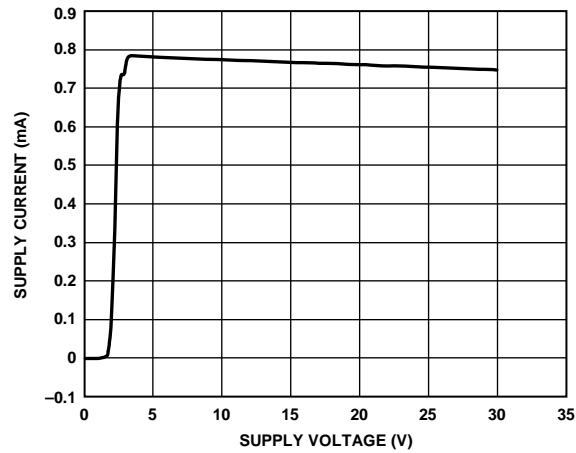


Figure 16.  $I_{SY}$  vs.  $V_{SY}$

10238-126

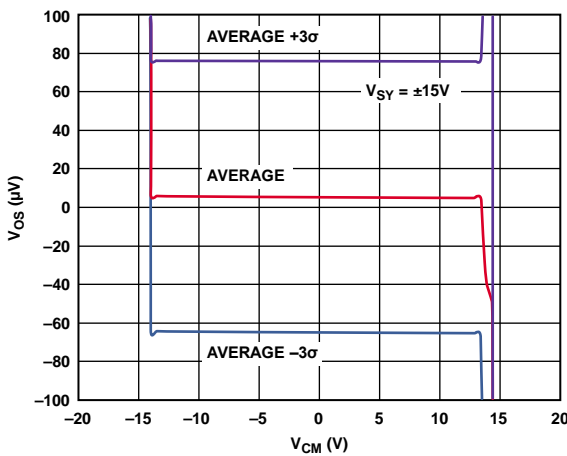


Figure 14.  $V_{OS}$  vs.  $V_{CM}$

10238-112

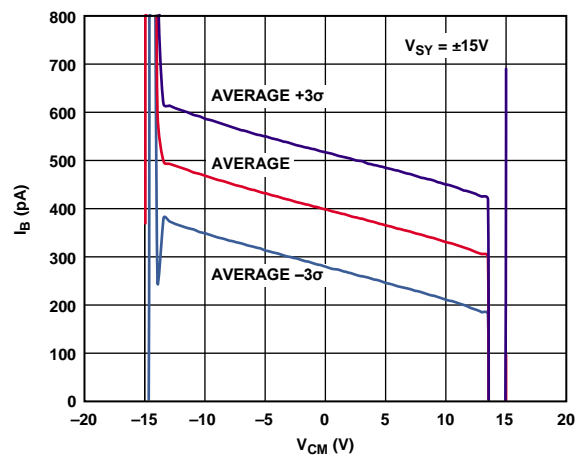


Figure 17. Input Bias Current vs.  $V_{CM}$

10238-115





Figure 18. Input Bias Current

10238-013

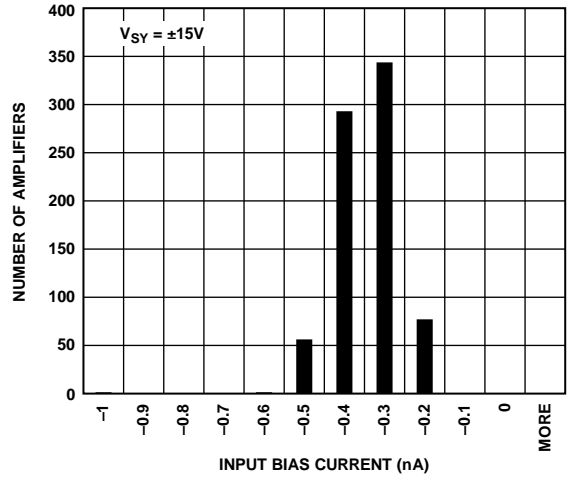


Figure 21. Input Bias Current

10238-016

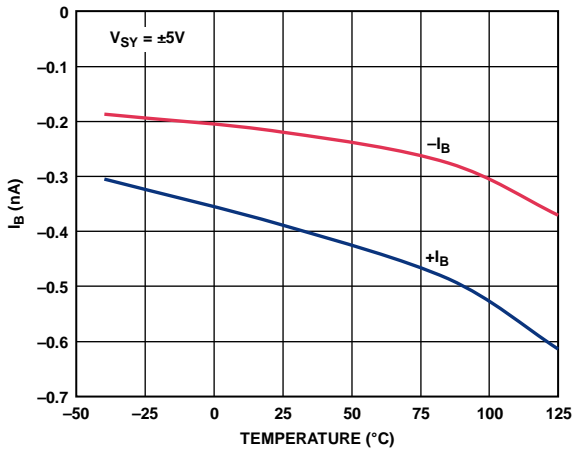


Figure 19. Input Bias Current vs. Temperature

10238-014

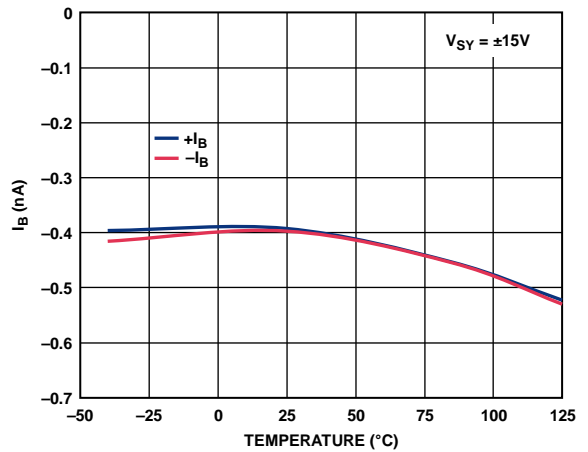


Figure 22. Input Bias Current vs. Temperature

10238-017

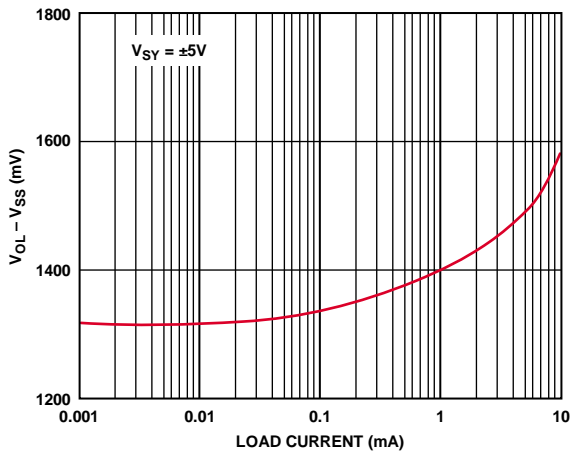


Figure 20. VOL vs. Load

10238-118

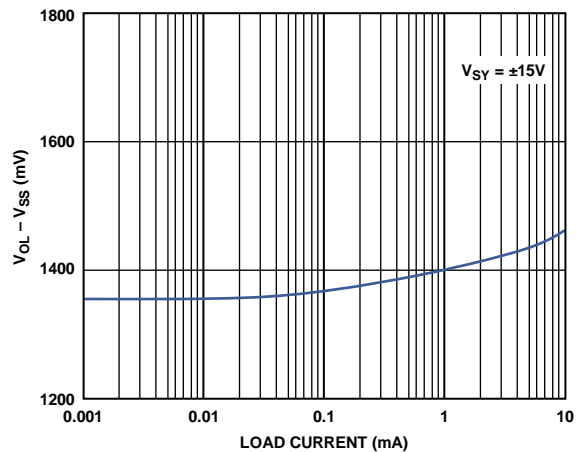


Figure 23. VOL vs. Load

10238-122



Figure 24. Output Dropout Voltage vs. Load



Figure 27. Output Dropout Voltage vs. Load



Figure 25. Open-Loop Gain and Phase vs. Frequency



Figure 28. Open-Loop Gain and Phase vs. Frequency



Figure 26. Output Voltage Swing vs. Temperature



Figure 29. Output Voltage Swing vs. Temperature



Figure 30. PSRR vs. Frequency,  $\pm 5 V$

10238-034



Figure 33. PSRR vs. Frequency,  $\pm 15 V$

10238-037



Figure 31. CMRR vs. Temperature

10238-030



Figure 34. CMRR vs. Temperature

10238-033



Figure 32. CMRR vs. Frequency

10238-029



Figure 35. PSRR vs. Temperature

10238-035

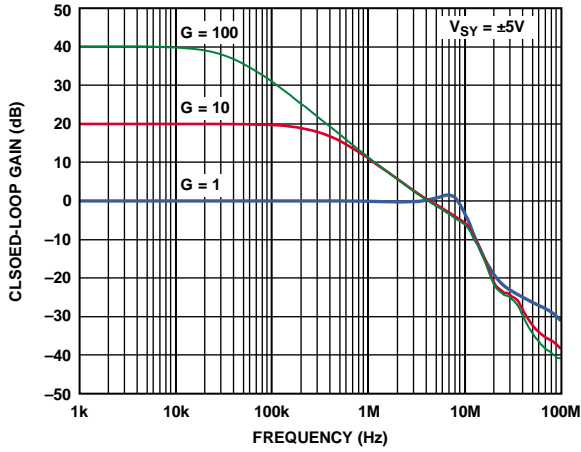


Figure 36. Closed-Loop Gain vs. Frequency

10238-028



Figure 39. Closed-Loop Gain vs. Frequency

10238-031

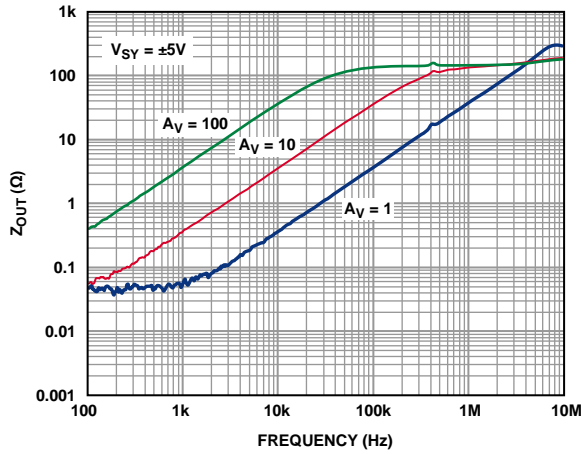


Figure 37. Output Impedance vs. Frequency

10238-036



Figure 40. Output Impedance vs. Frequency

10238-039



Figure 38. Large Signal Transient Response

10238-040



Figure 41. Large Signal Transient Response

10238-043



Figure 42. Small Signal Transient Response

10238-041



Figure 45. Small Signal Transient Response

10238-044

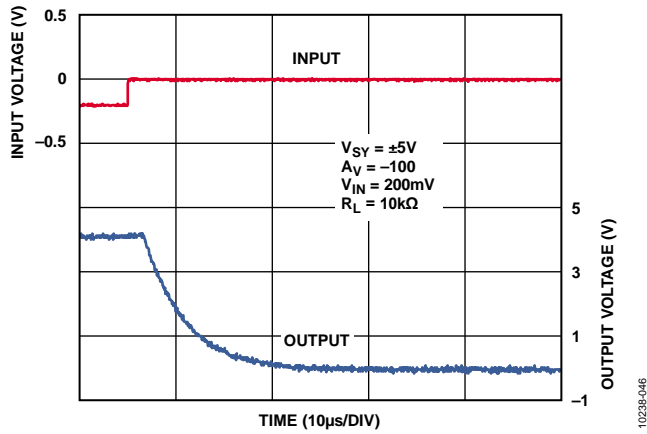


Figure 43. Positive Overload Recovery

10238-046

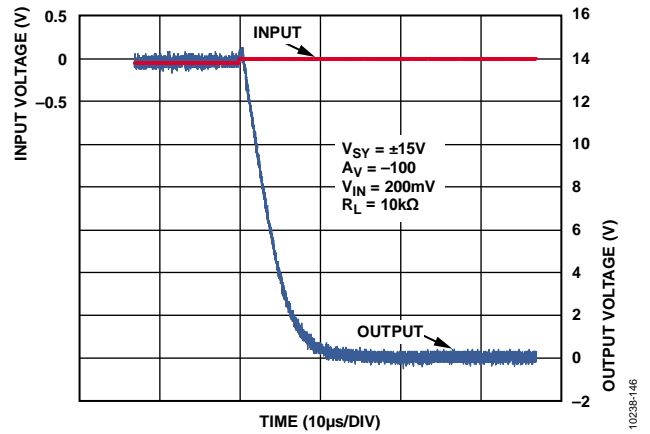


Figure 46. Positive Overload Recovery

10238-146

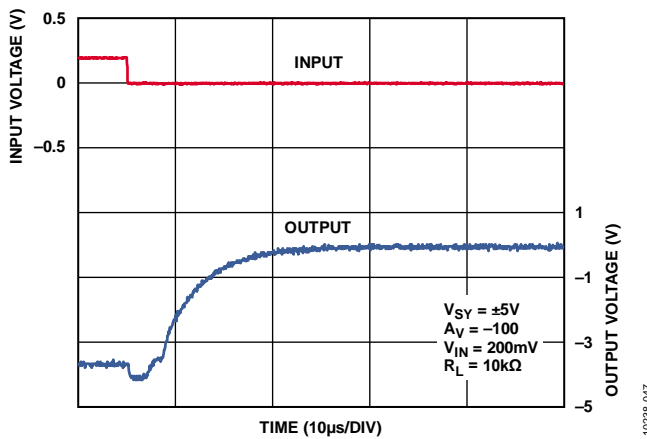


Figure 44. Negative Overload Recovery

10238-047

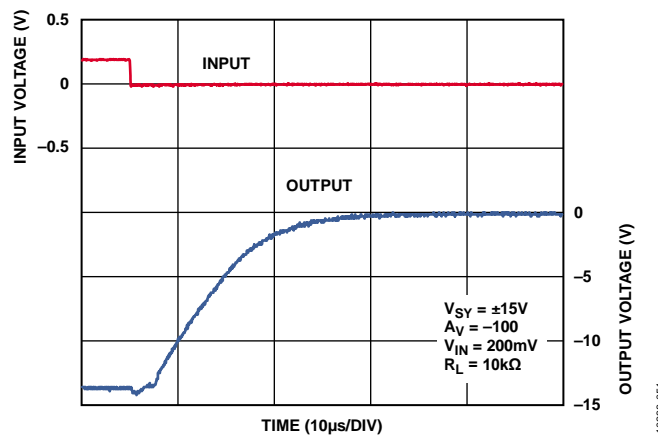


Figure 47. Negative Overload Recovery

10238-051



Figure 48. Small Signal Overshoot vs. Load Capacitance



Figure 51. Small Signal Overshoot vs. Load Capacitance



Figure 49. Positive Settling Time



Figure 52. Positive Settling Time



Figure 50. Voltage Noise Density vs. Frequency

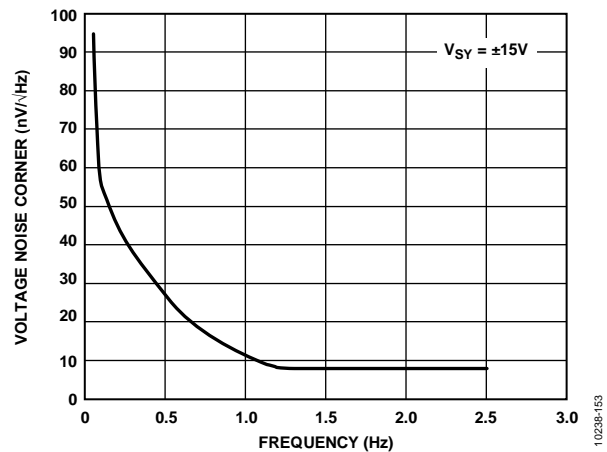


Figure 53. Voltage Noise Corner Frequency



Figure 54. THD + N vs. Frequency



Figure 56. THD + N vs. Frequency

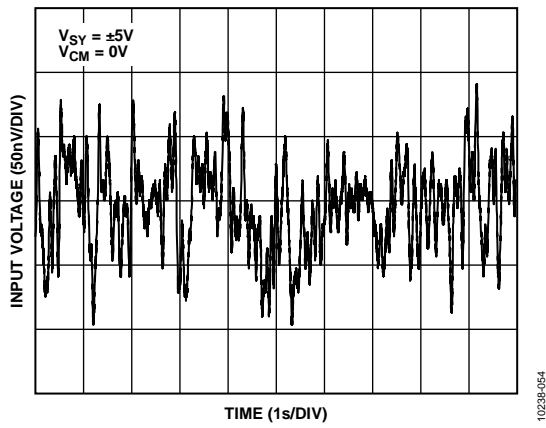


Figure 55. 0.1 Hz to 10 Hz Noise

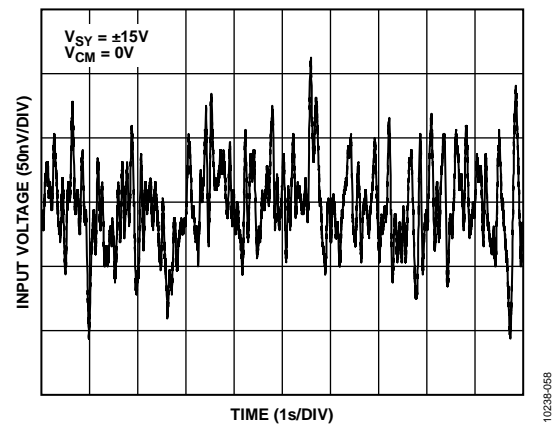


Figure 57. 0.1 Hz to 10 Hz Noise

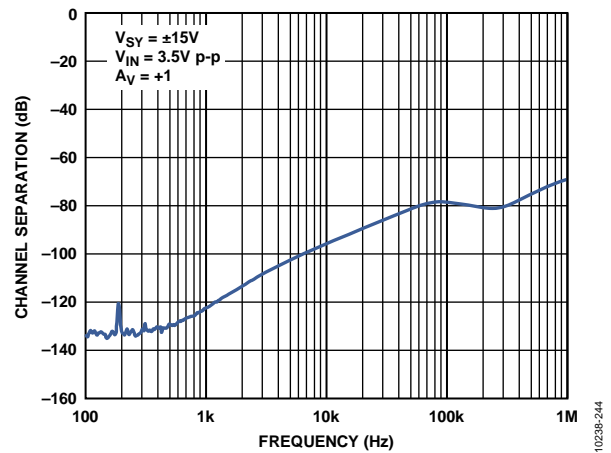


Figure 58. Channel Separation

## THEORY OF OPERATION

The [ADA4077-2](#) is the sixth generation of the Analog Devices, Inc., industry-standard [OP07](#) amplifier family. The [ADA4077-2](#) is a high precision, low noise operational amplifier with a combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125°C.

The Analog Devices proprietary process technology and linear design expertise have produced a high voltage amplifier with superior performance to the [OP07](#), [OP77](#), [OP177](#), and [OP1177](#) in tiny, 8-lead SOIC and 8-lead MSOP packages. Despite its small size, the [ADA4077-2](#) offers numerous improvements, including low wideband noise, wide bandwidth, lower offset and offset drift, lower input bias current, and complete freedom from phase inversion.

The [ADA4077-2](#) has a specified operating temperature range of -40°C to +125°C with a MSL1 rating, which is as wide as any similar device in a plastic surface-mount package. This is increasingly important as PCB and overall system sizes continue to shrink, causing internal system temperatures to rise.

In the [ADA4077-2](#), power consumption is reduced by a factor of four from the [OP177](#), and bandwidth and slew rate have both increased by a factor of six. The low power dissipation and very stable performance vs. temperature also act to reduce warm-up drift errors to insignificant levels.

Inputs are protected internally from overvoltage conditions referenced to either supply rail. Like any high performance amplifier, maximum performance is achieved by following appropriate circuit and PCB guidelines.



## APPLICATIONS INFORMATION

### OUTPUT PHASE REVERSAL

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ADA4077-2 is immune to phase reversal problems even at input voltages beyond the supplies.

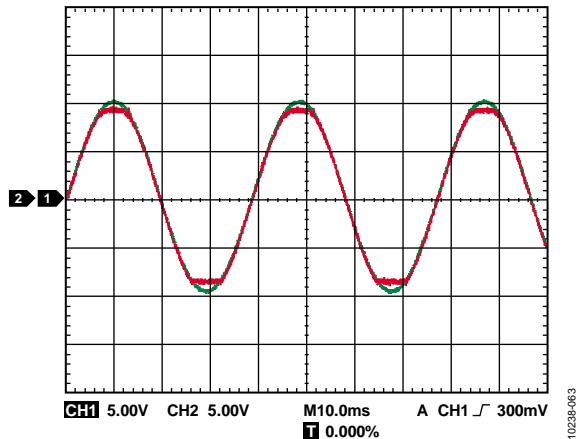


Figure 59. No Phase Reversal

### LOW POWER LINEARIZED RTD

A common application for a single element varying bridge is an RTD thermometer amplifier, as shown in Figure 60. The excitation is delivered to the bridge by a 2.5 V reference applied at the top of the bridge.

RTDs can have a thermal resistance as high as 0.5°C to 0.8°C per mW. To minimize errors due to resistor drift, the current through each leg of the bridge must be kept low. In this circuit, the amplifier supply current flows through the bridge. However, at the ADA4077-2 maximum supply current of 500 μA, the RTD dissipates less than 0.1 mW of power, even at the highest resistance. Errors due to power dissipation in the bridge are kept under 0.1°C.

Calibration of the bridge is made at the minimum value of the temperature to be measured by adjusting RP until the output is zero.

To calibrate the output span, set the full-scale and linearity potentiometers to midpoint and apply a 500°C temperature to the sensor or substitute the equivalent 500°C RTD resistance.

Adjust the full-scale potentiometer for a 5 V output. Finally, apply 250°C or the equivalent RTD resistance and adjust the linearity potentiometer for 2.5 V output. The circuit achieves better than ±0.5°C accuracy after adjustment.



Figure 60. Low Power Linearized RTD Circuit

### PROPER BOARD LAYOUT

The ADA4077-2 is a high precision device. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout.

To avoid leakage currents, maintain a clean and moisture-free board surface. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

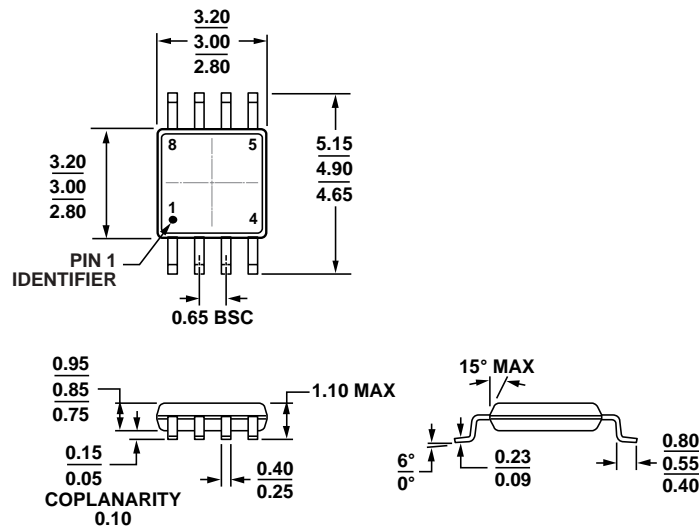
Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances caused by output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and helps to maintain a constant temperature across the circuit board.

# PACKAGING AND ORDERING INFORMATION

## OUTLINE DIMENSIONS

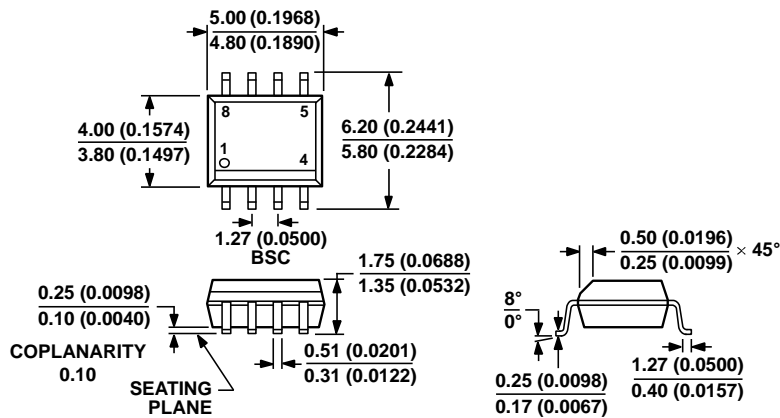


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 61. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2009-B



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 62. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407-A

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADA4077-2-ARMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-R7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-RL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

<sup>1</sup> Z = RoHS Compliant Part.



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- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
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