DEMO9S12XHY256

Demonstration Board for Freescale MC9S12XHY256 Microcontroller

USER GUIDE

Web Site: www.axman.com

Support: support@axman.com

CONTENTS

CAUTIONARY NOTES **4**
TERMINOLOGY **4**
FEATURES **5**
MEMORY MAP **6**
SOFTWARE DEVELOPMENT **6**
DEVELOPMENT SUPPORT **7**
INTEGRATED BDM 7
BDM_PORT HEADER 7
POWER **8**
POWER SELECT 8
PWR_SEL *8*
VX_EN *9*
RESET SWITCH **10**
LOW VOLTAGE RESET **10**
CLOCK **10**
COMMUNICATIONS **10**
RS-232 11
COM CONNECTOR *11*
COM_SEL *11*
USB SERIAL LINK 12
LIN PORT 12
LIN ENABLE *13*
LIN COM INPUT *13*
WAKE OPTION *13*
LIN_PWR OPTION *13*
MSTR OPTION *14*
LIN CONNECTOR *14*
CAN PORT 14
CAN TERMINATION ENABLE *15*
STANDBY MODE *16*
LCD **16**
LCD CONNECTIONS 16
MOTOR CONTROLLER **18**
MC POWER INPUT 18
MC PWM OUTPUT 18
MCU I/O PORT **19**
USER I/O **20**

POTENTIOMETER 20
LED'S 20
PUSHBUTTON SWITCHES 20

ACRONYMS 21

FIGURES

Figure 1: Memory Map 6
Figure 2: BDM_PORT Header 8
Figure 3: V_SEL Option Header 9
Figure 4: VX_EN Option Header 10
Figure 5: Serial Connections 11
Figure 6: COM1 Connector 11
Figure 7: COM_SEL Option Header 12
Figure 8: BCOM_EN Option Header 12
Figure 9: LIN Block Diagram 12
Figure 10: Option Header 13
Figure 11: LIN Option Header 14
Figure 12: LIN Connector 14
Figure 13: CAN_PORT 15
Figure 14: CAN Termination Enable 15
Figure 15: LCD Connections 17
Figure 16: Motor Power Input 18
Figure 17: Motor Controller I/O PORT 19
Figure 18: MCU I/O PORT 19
Figure 19: User Option Header 20

REVISION

Date	Rev	Comments
June 29, 2010	A	Initial Release
July 15, 2010	B	Minor corrections, Added option reference designators, Re-ordered document structure, Added acronyms section

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the DEMO9S12XHY256 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

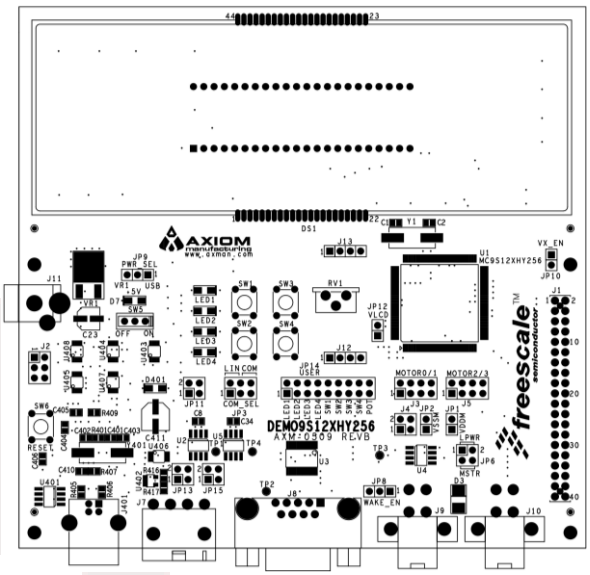
Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The DEMO9S12XHY256 is a demonstration board for the MC9S12XHY256 microcontroller. Application development is quick and easy with the integrated USB-BDM, sample software tools, and examples. An optional BDM_PORT port is also provided to allow use of a BDM_PORT cable. A 40-pin connector provides access to most IO signals on the target MCU.



MC9S12XHY256, 100 LQFP
- S12XCPU
- 256K Bytes Flash
- 8K Bytes Data Flash
- 12K Bytes RAM
- 8Ch, 12b ADC
- Integrated LCD Driver
- Integrated 4-Ch Stepper Motor Controller
- Integrated Stepper Motor Stall Detect
- 40MHz Maximum Bus Frequency

- On-Board 4x40 Custom LCD Glass
- 2 ea. High-Speed CAN Physical Layer Transceivers
- Enhanced LIN Physical Layer Transceiver
- RS-232 Serial Data Physical Layer Transceiver
- Integrated USB-BDM
- BDM_PORT header for external BDM cable support
- MCU_PORT pin header for access to MCU IO signals
- On-board +5V regulator
- Optional Power from USB-BDM or MCU_PORT connector
- Power Input Selection Jumpers
  - Power input from USB-BDM
  - Power input from on-board regulator
  - Power input from Connector J1
  - Optional Power output through Connector J1
- User Components Provided
  - 5 Push Switches; 4 User, 1 Reset
  - 6 LED Indicators; 4 User, +5V, USB
  - 5K ohm POT w /LP Filter
- User Option Jumpers to disconnect Peripherals
- Connectors
  - 40-pin MCU I/O Pin Header
  - 2.0mm Barrel Connector
  - BDM_PORT Connector for External BDM Cable
  - USB Connector
  - DB9 Connector
  - 4.2mm, 1x4 Molex CAN Cable Connector
  - 4.2mm, 2x2 Molex LIN Cable Connector

Specifications:
Board Size 5.5” x 5.25”

MEMORY MAP

Figure 1 below shows the device register memory map. Refer to the MC9S12XHY256 Reference Manual (RM) for further information.

Figure 1: Memory Map

Address	Module	Size (Bytes)
0x0000–0x0009	PIM (port integration module)	10
0x000A–0x000B	MMC (memory map control)	2
0x000C–0x000D	PIM (port integration module)	2
0x000E–0x000F	Reserved	2
0x0010–0x0017	MMC (memory map control)	8
0x0018–0x0019	Reserved	2
0x001A–0x001B	Device ID register	2
0x001C–0x001F	PIM (port integration module)	4
0x0020–0x002F	DBG (debug module)	16
0x0030–0x0033	Reserved	4
0x0034–0x003F	ECRG (clock and reset generator)	12
0x0040–0x006F	TIM0 (timer module)	48
0x0070–0x009F	ATD (analog-to-digital converter 10 bit 8-channel)	48
0x00A0–0x00C7	PWM (pulse-width modulator 8 channels)	40
0x00C8–0x00 D7	SCI[1:0] (serial communications interface)	16
0x00D8–0x00DF	SPI (serial peripheral interface)	8
0x00E0–0x00E7	IIC (Inter IC bus)	8
0x00E8–0x00FF	Reserved	24
0x0100–0x0113	FTMR control registers	20
0x0114–0x011F	Reserved	12
0x0120-0x012F	INT (interrupt module)	1
0x0130–0x013F	Reserved	31
0x0140–0x017F	CAN0	64
0x0180–0x01BF	CAN1	64
0x01C0–0x01FF	MC(motor controller)	64
0x0200–0x021F	LCD	32
0x0220–0x023F	Stepper Stall Detector 0 (SSD[3:0])	32
0x0240–0x029F	PIM (port integration module)	96
0x02A0–0x02CF	TIM1(timer module)	48
0x02D0–0x02EF	Reserved	32
0x02F0–0x02F7	Voltage Regulator	8
0x02F8–0x07FF	Reserved	1288

SOFTWARE DEVELOPMENT

Software development requires the use of a compiler or an assembler supporting the HCS12(X) instruction set and a host PC operating a debug interface. CodeWarrior Development Studio is supplied with this board for application development and debug. Refer to the supporting CodeWarrior documentation for details on use and capabilities.

DEVELOPMENT SUPPORT

Application development and debug for the target MC9S12XHY256 is supported through the background debug mode (BDM) interface. The BDM interface consists of an integrated USB-Multilink BDM and a 6-pin interface header (BDM_PORT). The BDM_PORT header allows connecting an external HCS12 BDM cable. Refer to the MC9S12XHY Reference Manual for details and capabilities of the BDM.

Integrated BDM

The DEMO9S12XHY256 board features an integrated USB-BDM. The integrated BDM supports application development and debug via background debug mode. All necessary signals are provided by the integrated BDM. A USB, type B, connector provides connection from the target board to a host PC.

The integrated USB-Multilink BDM provides power and ground to the target board eliminating the need for external power. Power from the USB-Multilink BDM is derived from the USB bus; therefore, total current consumption for the target board, and connected circuitry, **must not exceed 500mA**. This current limit describes the current supplied by the USB cable to the BDM circuit, the target board, and any connected circuitry. Excessive current drain will violate the USB specification causing the bus to disconnect. Damage to the host PC USB hub or the target board may result.

CAUTION:

When powered from the USB bus, do not exceed the 500mA maximum allowable current drain. Damage to the target board or host PC may result

NOTE:

10K ohm pull-ups are applied to BDM signals RESET* and BKGD inside the P&E BDM block. These pull-ups are not shown on the schematic.

BDM_PORT Header

An HCS(X)12 compatible BDM cable may be attached to the 6-pin BDM interface header (J2) if desired. Figure 2 below shows the pin-out for the BDM_PORT header.

Figure 2: BDM_PORT Header

See the MC9S12XHY Reference Manual for details

POWER

The DEMO9S12XHY256 may be powered from several sources. An option header allows selection between the various power inputs. For application development and debug, the board may be powered from the USB BDM. The 2.0mm, center-positive, barrel connector supports stand-alone operation and higher power requirements. Power may also be applied to connector J1 or the board may be configured to supply power from connector J1 to external circuitry. Use J1-1 and J1-3 to connect power to or source power from the demo board.

Use of LIN circuitry requires application of +12V at the barrel connector (J11) or though the LIN connector. Power applied at the LIN connector provides input to the on-board regulator and is selected in a similar manner as the barrel connector input.

CAUTION:

Damage to the board may result if voltages greater than +5.0V are applied at the connector J1 input.

Power Select

Power may be applied to the board through the integrated USB-BDM circuitry, a 2.0mm barrel connector, or through connector J1. Power selection is achieved using 2 selection headers: the PWR_SEL (JP9) option header and the VX_EN (JP10) option header.

PWR_SEL

The PWR_SEL option header (JP9) allows the user to select power input either from an external power source connected to the VIN connector or from the integrated USB-BDM. If using an external power source, input voltage should fall between +7V and +35V. However, external input voltage should be kept as low as possible to prevent the voltage regulator from becoming excessively hot. Figure 3 below details the PWR_SEL (JP9) header connections.

Figure 3: V_SEL Option Header

PWR_SEL Enable power to board from on-board regulator
VR1 USB

PWR_SEL Enable power to board from integrated USB-BDM
VR1 USB

Power from the integrated BDM is drawn from the USB bus and is limited to **500 mA**. This current limit accounts for the total current supplied over the USB cable to the BDM circuit, the target board, and any connected circuitry. Current drain in excess of 500 mA will violate the USB specification and will cause the USB bus to disconnect. This will cause the board to exhibit power cycling where the board appears to turn-on then off continually. Damage to the host PC or the target board may also result.

CAUTION:

When powered from the USB bus, do not exceed the 500mA maximum allowable current drain. Damage to the target board or host PC may result

VX_EN

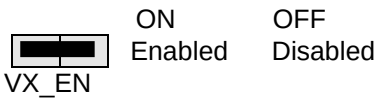
The VX_EN (JP10) option header is a 2-pin jumper that connects or disconnects input J1-1 directly to the target board voltage rail. J1-3 connects directly to the target board ground plane. Use of this feature requires a regulated input power source. This power input is decoupled to minimize noise but is not regulated or protected. Care should be exercised when using this feature; no protection is applied on this input and damage to the target board may result if excessive voltage is applied. Also, do not attempt to power the target board through this connector while also applying power through the USB-Multilink BDM or the PWR connector; damage to the board may result.

CAUTION:

Damage to the board may result if voltages greater than +5.5V are applied at the connector J1 input. Using the J1-1 and J1-3 input connects input voltage directly to the target board voltage rails.

Power may also be sourced to off-board circuitry through the J1 connector. The current supplied from the USB bus or the on-board regulator limits current available to external circuitry. Excessive current drain may damage the target board, the host PC USB hub, or the on-board regulator. Figure 4 below shows the VX_EN header option settings.

Figure 4: VX_EN Option Header



CAUTION:

Do not exceed available current from USB-BDM or on-board regulator when sourcing power through connector J1 to external circuitry.

RESET SWITCH

The RESET switch (SW6) applies an asynchronous RESET to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. A pull-up bias resistor allows normal MCU operation.

LOW VOLTAGE RESET

The MC9S12XHY256 utilizes an internal Low Voltage Detect (LVD) circuit. The LVD holds the MCU in reset until applied voltage reaches an appropriate level. The LVD also protect against under-voltage conditions. Consult the MC9S12XHY256 reference manual for details LVD operation.

CLOCK

The DEMO9S12XHY256 applies an 8MHz crystal oscillator for timing input. User application must configure the external timing input for proper operation. Refer to the MC9S12XHY Reference Manual for details on use and configuration of the external clock source.

COMMUNICATIONS

Communications options for the DEMO9S12XHY256 include serial RS-232, LIN bus, and CAN bus. Serial RS-232 communications is supported through a RS-232 physical layer device (PHY) and standard DB-9 connector, or through the integrated BDM. A high-speed, enhanced, LIN PHY provides LIN bus communications through a 2 x 2 Molex connector (pn 39-29-1048). A high-speed CAN PHY provides CAN bus communications through a 1 x 4 Molex connector (pn 39-30-3045).

The COM_SEL (JP3) option header connects the MCU SCI signal to either the LIN PHY or the RS-232 PHY. See Figure 7 below for jumper position options.

The JP11 option header enables serial communications through the integrated USB BDM. See Figure 8 below for jumper position options.

RS-232

The DEMO9S12XHY256 applies the MAX3387E, RS-232 transceiver to support serial communications. A right-angle, DB-9 connector allows attaching standard serial cables to the target board. A ferrite bead on shield ground provides conducted immunity protection for the board. Figure 5 below shows the SCI signal connections.

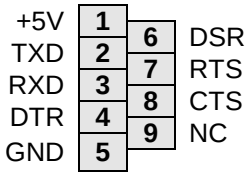
Figure 5: Serial Connections

MCU Port Signal	Transceiver Signal	DB-9 CONNECTOR	COMMENTS
	+5V	J8-1	
PS1/PWM7/TXD	TXD	J8-2	
PS0/PWM6/RXD	RXD	J8-3	
PR2/IOC1_6/KWR2	DTR	J8-4	CT1 (NC)
	GND	J8-5	
PR0IOC0_6/KWR0	DSR	J8-6	Pull-up
PR3/IOC1_7/KWR3	RTS	J8-7	CT2 (NC)
PR1/IOC0_7/KWR1	CTS	J8-8	Pull-up
	TP2	J8-9	
PAD00/AN00/KWAD0	INVALID*		CT3 (NO)
PAD02/AN02/KWAD2	FORCEOFF*		CT4 (NC)

COM Connector

A standard 9-pin Dsub connector provides external connections for the SCI port. The Dsub shell is connected to board ground through a ferrite bead providing noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 6: COM1 Connector

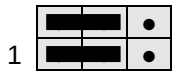


Female DB9 connector that interfaces to the MCU internal SCI0 serial port via the RS-232 transceiver. Handshaking signals connect to the MCU GPIO inputs via the RS-232 transceiver.

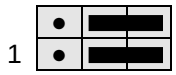
COM_SEL

The COM_SEL (JP3) option header connects the MCU SCI port to either the SCI PHY or the USB-BDM connection. Figure 7 below shows the option jumper configuration for the COM_SEL option header.

Figure 7: COM_SEL Option Header



Connects target MCU SCI port to LIN PHY to enable LIN bus communications

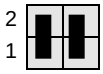


Connects target MCU SCI port to RS-232 PHY to enable serial communications

USB Serial Link

The integrated USB-BDM provides a serial link from the target MCU to the host PC through the a utility application. Refer to the P&E Multilink documentation for further details. This signal path is enabled using option jumper JP11, BCOM_EN. Figure 8 below shows the configuration for the JP11 option header.

Figure 8: BCOM_EN Option Header



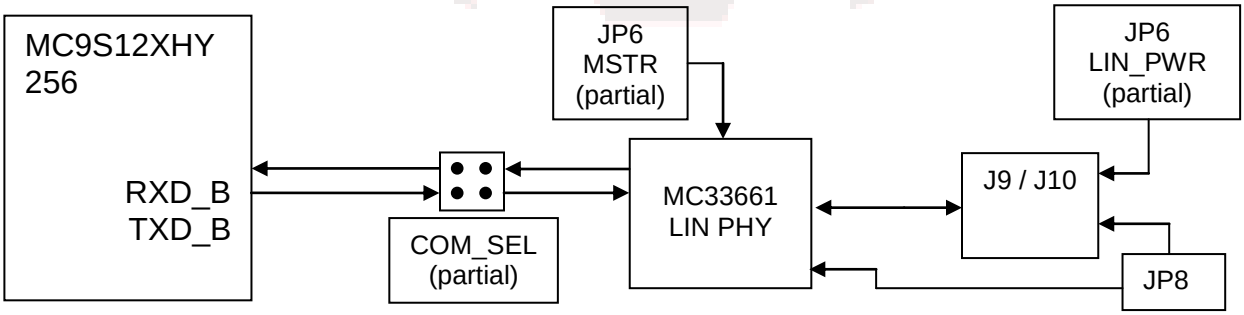
Enables serial communications through the integrated USB BDM. Remove shunts to disable serial comm. through the USB BDM.

NOTE: These option jumpers must be removed to enable SCI communications through the COM port.

LIN Port

The DEMO9S12XHY256 applies the MC33661 LIN bus physical layer device (PHY) to support LIN communications. The PHY may be configured as a Master or Slave node on the LIN bus. LIN connectors J9 & J10 are configured in parallel to support pass-thru signaling if needed. Connector J9 is not installed in default configurations. Figure 9 shows the LIN block diagram.

Figure 9: LIN Block Diagram



The LIN interface provides optional features of slew rate control, network supply, and wake up option. Refer to the MC33661 Reference Manual for detail on PHY functionality. The following sections detail functionality for LIN option jumpers.

LIN Enable

The LIN PHY is enabled by default. The LIN PHY may be disabled by connecting the test point TP3 to GND.

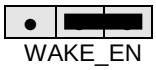
LIN COM Input

LIN inputs RX and TX are selectable using the COM_EN option header. Refer to Figure 7 above for details on configuring this header.

Wake Option

Option header JP9 allows a LIN Master node to wake a Slave node if enabled. A low-to-high transition wakes the Slave device from sleep mode.

Figure 10: Option Header



1 LIN Network Master can WAKE LIN device

1 J9-2 & J10-2 connect to GND

LIN_PWR Option

The LIN_PWR (JP6-1/JP6-2) option jumper connects pin 1 of both LIN connectors to the +V input. In Master mode, this option may be used to power the LIN bus. This option requires +12V be applied at connector J11. In Slave mode, this option allows slave device to draw power from the LIN network. For Slave mode configuration, external power should not be applied at the barrel connector (J11). LIN_PWR is enabled by installing a shunt from JP6-1 to JP6-2. Refer to Figure 11 below.

CAUTION:

If the target board draws power from the LIN bus in Slave mode, do not apply external power to connector J11. Damage to the board may result.

NOTE:

If the target board powers the LIN bus in Master mode, +12V must be applied externally at connector J11.

MSTR Option

The MSTR option jumper allows the LIN transceiver to be configured for master mode functionality. Master mode may also be set using the INH pin. Refer to the MC33661 device datasheet for details on use and configuration. Refer to Figure 11 below.

Figure 11: LIN Option Header

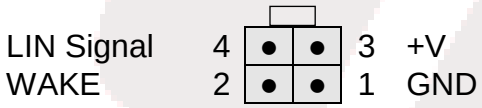
Connects +V input to LIN bus for Slave node configuration
Enables LIN Master configuration

NOTE: LIN PHY may also be configured as a Master Node using the INH pin. Refer to the LIN PHY data sheet for details.

LIN Connector

The DEMO9S12XHY256 supports two, 2 x 2 Molex connectors to interface to the LIN bus. One connector (J9) is not installed in default configurations.

Figure 12: LIN Connector



Front View – Looking into Connector

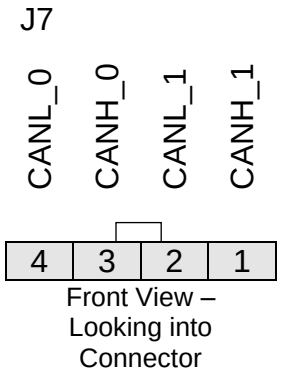
NOTE: LIN Port Connector – Molex 39-29-1048
Mates with; Housing – Molex 39-01-2040, Pin – Molex 39-00-0036

CAN Port

Two, TJA1040T, High-Speed CAN physical layer transceiver (PHY) is applied to support CAN bus communications. A 4-pos, 4.22mm MOLEX connector interfaces to external CAN cabling.

Differential input CAN signals, for both CAN channels, are terminated with 120 ohms. Option headers, JP13 and JP15 allow the user to optionally disconnect signal termination. Avalanche diodes protect the CAN PHY from voltage surges on the input differential signal lines. Figure 13 below shows the CAN connector pin-out.

Figure 13: CAN_PORT



NOTE: CAN Port Connector – Molex 39-30-3045
Mates with; Housing – Molex 39-01-4040, Pin – Molex 39-00-0036

CAN Termination Enable

CAN bus termination of 120 ohm with virtual ground is applied to the differential CAN signals on both channels. The SPLIT output from each PHY is connected to the virtual ground providing common-mode stabilization. The differential CAN bus signal termination may be removed using option header JP13 or JP15. To prevent signal corruption, both option jumpers **must** be installed or both option jumpers **must** be removed. The CAN bus should not be operated with only 1 signal termination applied.

NOTE:

To prevent signal corruption both shunts should be either ON or OFF

Figure 14: CAN Termination Enable

2 Connects CANL termination
4 Connects CANH termination

NOTE: JP13 applies termination to CAN0 while JP15 applies termination to CAN1. JP15 is similar to JP13.

Standby Mode

The CAN PHY is configured for normal mode by default. To enable standby (STB) moved, apply a high logic level at test point TP1.

LCD

The DEMO9S12XHY256 applies a 4 x 40 custom LCD glass connected directly to the target MCU. Refer to the MC9S12XHY256 Reference Manual for details on use and configuration of the LCD module. The LCD data sheet can be found on the Support CD received with the board or at the Axiom Manufacturing Support web site (www.axman.com/support) . Refer to the MC9S12XHY Reference Manual for details on configuration and use of the LCD module. Figure 15 at the end of this document shows the signal connections between the target MCU and the LCD.

LCD Connections

The figure below shows the connections between the target MCU and the GD-5506P Custom LCD Glass.

Figure 15: LCD Connections

MCU PIN	SIGNAL	LCD PIN
100	BP3/PB7	1
101	BP2/PB6	2
102	BP1/PB5	3
103	BP0/PB4	4
97	FP39/PB3	5
96	FP38/PB2	6
95	FP37/PB1	7
94	FP36/PA7	8
93	FP35/PA6	9
92	FP34/PA5	10
91	FP33/PA4	11
90	FP32/API_EXTCLK/XCLKS/PA3	12
89	FP31/PA2	13
88	FP30/XIRQ*/PA1	14
87	FP29/IRQ*/PA0	15
86	FP28/PB0	16
85	FP27/PR7	17
84	FP26/PH7	18
83	FP25/PH6	19
76	FP24/PH5	20
75	FP23/PH4	21
66	FP22/SDA/SS*/PH3	22
65	FP21/SCK/ECLK/PH2	23
64	FP20/MOSI/TXD1/PH1	24
29	FP0/PWM0/PP0	25
30	FP1/PWM1/PP1	26
31	FP2/PWM2/PP2	27
32	FP3/PWM3/PP3	28
33	FP4/PWM4/PP4	29
34	FP5/PWM5/PP5	30
35	FP6/PWM6/PP6	31
36	FP7/PWM7/PP7	32
52	FP8/KWT0/IOC1_4/PT0	33
53	FP9/KWT1/IOC1_5/PT1	34
54	FP10/KWT2/IOC1_6/PT2	35
55	FP11/KWT3/IOC1_7/PT3	36
56	FP12/KWR4/PR4	37
67	FP13/KWT4/IOC0_4/PT4	38
68	FP14/KWT5/IOC0_5/PT5	39
69	FP15/KWT6/IOC0_6/PT6	40
60	FP16/KWT7/IOC0_7/PT7	41
61	FP17/SDA/PR5	42
62	FP18/SCL/PR6	43
63	FP19/RXD1/MISO/PH0	44

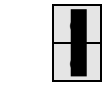
MOTOR CONTROLLER

The MC9S12XHY256 provides multiple PWM Motor Controller outputs suitable to drive instrument stepper motors or other load requiring a PWM signal. The Motor Controller output consists of 16 signals which may be arranged as 8 channels of half H-bridge drivers or 4 channels of full/dual H-bridge drivers. All outputs are available on option headers MOTOR0/1 (J3) or MOTOR2/3 (J5). Refer to the DEMO9S12XHY256 Schematic for pin locations. Refer to the MC9S12XHY Reference Manual for details on use and capability of the Motor Controller module.

MC Power Input

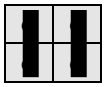
Motor controller power input is enabled using option jumpers VDDM (JP1), VSSM (JP2), and JP4. The VDDM and VSSM option jumpers allow the use of alternate input voltage rails if desired. The J4 option header currently serves no purpose; do not move jumpers from default postion. connects and disconnects power input to MCU motor controller. Although the MCU provides 2 VDDM and 2 VSSM motor controller inputs, the connects these inputs at the J4 option header.

Figure 16: Motor Power Input



JP1 VDDM — Enables power input to VDDM filter circuit. Allows use of alternate voltage input if desired

JP2 VSSM — Enables power input to VSSM filter circuit. Allows use of alternate voltage input if desired

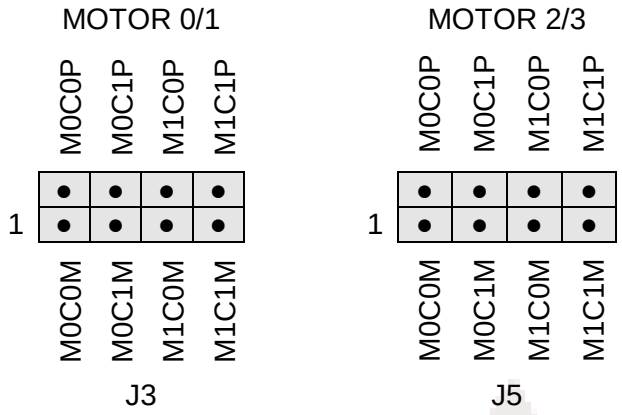


JP4 — Do not move jumpers from default position.

MC PWM Output

Motor Controller PWM output is accessible on connector headers J3 and J5. Each output header provides access to 2 motor output channels. Figure 17 below shows the pin-out connections for connectors MORTO0/1 (J3) and MORTOR2/3 (J5).

Figure 17: Motor Controller I/O PORT



MCU I/O PORT

The MCU I/O PORT connector provides access to the MC9S12XHY256 I/O signals. Figure 18 below show the pin-out for the MCU I/O connector.

Figure 18: MCU I/O PORT

J1

VDD	1	2	FP29/IRQ*/PA0
VSS	3	4	RESET
TXD/PWM7/PS1	5	6	BKGD/MODC
RXD/PWM6/PS0	7	8	FP12/PR4
KWR0/IOC0_6/RXCAN/PR0	9	10	KWAD0/AN00/PAD00
KWR1/IOC0_7/TXCAN/PR1	11	12	KWAD1/AN01/PAD01
KWR2/IOC1_6/PR2	13	14	KWAD2/AN02/PAD02
KWR3/IOC1_7/PR3	15	16	KWAD3/AN03/PAD03
KWS5/MOSI/PWM1/PS5	17	18	KWAD4/AN04/PAD04
MISO/SCL/PWM0/PS4	19	20	KWAD5/AN05/PAD05
KWS6/SCK/PWM2/PS6	21	22	KWAD6/AN06/PAD06
SS*/SDA/PWM3/PS7	23	24	KWAD7/AN07/PAD07
FP33/PA4	25	26	KWS3/TXCAN0/PWM5/PS3
FP34/PA5	27	28	KWS2/RXCAN0/PWM4/PS2
FP35/PA6	29	30	FP23/PH4
FP36/PA7	31	32	FP24/PH5
FP28/PB0	33	34	FP25/PH6
FP37/PB1	35	36	FP26/PH7
FP38/PB2	37	38	FP17/SDA/PR5
FP39/PB3	39	40	FP18/SCL/PR6

USER I/O

User I/O includes 1 potentiometer, 4 push button switches, and 4 green LEDs for user I/O. The USER (JP14) option header enables or disables each User I/O function individually. The sections below provide details on user I/O. Figure 19 below shows the USER jumper settings.

Potentiometer

The DEMO9S12XHY256 target board provides a single-turn, 5K, ohm potentiometer (POT) to simulate analog input. The POT is connected to an ATD input. The POT is decoupled to minimize noise transients during adjustment. Figure 19 below shows the USER jumper settings.

LED's

The DEMO9S12XHY256 target board provides 4, green, LEDs for output indication. Each LED is configured for active-low operation. A series, current-limit resistor prevents excessive diode current. Figure 19 below shows the USER jumper settings.

Pushbutton Switches

The DEMO9S12XHY256 provides 4 push-button switches for user input. Each push-button switch is configured for active-low operation. No bias is applied to these push-button inputs. Use of target MCU internal pull-ups is required for proper operation. Figure 19 below shows the USER jumper settings.

Figure 19: User Option Header

	JP14 USER		Signal	ON (default)	OFF
LED1	•	•	PR0/IOC0_6/KWR0	Enabled	Disabled
LED2	•	•	PR1/IOC0_7/KWR1	Enabled	Disabled
LED3	•	•	PR2/IOC1_6/KWR2	Enabled	Disabled
LED4	•	•	PR3/IOC1_7/KWR3	Enabled	Disabled
SW1	•	•	PAD04/AN04/KWAD4	Enabled	Disabled
SW2	•	•	PAD05/AN05/KWAD5	Enabled	Disabled
SW3	•	•	PAD06/AN06/KWAD6	Enabled	Disabled
SW4	•	•	PAD07/AN07/KWAD7	Enabled	Disabled
POT	•	•	PAD00/AN00/KWAD0	Enabled	Disabled

ACRONYMS

BDM	Background Debug Mode
ESD	Electro-static Discharge
LED	Light Emitting Diode
MCU	Microcontroller Unit
NC	Normally Closed
NO	Normally Open
PHY	Physical Layer Transceiver
pn	Part Number
PN	Part Number
POT	Potentiometer
RM	Reference Manual
STB	Standby

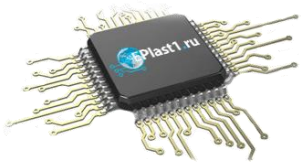
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.