Freescale Semiconductor
Technical Data

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√RoHS

RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

These 32 W RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1995 MHz.

A2T18S160W31SR3
A2T18S160W31GSR3

1805–1995 MHz, 32 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTORS

1800 MHz

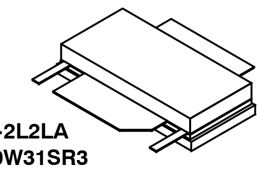
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, P_{out} = 32 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	19.6	32.1	7.2	–34.7	–12
1840 MHz	20.1	32.1	7.2	–35.0	–17
1880 MHz	19.9	31.6	7.2	–35.4	–12

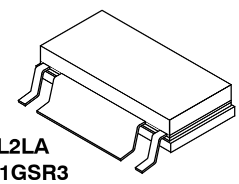
1900 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, P_{out} = 32 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

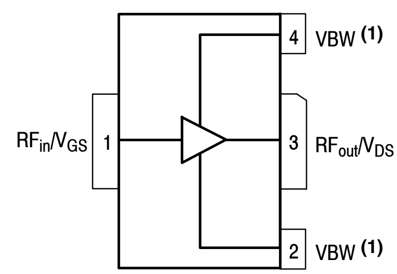
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1930 MHz	21.0	32.2	7.5	–34.4	–17
1960 MHz	21.3	32.2	7.4	–34.4	–19
1995 MHz	21.6	32.9	7.1	–33.9	–12



NI-780S-2L2LA
A2T18S160W31SR3



NI-780GS-2L2LA
A2T18S160W31GSR3



(Top View)

Figure 1. Pin Connections

1. Device can operate with the V_{DD} current supplied through pin 2 or pin 4 alone.

Features

- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Optimized for Doherty Applications

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	185 1.0	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 32 W CW, 28 Vdc, I_{DQ} = 1000 mA, 1840 MHz	$R_{\theta JC}$	0.36	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 160 μAdc)	$V_{GS(th)}$	1.2	1.8	2.2	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1000 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.6	3.1	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.6 Adc)	$V_{DS(on)}$	0.1	0.14	0.3	Vdc

Functional Tests (4,5) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, P_{out} = 32 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	18.5	19.9	21.5	dB
Drain Efficiency	η_D	27.0	31.6	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.7	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	–35.4	–32.0	dBc
Input Return Loss	IRL	—	–12	–6.5	dB

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. Part internally matched both on input and output.
5. Measurements made with device in straight lead configuration, before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.

(continued)

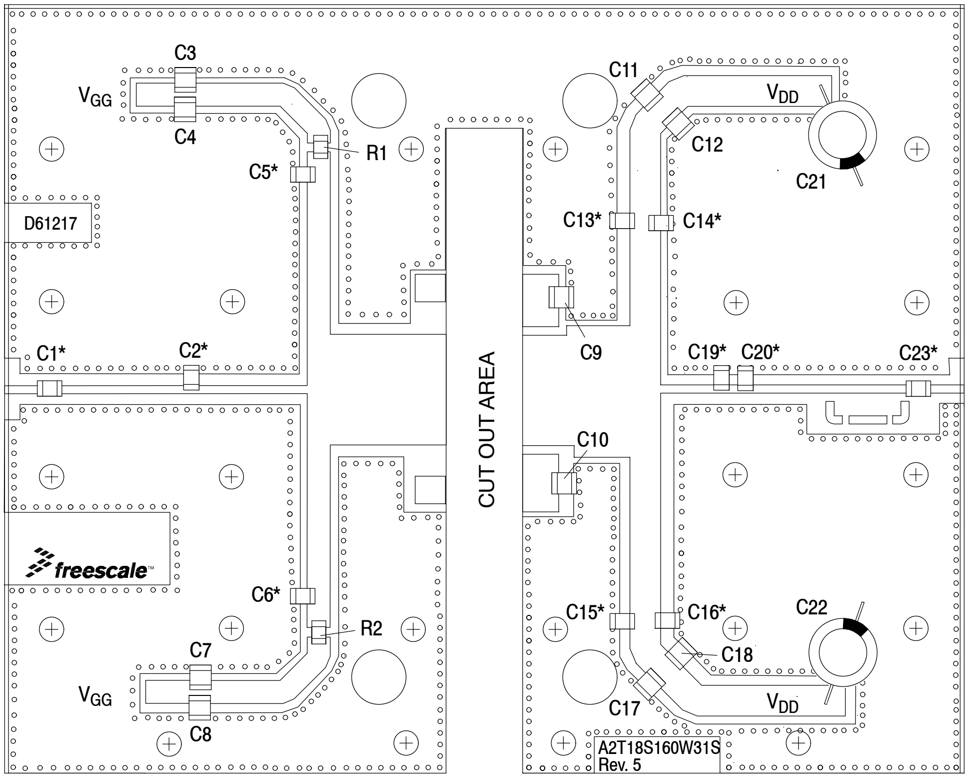
Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1000 mA, f = 1840 MHz					
VSWR 10:1 at 32 Vdc, 173 W CW Output Power (3 dB Input Overdrive from 129 W CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	129	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range.)	Φ	—	–15	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	110	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 32 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.006	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) (1)	ΔP1dB	—	0.005	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T18S160W31SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	NI-780S-2L2LA
A2T18S160W31GSR3		NI-780GS-2L2LA

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



*C1, C2, C5, C6, C13, C14, C15, C16, C19, C20, and C23 are mounted vertically.

Figure 2. A2T18S160W31SR3 Test Circuit Component Layout

Table 6. A2T18S160W31SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C13, C14, C15, C16, C23	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C2	1.7 pF Chip Capacitor	ATC100B1R7BT500XT	ATC
C3, C4, C7, C8, C9, C10, C11, C12, C17, C18	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C5, C6	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C19	2.2 pF Chip Capacitor	ATC100B2R2JT500XT	ATC
C20	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C21, C22	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	2.37 Ω, 1/4 W Chip Resistors	CRCW12062R37FNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D61217	MTL

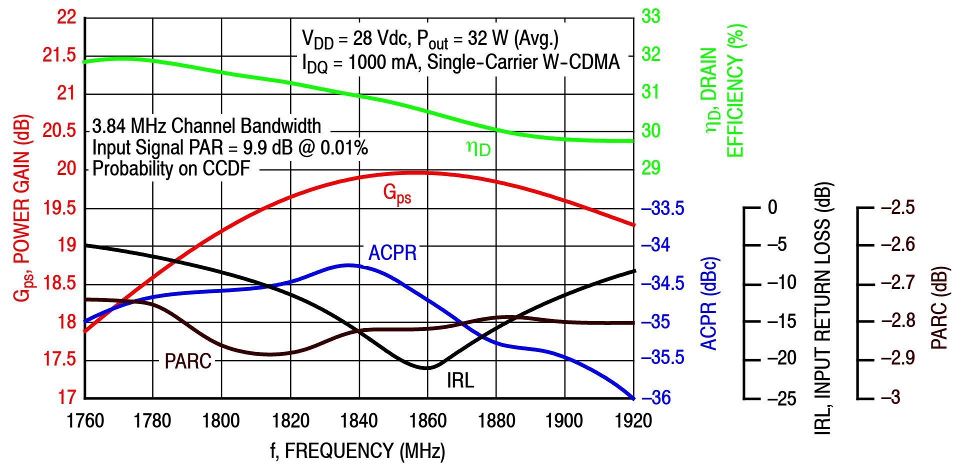


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 32 Watts Avg.

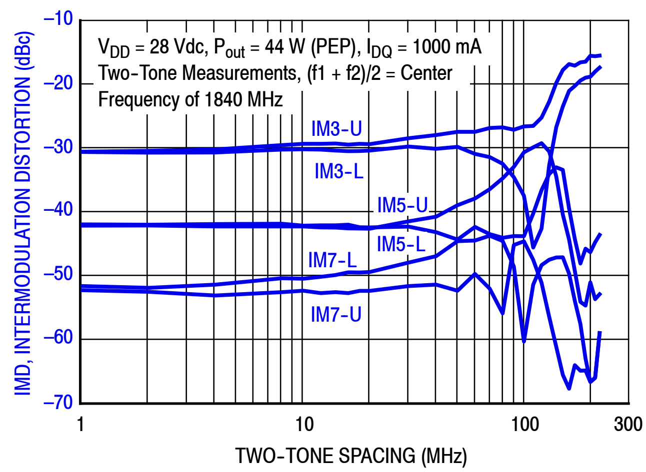


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

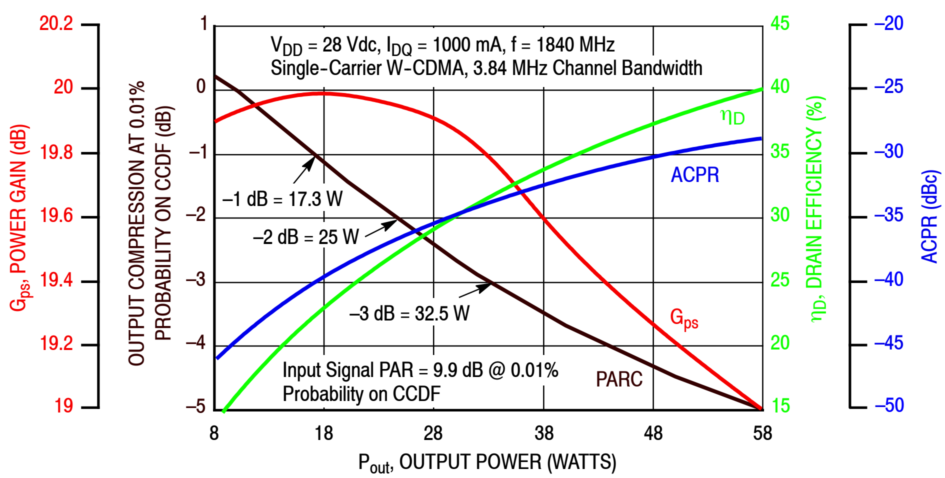


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

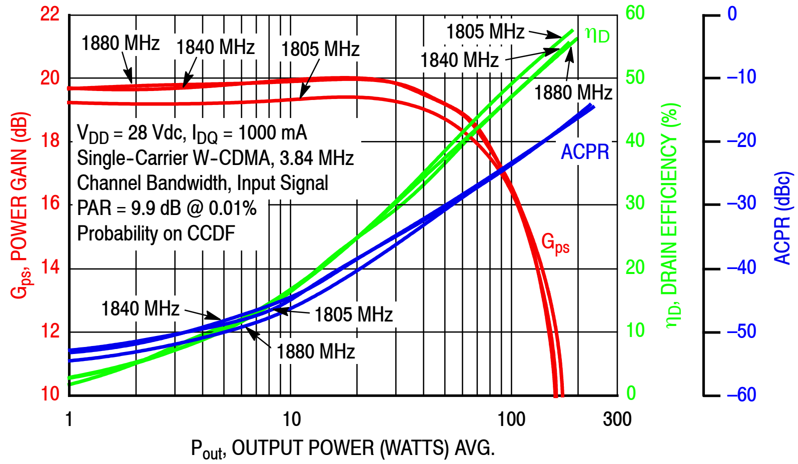


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

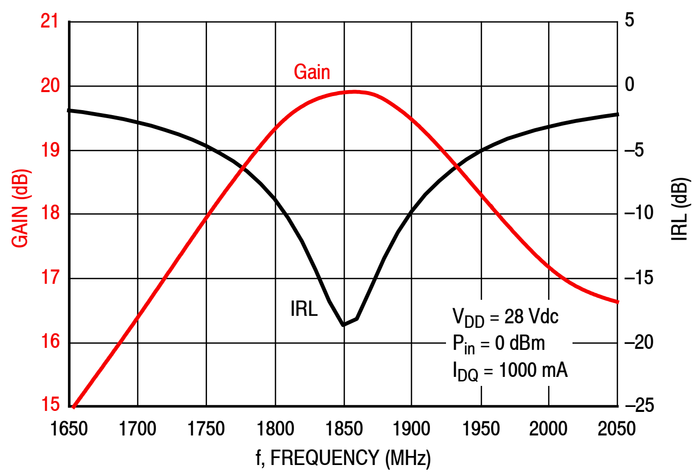


Figure 7. Broadband Frequency Response

Table 7. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1041 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.77 – j2.95	0.81 + j3.12	1.85 – j3.49	19.0	51.9	156	50.2	–9
1840	0.80 – j3.23	0.93 + j3.34	1.93 – j3.61	19.0	52.0	157	50.4	–11
1880	1.00 – j3.43	1.14 + j3.63	2.03 – j3.75	19.0	51.8	150	49.3	–11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.77 – j2.95	0.75 + j3.23	1.89 – j3.56	17.0	53.0	199	54.2	–13
1840	0.80 – j3.23	0.86 + j3.47	1.96 – j3.58	17.0	53.0	200	55.0	–15
1880	1.00 – j3.43	1.05 + j3.80	2.03 – j3.43	17.4	52.9	197	56.3	–15

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

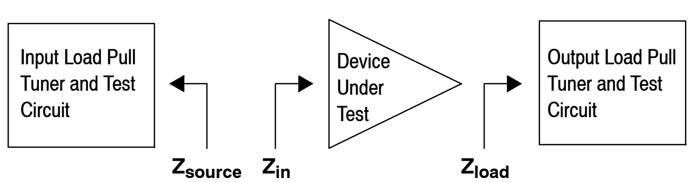
Table 8. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1041 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.77 – j2.95	0.82 + j3.23	3.67 – j0.62	22.5	49.3	85	61.0	–10
1840	0.80 – j3.23	0.87 + j3.45	2.54 – j0.27	23.1	49.3	85	62.6	–11
1880	1.00 – j3.43	1.07 + j3.82	2.12 – j0.54	23.0	49.7	93	66.7	–14

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.77 – j2.95	0.81 + j3.37	3.49 – j0.50	20.6	50.6	115	67.0	–16
1840	0.80 – j3.23	0.90 + j3.56	2.96 – j0.69	20.6	50.9	124	68.1	–17
1880	1.00 – j3.43	1.12 + j3.91	2.66 – j0.75	20.7	51.0	126	70.4	–20

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

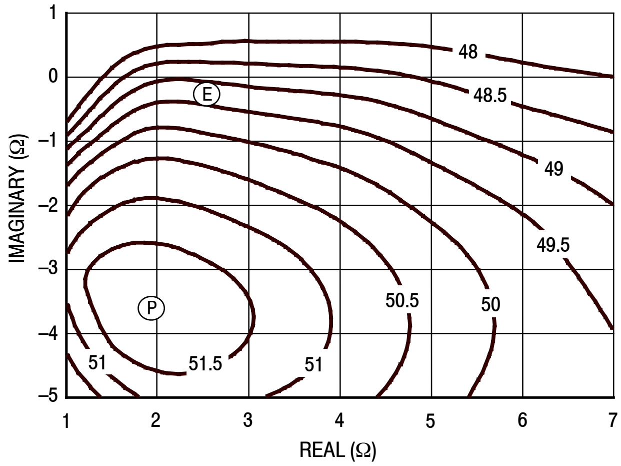


Figure 8. P1dB Load Pull Output Power Contours (dBm)

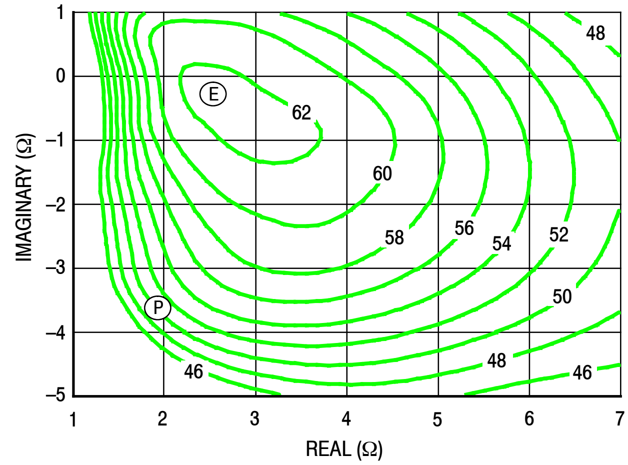


Figure 9. P1dB Load Pull Efficiency Contours (%)

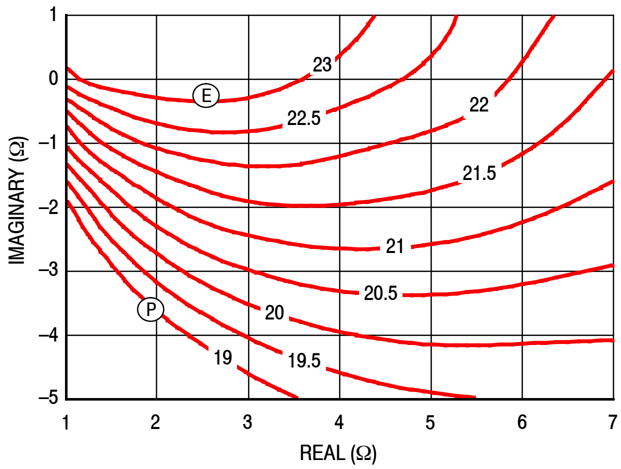


Figure 10. P1dB Load Pull Gain Contours (dB)

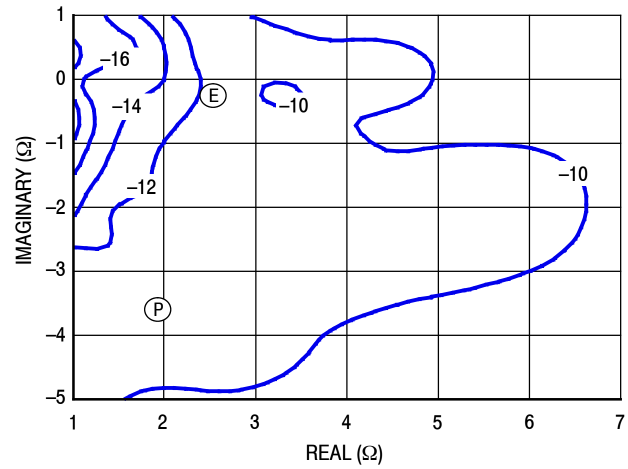


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power

E = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

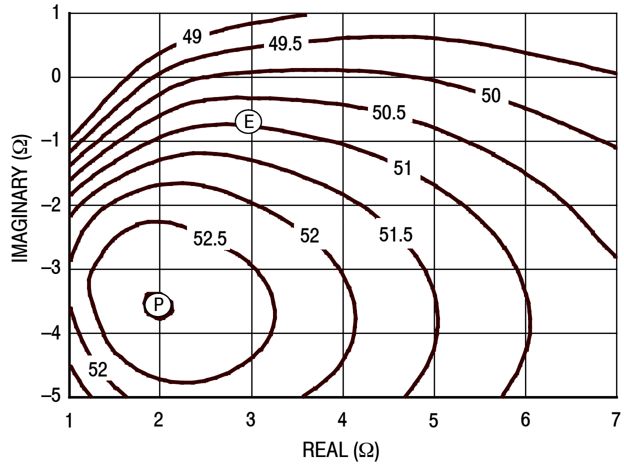


Figure 12. P3dB Load Pull Output Power Contours (dBm)

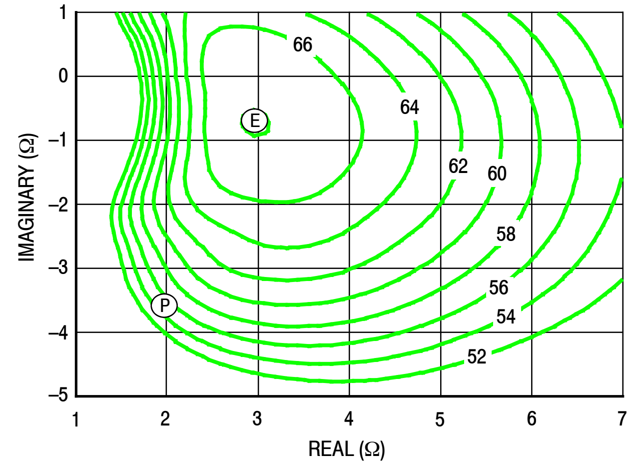


Figure 13. P3dB Load Pull Efficiency Contours (%)

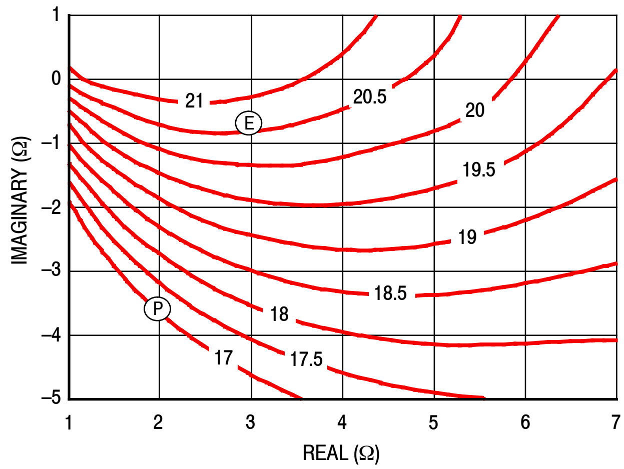


Figure 14. P3dB Load Pull Gain Contours (dB)

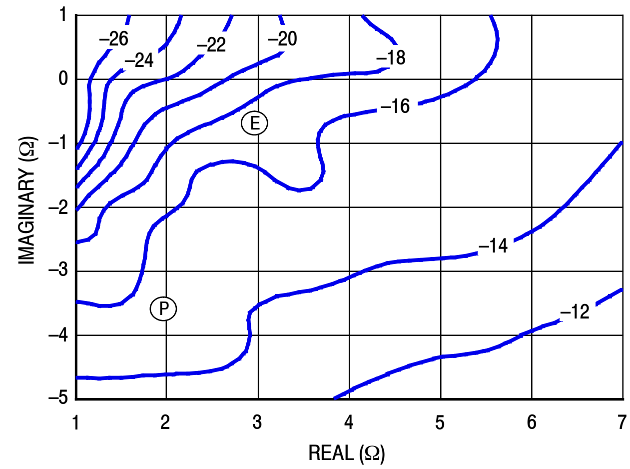
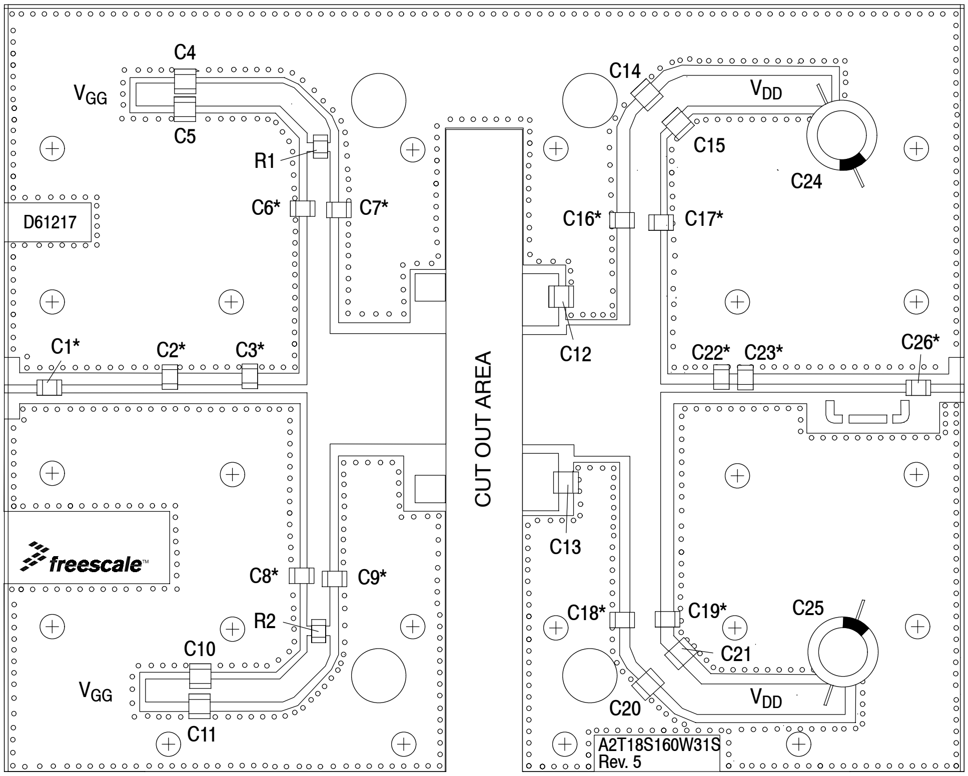


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power



*C1, C2, C3, C6, C7, C8, C9, C16, C17, C18, C19, C22, C23, and C26 are mounted vertically.

Figure 16. A2T18S160W31SR3 Test Circuit Component Layout — 1930–1995 MHz

Table 9. A2T18S160W31SR3 Test Circuit Component Designations and Values — 1930–1995 MHz

Part	Description	Part Number	Manufacturer
C1, C6, C7, C8, C9, C16, C17, C18, C19, C26	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C2	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C3	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C4, C5, C10, C11, C12, C13, C14, C15, C20, C21	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C22	2.2 pF Chip Capacitor	ATC100B2R2JT500XT	ATC
C23	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C24, C25	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	2.37 Ω, 1/4 W Chip Resistors	CRCW12062R37FNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D61217	MTL

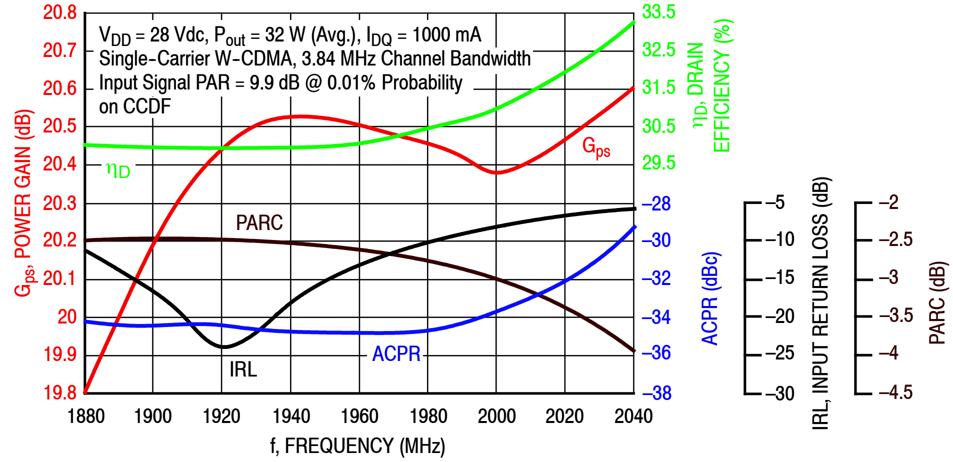


Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 32 Watts Avg.

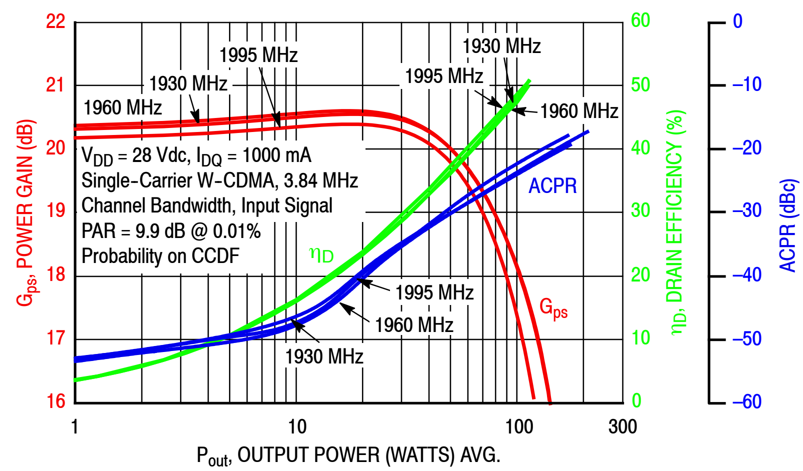


Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

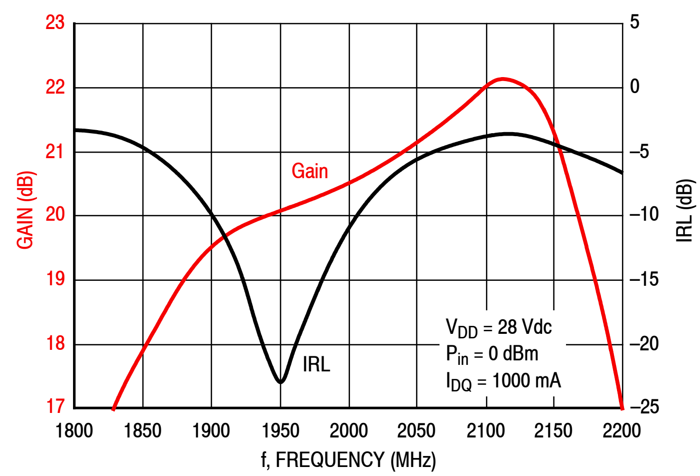


Figure 19. Broadband Frequency Response

Table 10. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1044 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.28 – j3.84	1.45 + j4.15	1.49 – j2.77	20.3	52.2	166	56.2	–10
1960	1.53 – j4.20	1.80 + j4.46	1.49 – j2.90	20.4	52.4	173	57.9	–11
1995	2.15 – j4.41	2.49 + j4.79	1.54 – j3.27	20.4	52.3	170	55.2	–12

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.28 – j3.84	1.43 + j4.30	1.70 – j3.10	18.1	53.3	212	60.1	–16
1960	1.53 – j4.20	1.80 + j4.66	1.70 – j3.17	18.2	53.4	217	61.6	–17
1995	2.15 – j4.41	2.53 + j5.08	1.66 – j3.36	18.3	53.2	211	59.4	–17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

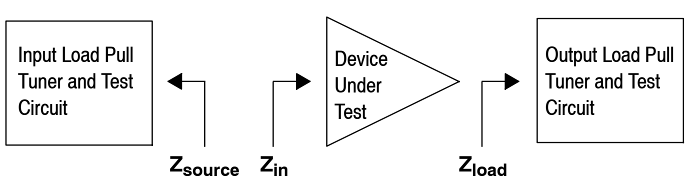
Table 11. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1044 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.28 – j3.84	1.51 + j4.28	1.85 – j1.07	23.4	50.1	103	68.4	–15
1960	1.53 – j4.20	1.91 + j4.57	1.81 – j1.49	23.1	50.7	118	70.3	–16
1995	2.15 – j4.41	2.69 + j4.90	1.75 – j1.77	23.1	50.6	114	66.1	–16

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.28 – j3.84	1.55 + j4.38	2.26 – j1.34	20.9	51.5	142	71.9	–21
1960	1.53 – j4.20	2.03 + j4.74	2.05 – j1.25	21.3	51.2	130	73.0	–24
1995	2.15 – j4.41	2.78 + j5.10	1.96 – j1.87	20.9	51.6	145	69.3	–23

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 1960 MHz

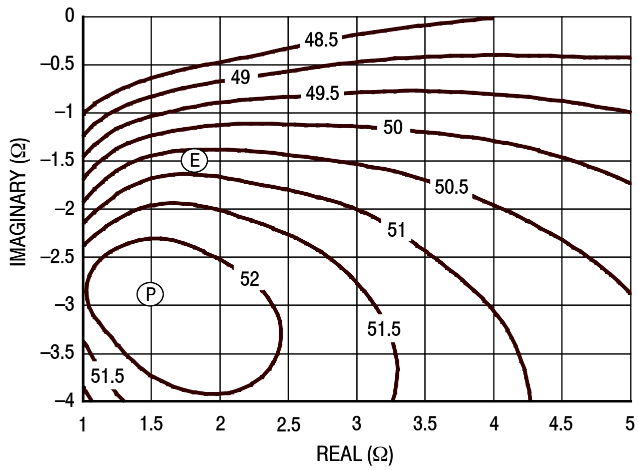


Figure 20. P1dB Load Pull Output Power Contours (dBm)

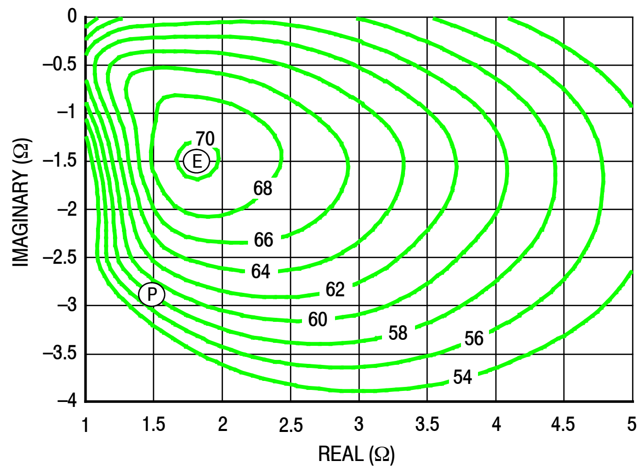


Figure 21. P1dB Load Pull Efficiency Contours (%)

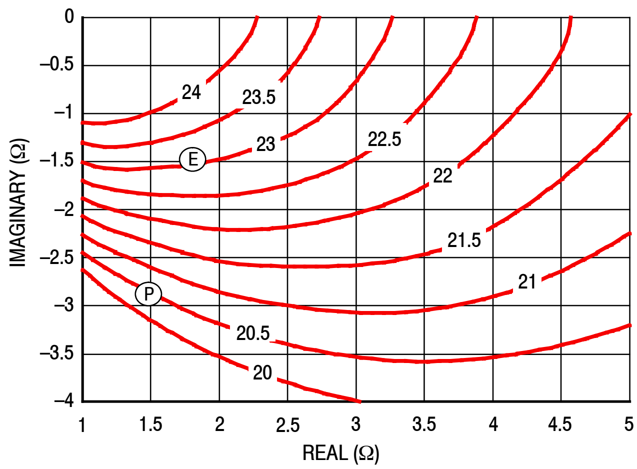


Figure 22. P1dB Load Pull Gain Contours (dB)

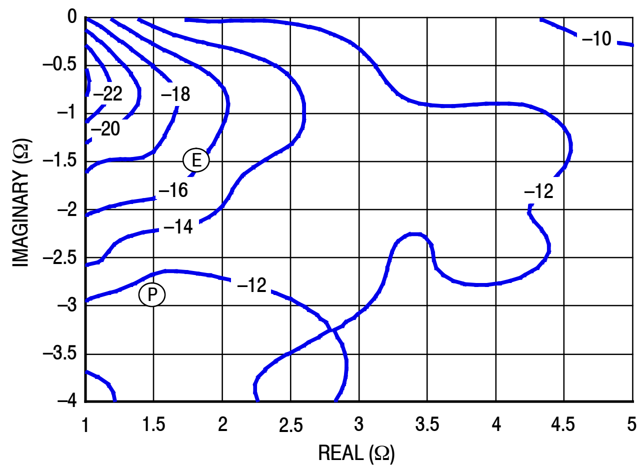


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1960 MHz

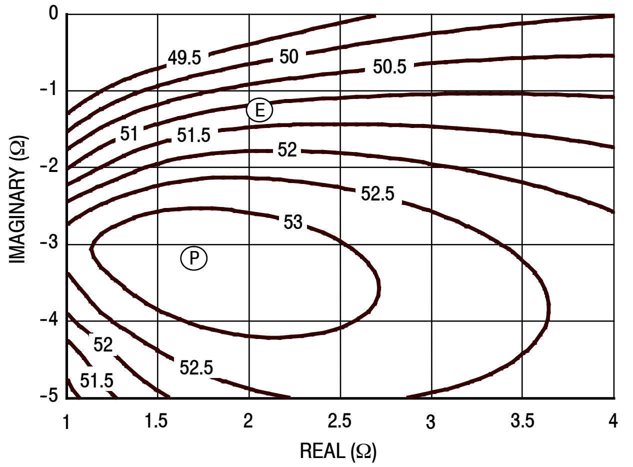


Figure 24. P3dB Load Pull Output Power Contours (dBm)

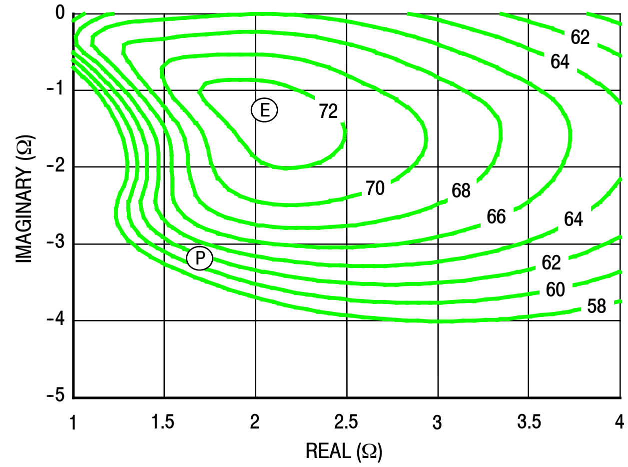


Figure 25. P3dB Load Pull Efficiency Contours (%)

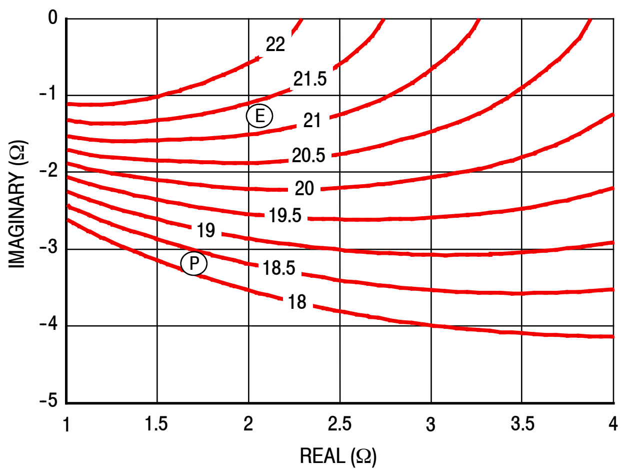


Figure 26. P3dB Load Pull Gain Contours (dB)

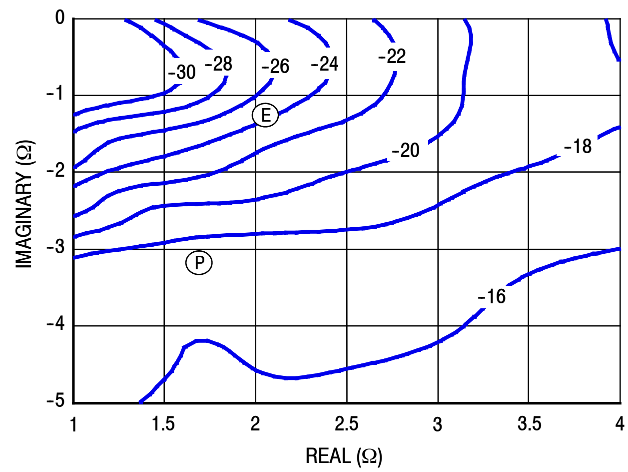


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

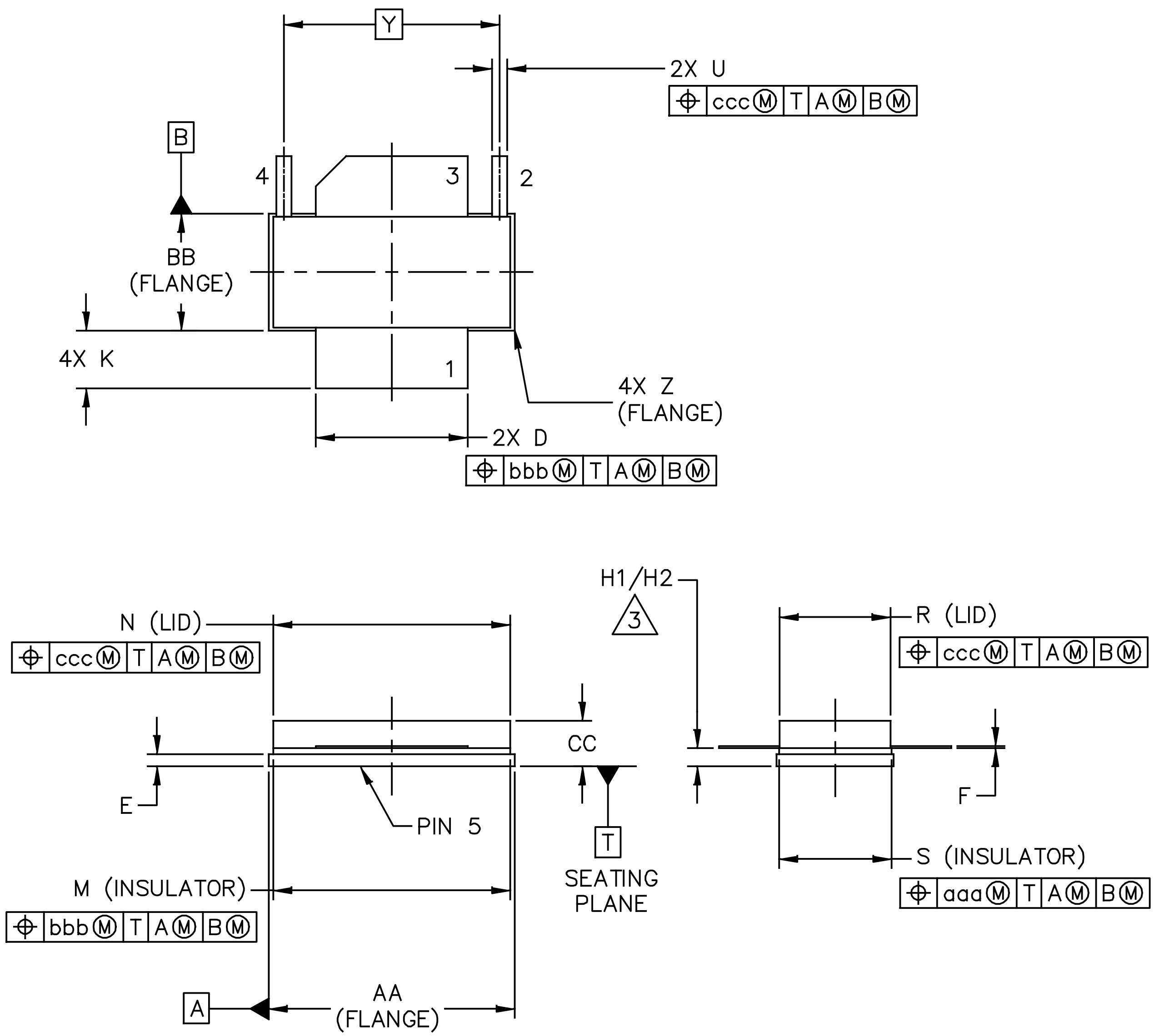
Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 1960 MHz



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TITLE: NI–780S–2L2LA	DOCUMENT NO: 98ASA00658D	REV: 0
	STANDARD: NON–JEDEC	
		05 DEC 2014

NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM THE FLANGE TO CLEAR THE EPOXY FLOW OUT REGION PARALLEL TO DATUM B. H1 APPLIES TO PINS 1 & 3. H2 APPLIES TO PINS 2 & 4.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.045	.055	1.14	1.40
D	.495	.505	12.57	12.83	Y	.710 BSC		18.03 BSC	
E	.035	.045	0.89	1.14	Z	R.000	R.040	R0.00	R1.02
F	.003	.007	0.08	0.18	aaa	.005		0.13	
H1	.057	.067	1.45	1.70	bbb	.010		0.25	
H2	.054	.070	1.37	1.78	ccc	.015		0.38	
K	.170	.210	4.32	5.33					
M	.774	.786	19.66	19.96					
N	.772	.788	19.61	20.02					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI−780S−2L2LA	DOCUMENT NO: 98ASA00658D	REV: 0
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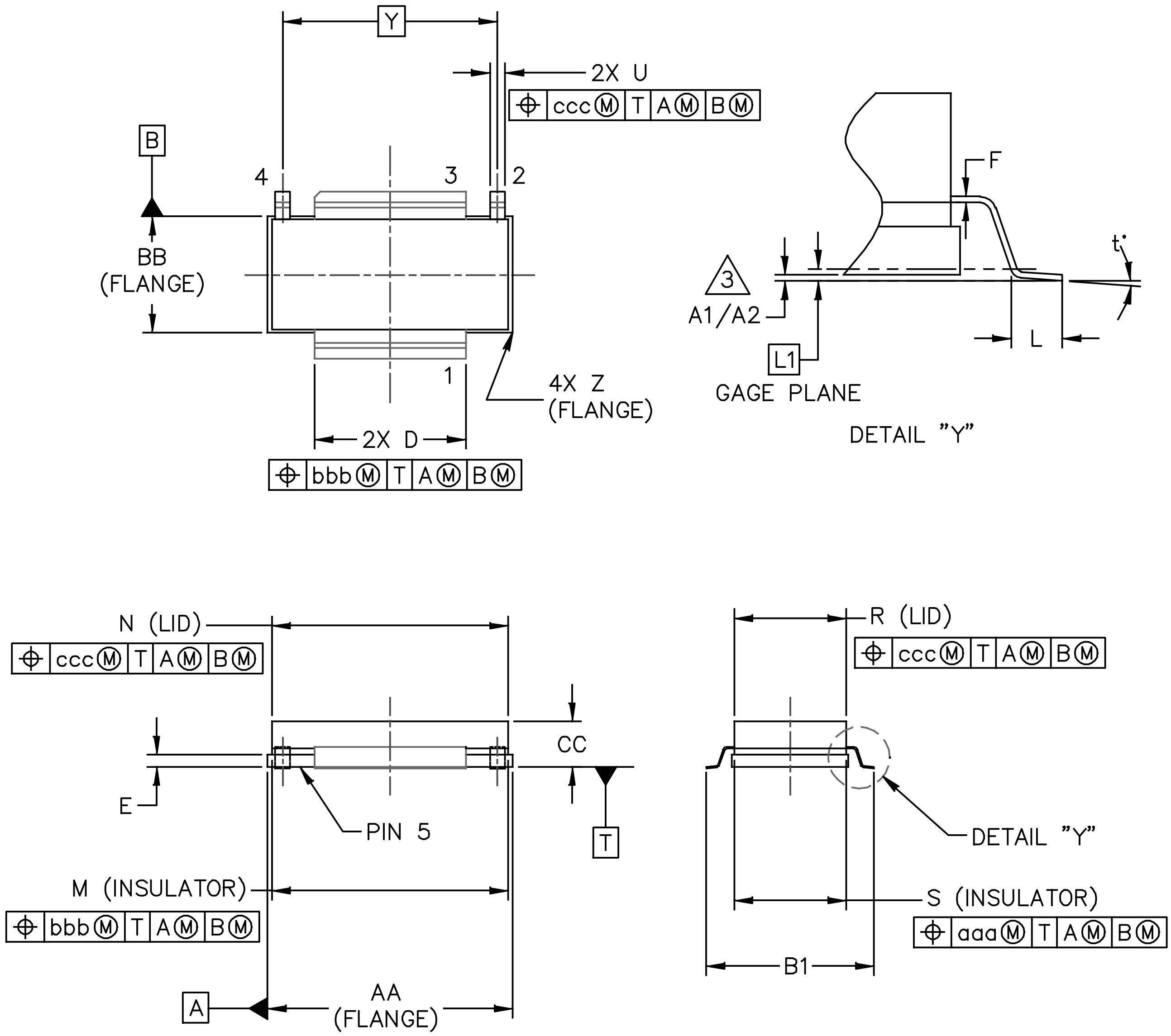

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TITLE: NI–780GS–2L2LA	DOCUMENT NO: 98ASA00624D	REV: 0
	STANDARD: NON–JEDEC	
		05 DEC 2014

NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSION A1/A2 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM. A1 APPLIES TO PINS 1 AND 3. A2 APPLIES TO PINS 2 AND 4.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
A1	.002	.008	0.05	0.20	S	.365	.375	9.27	9.53
A2	.002	.008	0.05	0.20	U	.045	.055	1.14	1.40
BB	.380	.390	9.65	9.91	Y	.710 BSC		18.03 BSC	
B1	.546	.562	13.87	14.27	Z	R.000	R.040	R0.00	R1.02
CC	.125	.170	3.18	4.32	t°	0°	8°	0°	8°
D	.495	.505	12.57	12.83	aaa	.005		0.13	
E	.035	.045	0.89	1.14	bbb	.010		0.25	
F	.003	.007	0.08	0.18	ccc	.015		0.38	
L	.038	.046	0.97	1.17					
L1	.010 BSC		0.25 BSC						
M	.774	.786	19.66	19.96					
N	.772	.788	19.61	20.02					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI–780GS–2L2LA	DOCUMENT NO: 98ASA00624D	REV: 0
	STANDARD: NON–JEDEC	
		05 DEC 2014

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2015	• Initial Release of Data Sheet

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