KSZ8081MNX/KSZ8081RNB

10Base-T/100Base-TX Physical Layer Transceiver

Data Sheet Rev. 1.0

General Description

The KSZ8081 is a single-supply 10Base-T/100Base-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081 is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core.

The KSZ8081MNX offers the Media Independent Interface (MII) and the KSZ8081RNB offers the Reduced Media Independent Interface (RMII) for direct connection with MII/RMII-compliant Ethernet MAC processors and switches.

A 25MHz crystal is used to generate all required clocks, including the 50MHz RMII reference clock output for the KSZ8081RNB.

The KSZ8081 provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ8081 I/Os and the board. Micrel LinkMD® TDR-based cable diagnostics identify faulty copper cabling.

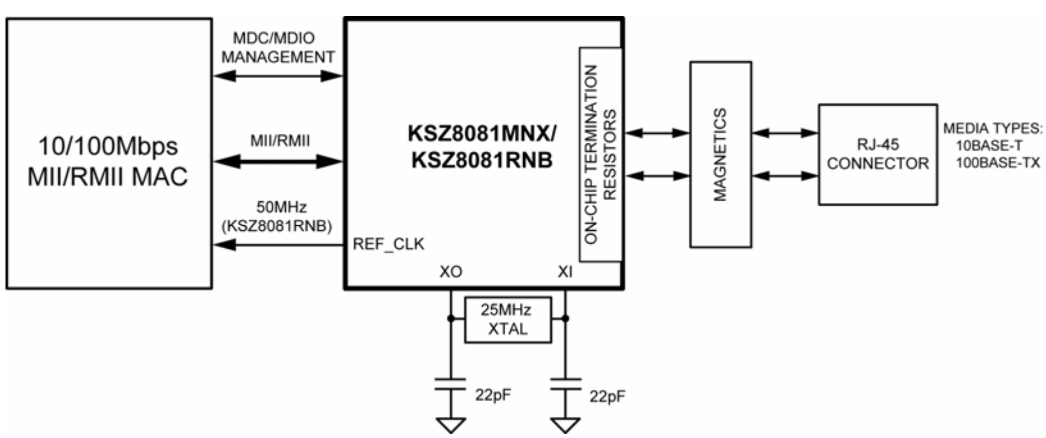
The KSZ8081MNX and KSZ8081RNB are available in 32-pin, lead-free QFN packages (see "Ordering Information").

Data sheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- Single-chip 10Base-T/100Base-TX IEEE 802.3 compliant Ethernet transceiver
- MII interface support (KSZ8081MNX)
- RMII v1.2 Interface support with a 50MHz reference clock output to MAC, and an option to input a 50MHz reference clock (KSZ8081RNB)
- Back-to-back mode support for a 100Mbps copper repeater
- MDC/MDIO management interface for PHY register configuration
- Programmable interrupt output
- LED outputs for link, activity, and speed status indication
- On-chip termination resistors for the differential pairs
- Baseline wander correction
- HP Auto MDI/MDI-X to reliably detect and correct straight-through and crossover cable connections with disable and enable option
- Auto-negotiation to automatically select the highest link-up speed (10/100Mbps) and duplex (half/full)
- Power-down and power-saving modes
- LinkMD TDR-based cable diagnostics to identify faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and the board

Functional Diagram



LinkMD is a registered trademark of Micrel, Inc.

Features (Continued)

- Loopback modes for diagnostics
- Single 3.3V power supply with VDD I/O options for 1.8V, 2.5V, or 3.3V
- Built-in 1.2V regulator for core
- Available in 32-pin (5mm x 5mm) QFN package

Applications

- Game console
- IP phone
- IP set-top box
- IP TV
- LOM
- Printer

Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Wire Bonding	Description
KSZ8081MNXCA	0°C to 70°C	32-Pin QFN	Pb-Free	Gold	MII, Commercial Temperature, Gold Wire Bonding
KSZ8081MNXCC(1)	0°C to 70°C	32-Pin QFN	Pb-Free	Copper	MII, Commercial Temperature, Copper Wire Bonding
KSZ8081MNXIA(1)	–40°C to 85°C	32-Pin QFN	Pb-Free	Gold	MII, Industrial Temperature, Gold Wire Bonding
KSZ8081MNXIC(1)	–40°C to 85°C	32-Pin QFN	Pb-Free	Copper	MII, Industrial Temperature, Copper Wire Bonding
KSZ8081RNBCA	0°C to 70°C	32-Pin QFN	Pb-Free	Gold	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Commercial Temperature, Gold Wire Bonding
KSZ8081RNBCC(1)	0°C to 70°C	32-Pin QFN	Pb-Free	Copper	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Commercial Temperature, Copper Wire Bonding
KSZ8081RNBIA(1)	–40°C to 85°C	32-Pin QFN	Pb-Free	Gold	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Industrial Temperature, Gold Wire Bonding
KSZ8081RNBIC(1)	–40°C to 85°C	32-Pin QFN	Pb-Free	Copper	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Industrial Temperature, Copper Wire Bonding
KSZ8081MNX-EVAL	0°C to 70°C	32-Pin QFN	Pb-Free		KSZ8081MNX Evaluation Board (Mounted with KSZ8081MNX device in commercial temperature)
KSZ8081RNB-EVAL	0°C to 70°C	32-Pin QFN	Pb-Free		KSZ8081RNB Evaluation Board (Mounted with KSZ8081RNB device in commercial temperature)

Note:

1. Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
1.0	11/05/12	Data sheet created

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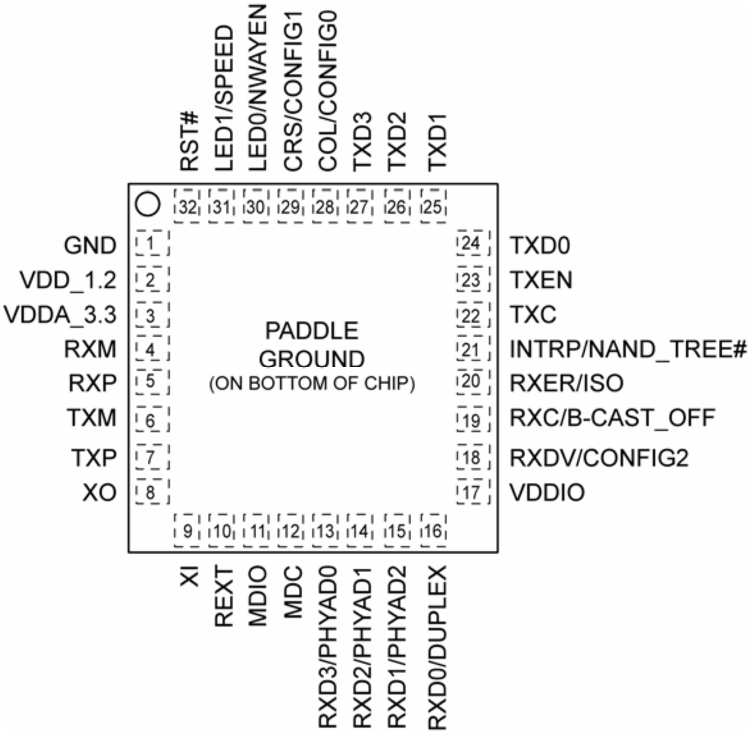
Pin Configuration– KSZ8081MNX



32-Pin (5mm x 5mm) QFN

Pin Description– KSZ8081MNX

Pin Number	Pin Name	Type[(1)]	Pin Function
1	GND	Gnd	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8081MNX) Decouple with 2.2µF and 0.1µF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RXM	I/O	Physical receive or transmit signal (– differential)
5	RXP	I/O	Physical receive or transmit signal (+ differential)
6	TXM	I/O	Physical transmit or receive signal (– differential)
7	TXP	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback for 25MHz crystal This pin is a no connect if an oscillator or external clock source is used.
9	XI	I	Crystal / Oscillator / External Clock input 25MHz ±50ppm
10	REXT	I	Set PHY transmit output current Connect a 6.49kΩ resistor to ground on this pin.
11	MDIO	Ipu/Opu	Management Interface (MII) Data I/O This pin has a weak pull-up, is open-drain, and requires an external 1.0kΩ pull-up resistor.
12	MDC	Ipu	Management Interface (MII) Clock input This clock pin is synchronous to the MDIO data pin.
13	RXD3/ PHYAD0	Ipu/O	MII mode: MII Receive Data Output[3][(2)] Config mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See the "Strapping Options" section for details.
14	RXD2/ PHYAD1	Ipd/O	MII mode: MII Receive Data Output[2][(2)] Config mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See the "Strapping Options" section for details.
15	RXD1/ PHYAD2	Ipd/O	MII mode: MII Receive Data Output[1][(2)] Config mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See the "Strapping Options" section for details.
16	RXD0/ DUPLEX	Ipu/O	MII mode: MII Receive Data Output[0][(2)] Config mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See the "Strapping Options" section for details.
17	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DD}
18	RXDV/ CONFIG2	Ipd/O	MII mode: MII Receive Data Valid output Config mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See the "Strapping Options" section for details.
19	RXC/ B-CAST_OFF	Ipd/O	MII mode: MII Receive Clock output Config mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See the "Strapping Options" section for details.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>20</td><td>RXER/
ISO</td><td>Ipd/O</td><td>MII mode: MII Receive Error output
Config mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset.
See the “Strapping Options” section for details.</td></tr>
<tr><td>21</td><td>INTRP/
NAND_Tree#</td><td>Ipu/Opu</td><td>Interrupt output: Programmable interrupt output
This pin has a weak pull-up, is open-drain, and requires an external 1.0kΩ pull-up resistor.
Config mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.
See the “Strapping Options” section for details</td></tr>
<tr><td>22</td><td>TXC</td><td>I/O</td><td>MII mode: MII Transmit Clock output
MII back-to-back mode: MII Transmit Clock input</td></tr>
<tr><td>23</td><td>TXEN</td><td>I</td><td>MII mode: MII Transmit Enable input</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>MII mode: MII Transmit Data Input[0][3]</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>MII mode: MII Transmit Data Input[1][3]</td></tr>
<tr><td>26</td><td>TXD2</td><td>I</td><td>MII mode: MII Transmit Data Input[2][3]</td></tr>
<tr><td>27</td><td>TXD3</td><td>I</td><td>MII Mode: MII Transmit Data Input[3][3]</td></tr>
<tr><td>28</td><td>COL/
CONFIG0</td><td>Ipd/O</td><td>MII mode: MII Collision Detect output
Config mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset.
See the “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>CRS/
CONFIG1</td><td>Ipd/O</td><td>MII mode: MII Carrier Sense output
Config mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset.
See the “Strapping Options” section for details.</td></tr>
<tr><td>30</td><td>LED0/
NWAYEN</td><td>Ipu/O</td><td>LED output: Programmable LED0 output
Config mode: Latched as auto-negotiation enable (register 0h, bit [12]) at the de-assertion of reset.
See the “Strapping Options” section for details.
The LED0 pin is programmable using register 1Fh bits [5:4], and is defined as follows.
<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
</table>
LED mode = [10], [11] Reserved</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>31</td><td>LED1/
SPEED</td><td>Ipu/O</td><td>LED output: Programmable LED1 output
Config mode: Latched as Speed (register 0h, bit [13]) at the de-assertion of reset.
See the “Strapping Options” section for details.
The LED1 pin is programmable using register 1Fh bits [5:4], and is defined as follows.

LED mode = [00]
<table><tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>10Base-T</td><td>High</td><td>OFF</td></tr><tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr></table>
LED mode = [01]
<table><tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No activity</td><td>High</td><td>OFF</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
LED mode = [10], [11] Reserved</td></tr>
<tr><td>32</td><td>RST#</td><td>Ipu</td><td>Chip reset (active low)</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>Gnd</td><td>Ground</td></tr>
</table>

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up (see “Electrical Characteristics” for value).
   Ipu/O = Input with internal pull-up (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see “Electrical Characteristics” for value) and output with internal pull-up (see “Electrical Characteristics” for value).
2. MII RX Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC. RXD[3:0] is invalid data from the PHY when RXDV is de-asserted.
3. MII TX Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] presents valid data from the MAC. TXD[3:0] has no effect on the PHY when TXEN is de-asserted.

Strapping Options – KSZ8081MNX

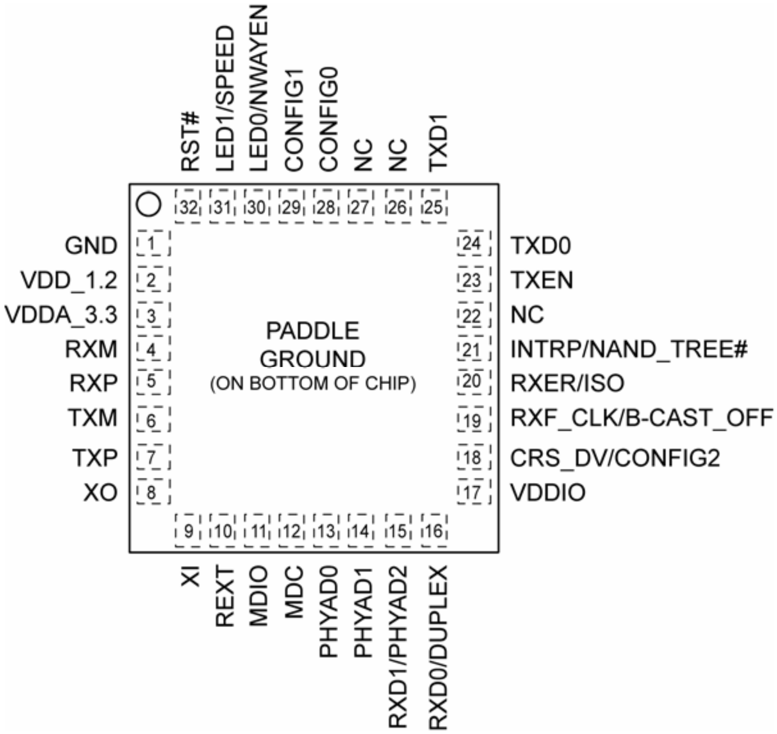
<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>15
14
13</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>PHYAD[2:0] is latched at de-assertion of reset and is configurable to any value from 0 to 7 with PHY Address 1 as the default value.
PHY Address 0 is assigned by default as the broadcast PHY address, but it can be assigned as a unique PHY address after pulling the B-CAST_OFF strapping pin high or writing a ‘1’ to register 16h, bit [9].
PHY Address bits [4:3] are set to 00 by default.</td></tr>
<tr><td>18
29
28</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>110</td><td>MII back-to-back</td></tr><tr><td>001 – 101, 111</td><td>Reserved – not used</td></tr></table></td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>Isolate mode
Pull-up = Enable
Pull-down (default) = Disable
At the de-assertion of reset, this pin value is latched into register 0h, bit [10].</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>Speed mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
At the de-assertion of reset, this pin value is latched into register 0h, bit [13] as the speed select, and also is latched into register 4h (auto-negotiation advertisement) as the speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>Duplex mode
Pull-up (default) = Half-duplex
Pull-down = Full-duplex
At the de-assertion of reset, this pin value is latched into register 0h, bit [8].</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway auto-negotiation enable
Pull-up (default) = Enable auto-negotiation
Pull-down = Disable auto-negotiation
At the de-assertion of reset, this pin value is latched into register 0h, bit [12].</td></tr>
<tr><td>19</td><td>B-CAST_OFF</td><td>Ipd/O</td><td>Broadcast off – for PHY Address 0
Pull-up = PHY Address 0 is set as an unique PHY address
Pull-down (default) = PHY Address 0 is set as a broadcast PHY address
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
<tr><td>21</td><td>NAND_Tree#</td><td>Ipu/Opu</td><td>NAND tree mode
Pull-up (default) = Disable
Pull-down = Enable
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see “Electrical Characteristics” for value) and output with internal pull-up (see “Electrical Characteristics” for value).

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to unintended high/low states. In this case, external pull-ups (4.7kΩ) or pull-downs (1.0kΩ) should be added on these PHY strap-in pins to ensure that the intended values are strapped-in correctly.

Pin Configuration – KSZ8081RNB



32-Pin (5mm x 5mm) QFN

Pin Description– KSZ8081RNB

Pin Number	Pin Name	Type(1)	Pin Function
1	GND	Gnd	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8081RNB) Decouple with 2.2µF and 0.1µF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RXM	I/O	Physical receive or transmit signal (– differential)
5	RXP	I/O	Physical receive or transmit signal (+ differential)
6	TXM	I/O	Physical transmit or receive signal (– differential)
7	TXP	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback for 25MHz crystal This pin is a no connect if an oscillator or external clock source is used.
9	XI	I	25MHz Mode: 25MHz ±50ppm Crystal / Oscillator / External Clock Input 50MHz Mode: 50MHz ±50ppm Oscillator / External Clock Input
10	REXT	I	Set PHY transmit output current Connect a 6.49kΩ resistor to ground on this pin.
11	MDIO	Ipu/Opu	Management Interface (MII) Data I/O This pin has a weak pull-up, is open-drain, and requires an external 1.0kΩ pull-up resistor.
12	MDC	Ipu	Management Interface (MII) Clock input This clock pin is synchronous to the MDIO data pin.
13	PHYAD0	Ipu/O	The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See the "Strapping Options" section for details.
14	PHYAD1	Ipd/O	The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See the "Strapping Options" section for details.
15	RXD1/ PHYAD2	Ipd/O	RMII mode: RMII Receive Data Output[1](2) Config mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See the "Strapping Options" section for details.
16	RXD0/ DUPLEX	Ipu/O	RMII mode: RMII Receive Data Output[0](2) Config mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See the "Strapping Options" section for details.
17	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DD}
18	CRS_DV/ CONFIG2	Ipd/O	RMII mode: RMII Carrier Sense/Receive Data Valid output / Config mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See the "Strapping Options" section for details.
19	REF_CLK/ B-CAST_OFF	Ipd/O	RMII mode: 25MHz mode: This pin provides the 50MHz RMII reference clock output to the MAC. See also XI (pin 9). 50MHz mode: This pin is a no connect. See also XI (pin 9). Config mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See the "Strapping Options" section for details.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>20</td><td>RXER/
ISO</td><td>Ipd/O</td><td>RMII mode: RMII Receive Error output
Config mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset.
See the “Strapping Options” section for details.</td></tr>
<tr><td>21</td><td>INTRP/
NAND_Tree#</td><td>Ipu/Opu</td><td>Interrupt output: Programmable interrupt output
This pin has a weak pull-up, is open-drain, and requires an external 1.0kΩ pull-up resistor.
Config mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.
See the “Strapping Options” section for details.</td></tr>
<tr><td>22</td><td>NC</td><td>-</td><td>No connect – This pin is not bonded and can be left floating.</td></tr>
<tr><td>23</td><td>TXEN</td><td>I</td><td>RMII Transmit Enable input</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>RMII Transmit Data Input[0][3]</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>RMII Transmit Data Input[1][3]</td></tr>
<tr><td>26</td><td>NC</td><td>-</td><td>No connect – This pin is not bonded and can be left floating.</td></tr>
<tr><td>27</td><td>NC</td><td>-</td><td>No connect – This pin is not bonded and can be left floating.</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See the “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See the “Strapping Options” section for details.</td></tr>
<tr><td>30</td><td>LED0/
NWAYEN</td><td>Ipu/O</td><td>LED output: Programmable LED0 output
Config mode: Latched as auto-negotiation enable (register 0h, bit [12]) at the de-assertion of reset.
See the “Strapping Options” section for details.
The LED0 pin is programmable using register 1Fh bits [5:4], and is defined as follows.
<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
</table>
LED mode = [10], [11] Reserved</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[(1)]</th><th>Pin Function</th></tr>
<tr><td>31</td><td>LED1/
SPEED</td><td>Ipu/O</td><td>LED output: Programmable LED1 output
Config mode: Latched as Speed (register 0h, bit [13]) at the de-assertion of reset.
See the “Strapping Options” section for details.
The LED1 pin is programmable using register 1Fh bits [5:4], and is defined as follows.

LED mode = [00]
<table><tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>10Base-T</td><td>High</td><td>OFF</td></tr><tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr></table>
LED mode = [01]
<table><tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No activity</td><td>High</td><td>OFF</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
LED mode = [10], [11] Reserved</td></tr>
<tr><td>32</td><td>RST#</td><td>Ipu</td><td>Chip reset (active low)</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>Gnd</td><td>Ground</td></tr>
</table>

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up (see “Electrical Characteristics” for value).
   Ipu/O = Input with internal pull-up (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see “Electrical Characteristics” for value) and output with internal pull-up (see “Electrical Characteristics” for value).
   NC = Pin is not bonded to the die.
2. RMII RX Mode: The RXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.
3. RMII TX Mode: The TXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock. For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

Strapping Options – KSZ8081RNB

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>15
14
13</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>PHYAD[2:0] is latched at de-assertion of reset and is configurable to any value from 0 to 7 with PHY Address 1 as the default value.
PHY Address 0 is assigned by default as the broadcast PHY address, but it can be assigned as a unique PHY address after pulling the B-CAST_OFF strapping pin high or writing a ‘1’ to register 16h, bit [9].
PHY Address bits [4:3] are set to 00 by default.</td></tr>
<tr><td>18
29
28</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>001</td><td>RMII</td></tr><tr><td>101</td><td>RMII back-to-back</td></tr><tr><td>000, 010 – 100, 110, 111</td><td>Reserved – not used</td></tr></table></td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>Isolate mode
Pull-up = Enable
Pull-down (default) = Disable
At the de-assertion of reset, this pin value is latched into register 0h, bit [10].</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>Speed mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
At the de-assertion of reset, this pin value is latched into register 0h, bit [13] as the speed select, and also is latched into register 4h (auto-negotiation advertisement) as the speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>Duplex mode
Pull-up (default) = Half-duplex
Pull-down = Full-duplex
At the de-assertion of reset, this pin value is latched into register 0h, bit [8].</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway auto-negotiation enable
Pull-up (default) = Enable auto-negotiation
Pull-down = Disable auto-negotiation
At the de-assertion of reset, this pin value is latched into register 0h, bit [12].</td></tr>
<tr><td>19</td><td>B-CAST_OFF</td><td>Ipd/O</td><td>Broadcast off – for PHY Address 0
Pull-up = PHY Address 0 is set as an unique PHY address
Pull-down (default) = PHY Address 0 is set as a broadcast PHY address
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
<tr><td>21</td><td>NAND_Tree#</td><td>Ipu/Opu</td><td>NAND tree mode
Pull-up (default) = Disable
Pull-down = Enable
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see “Electrical Characteristics” for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see “Electrical Characteristics” for value) and output with internal pull-up (see “Electrical Characteristics” for value).

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched to unintended high/low states. In this case, external pull-ups (4.7kΩ) or pull-downs (1.0kΩ) should be added on these PHY strap-in pins to ensure that the intended values are strapped-in correctly.

Functional Description: 10Base-T/100Base-TX Transceiver

The KSZ8081 is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8081 supports 10Base-T and 100Base-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8081MNX offers the Media Independent Interface (MII) and the KSZ8081RNB offers the Reduced Media Independent Interface (RMII) for direct connection with MII and RMII compliant Ethernet MAC processors and switches, respectively.

The MII management bus option gives the MAC processor complete access to the KSZ8081 control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

The KSZ8081MNX/RNB is used to refer to both KSZ8081MNX and KSZ8081RNB versions in this data sheet.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal to NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII format and provided as the input data to the MAC.

Scrambler/De-Scrambler (100Base-TX Only)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV, or with short pulse widths, to prevent noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8081MNX/RNB decodes a data frame. The receive clock is kept active during idle periods between data receptions.

SQE and Jabber Function (10Base-T Only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE test is needed to test the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

PLL Clock Synthesizer

The KSZ8081MNX/RNB generates all internal clocks and all external clocks for system timing from an external 25MHz crystal, oscillator, or reference clock. For the KSZ8081RNB in RMII 50MHz clock mode, these clocks are generated from an external 50MHz oscillator or system clock.

Auto-Negotiation

The KSZ8081MNX/RNB conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8081MNX/RNB link partner is forced to bypass auto-negotiation, then the KSZ8081MNX/RNB sets its operating mode by observing the signal at its receiver. This is known as parallel detection, which allows the KSZ8081MNX/RNB to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (NWAYEN, pin 42) or software (register 0h, bit [12]).

By default, auto-negotiation is enabled after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled by register 0h, bit [12]. If auto-negotiation is disabled, the speed is set by register 0h, bit [13], and the duplex is set by register 0h, bit [8].

The auto-negotiation link-up process is shown in Figure 1.

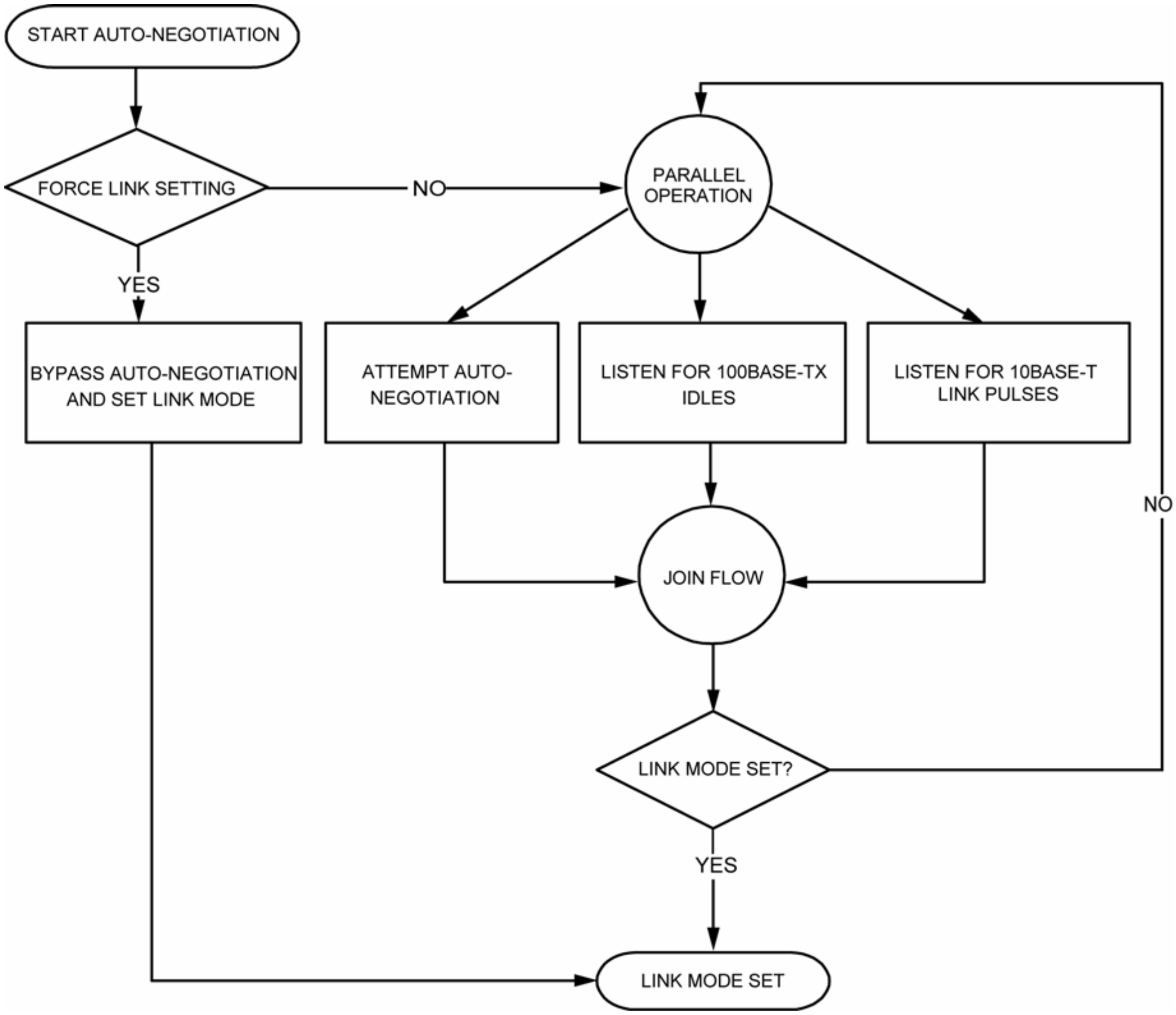


Figure 1. Auto-Negotiation Flow Chart

MII Interface (KSZ8081MNX only)

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 15 pins (6 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10Mbps and 100Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4 bits wide, a nibble.

By default, the KSZ8081MNX is configured to MII mode after it is powered up or hardware reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to 000 (default setting).

MII Signal Definition

Table 1 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

MII Signal Name	Direction (with respect to PHY, KSZ8081MNX signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data[3:0]
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data[3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

Table 1. MII Signal Definition

Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII. It is negated before the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

Transmit Data[3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted by the PHY for transmission. TXD[3:0] is 00 to indicate idle when TXEN is de-asserted. Values other than 00 on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while the carrier is active. RXC is derived from the PHY's reference clock when the line is idle or the link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If the link is down, RXC is derived from the PHY's reference clock.

RXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the start-of-frame delimiter (SFD), 5D, and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

Receive Data[3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This informs the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

MII Signal Diagram

The KSZ8081MNX MII pin connections to the MAC are shown in Figure 2.

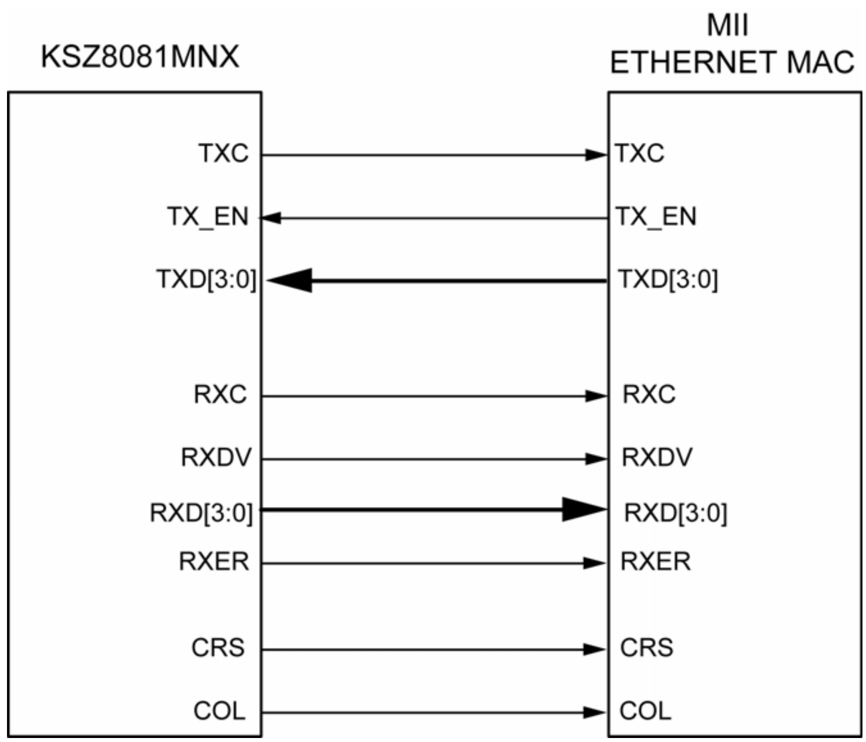


Figure 2. KSZ8081MNX MII Interface

RMII Data Interface (KSZ8081RNB only)

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, and 1 pin for the 50MHz reference clock).
- 10Mbps and 100Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2 bits wide, a dibit.

RMII – 25MHz Clock Mode

The KSZ8081RNB is configured to RMII – 25MHz clock mode after it is powered up or hardware reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to 001.
- Register 1Fh, bit [7] is set to 0 (default value) to select 25MHz clock mode.

RMII – 50MHz Clock Mode

The KSZ8081RNB is configured to RMII – 50MHz clock mode after it is powered up or hardware reset with the following:

- An external 50MHz clock source (oscillator) connected to XI (pin 9).
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to 001.
- Register 1Fh, bit [7] is set to 1 to select 50MHz clock mode.

RMII Signal Definition

Table 2 describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.

RMII Signal Name	Direction (with respect to PHY, KSZ8081RNB signal)	Direction (with respect to MAC)	Description
REF_CLK	Output (25MHz clock mode) / <no connect> (50MHz clock mode)	Input/ Input or <no connect>	Synchronous 50MHz reference clock for receive, transmit, and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data[1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data[1:0]
RXER	Output	Input, or (not required)	Receive Error

Table 2. RMII Signal Definition

Reference Clock (REF_CLK)

REF_CLK is a continuous 50MHz clock that provides the timing reference for TXEN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For 25MHz clock mode, the KSZ8081RNB generates and outputs the 50MHz RMII REF_CLK to the MAC at REF_CLK (pin 19).

For 50MHz clock mode, the KSZ8081RNB takes in the 50MHz RMII REF_CLK from the MAC or system board at XI (pin 9) and leaves the REF_CLK (pin 19) as a no connect.

Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII. It is negated before the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

Transmit Data[1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TXEN is asserted, the PHY accepts TXD[1:0] for transmission.

TXD[1:0] is 00 to indicate idle when TXEN is de-asserted. The PHY ignores values other than 00 on TXD[1:0] while TXEN is de-asserted.

Carrier Sense / Receive Data Valid (CRS_DV)

The PHY asserts CRS_DV when the receive medium is non-idle. It is asserted asynchronously when a carrier is detected. This happens when squelch is passed in 10Mbps mode, and when two non-contiguous 0s in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

While carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit. It is negated before the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid after CRS_DV is asserted. However, because the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is 00 until receive signals are properly decoded.

Receive Data[1:0] (RXD[1:0])

RXD[1:0] transitions synchronously with respect to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] is 00 to indicate idle when CRS_DV is de-asserted. The MAC ignores values other than 00 on RXD[1:0] while CRS_DV is de-asserted.

Receive Error (RXER)

RXER is asserted for one or more REF_CLK periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to REF_CLK. . While CRS_DV is de-asserted, RXER has no effect on the MAC.

Collision Detection (COL)

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

RMII Signal Diagram

The KSZ8081RNB RMII pin connections to the MAC for 25MHz clock mode are shown in Figure 3. The connections for 50MHz clock mode are shown in Figure 4 .

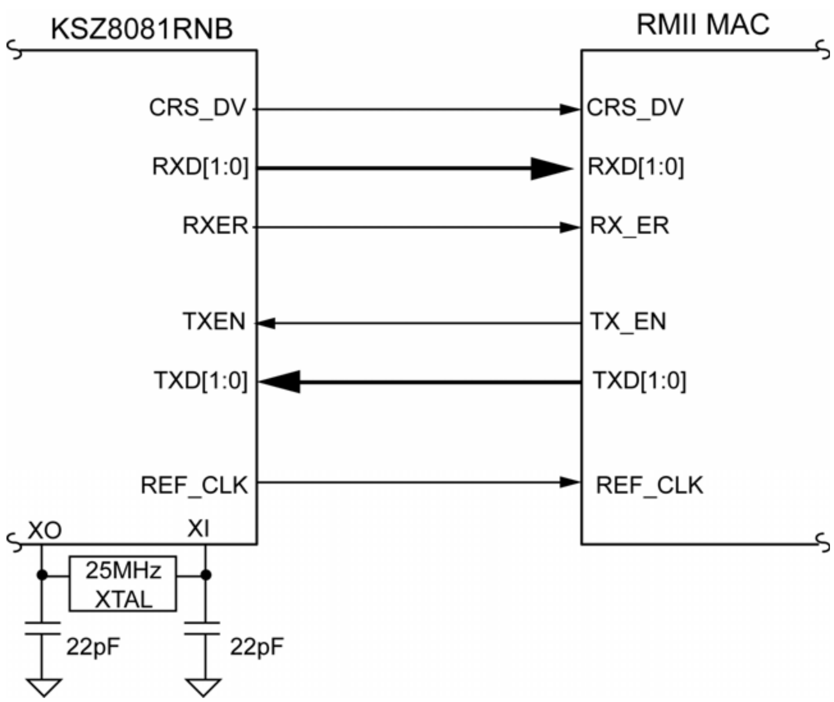


Figure 3. KSZ8081RNB RMII Interface (25MHz Clock Mode)

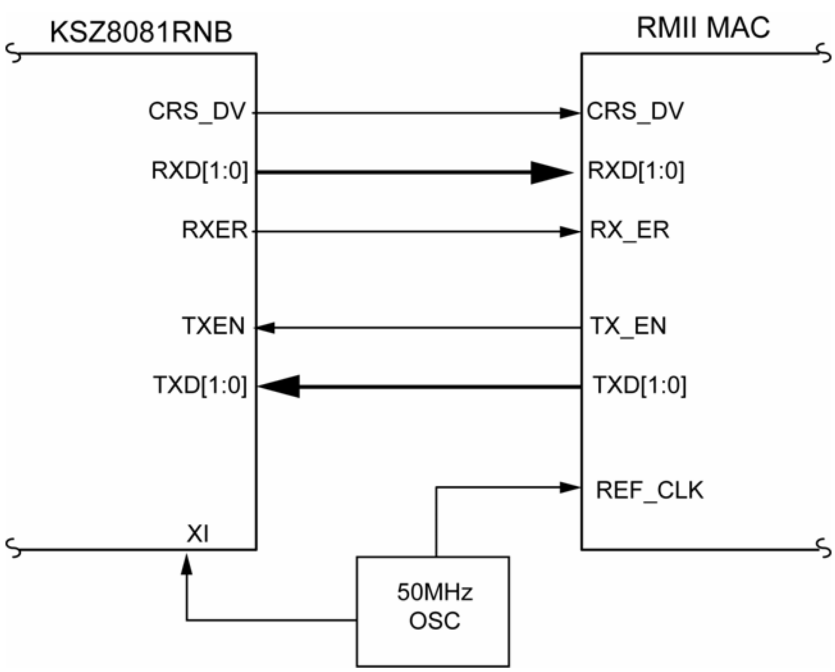


Figure 4. KSZ8081RNB RMII Interface (50MHz Clock Mode)

Back-to-Back Mode – 100Mbps Copper Repeater

Two KSZ8081MNX/RNB devices can be connected back-to-back to form a 100Base-TX copper repeater.

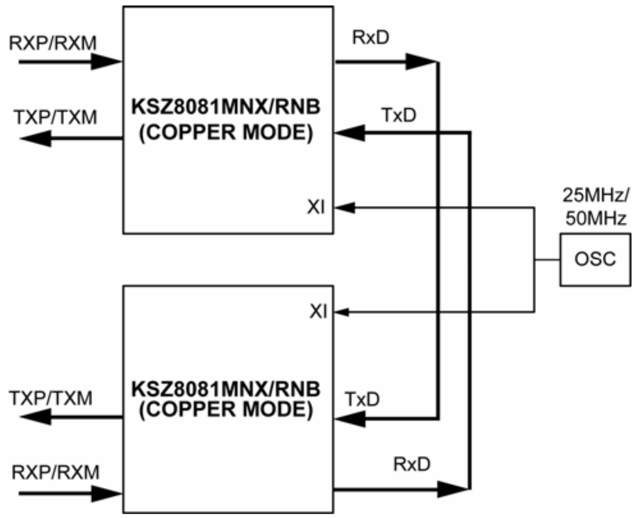


Figure 5. KSZ8081MNX/RNB to KSZ8081MNX/RNB Back-to-Back Copper Repeater

MII Back-to-Back Mode (KSZ8081MNX only)

In MII back-to-back mode, a KSZ8081MNX interfaces with another KSZ8081MNX to provide a complete 100Mbps copper repeater solution.

The KSZ8081MNX devices are configured to MII back-to-back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] (pins 18, 29, 28) set to 110
- A common 25MHz reference clock connected to XI (pin 9) of both KSZ8081MNX devices
- MII signals connected as shown in Table 3

KSZ8081MNX (100Base-TX copper) [Device 1]			KSZ8081MNX (100Base-TX copper) [Device 2]		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
RXC	19	Output	TXC	22	Input
RXDV	18	Output	TXEN	23	Input
RXD3	13	Output	TXD3	27	Input
RXD2	14	Output	TXD2	26	Input
RXD1	15	Output	TXD1	25	Input
RXD0	16	Output	TXD0	24	Input
TXC	22	Input	RXC	19	Output
TXEN	23	Input	RXDV	18	Output
TXD3	27	Input	RXD3	13	Output
TXD2	26	Input	RXD2	14	Output
TXD1	25	Input	RXD1	15	Output
TXD0	24	Input	RXD0	16	Output

Table 3. MII Signal Connection for MII Back-to-Back Mode (100Base-TX Copper Repeater)

RMII Back-to-Back Mode (KSZ8081RNB only)

In RMII back-to-back mode, a KSZ8081RNB interfaces with another KSZ8081RNB to provide a complete 100Mbps copper repeater solution.

The KSZ8081RNB devices are configured to RMII back-to-back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] (pins 18, 29, 28) set to 101
- A common 50MHz reference clock connected to XI (pin 9) of both KSZ8081RNB devices
- RMII signals connected as shown in Table 4

KSZ8081RNB (100Base-TX copper) [Device 1]			KSZ8081RNB (100Base-TX copper) [Device 2]		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
CRSDV	18	Output	TXEN	23	Input
RXD1	15	Output	TXD1	25	Input
RXD0	16	Output	TXD0	24	Input
TXEN	23	Input	CRSDV	18	Output
TXD1	25	Input	RXD1	15	Output
TXD0	24	Input	RXD0	16	Output

Table 4. RMII Signal Connection for RMII Back-to-Back Mode (100Base-TX Copper Repeater)

MII Management (MIIM) Interface

The KSZ8081MNX/RNB supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8081MNX/RNB. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Registers [0:8] are standard registers, and their functions are defined in the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See the "Register Map" section for details.

As the default, the KSZ8081MNX/RNB supports unique PHY addresses 1 to 7, and broadcast PHY address 0. The latter is defined in the IEEE 802.3 Specification, and can be used to read/write to a single KSZ8081MNX/RNB device, or write to multiple KSZ8081MNX/RNB devices simultaneously.

PHY address 0 can optionally be disabled as the broadcast address by either hardware pin strapping (B-CAST_OFF, pin 19) or software (register 16h, bit [9]), and assigned as a unique PHY address.

The PHYAD[2:0] strapping pins are used to assign a unique PHY address between 0 and 7 to each KSZ8081MNX/RNB device.

Table 5 shows the MII management frame format for the KSZ8081MNX/RNB.

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 5. MII Management Frame Format for the KSZ8081MNX/RNB

Interrupt (INTRP)

INTRP (pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8081MNX/RNB PHY register. Bits [15:8] of register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit [9] of register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8081MNX/RNB control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8081MNX/RNB and its link partner. This feature allows the KSZ8081MNX/RNB to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs to the KSZ8081MNX/RNB accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a ‘1’ to register 1Fh, bit [13]. MDI and MDI-X mode is selected by register 1Fh, bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 6 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TX+	1	RX+
2	TX–	2	RX–
3	RX+	3	TX+
6	RX–	6	TX–

Table 6. MDI/MDI-X Pin Definition

Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 6 shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).

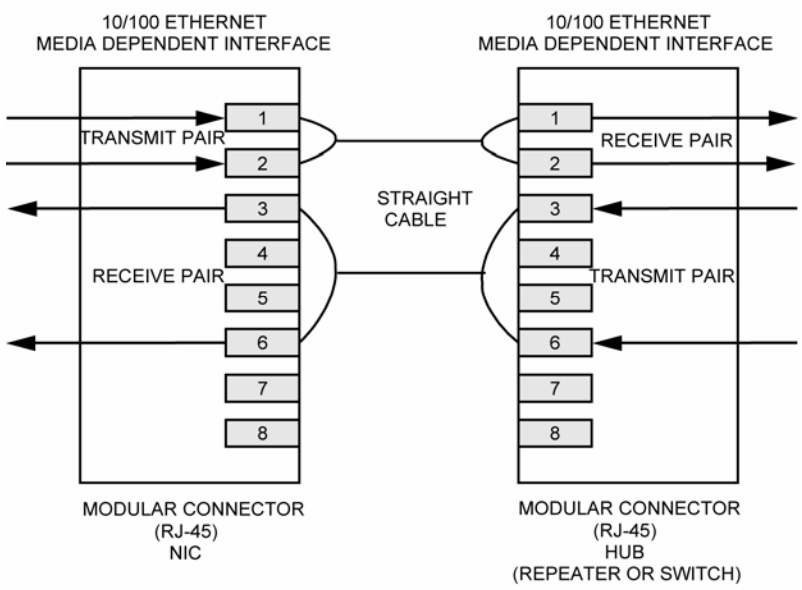


Figure 6. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 7 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

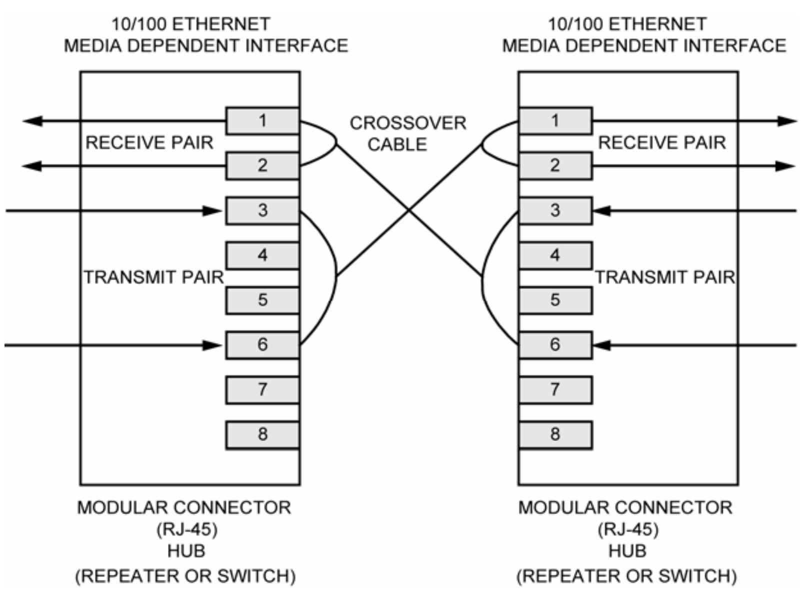


Figure 7. Typical Crossover Cable Connection

Loopback Mode

The KSZ8081MNX/RNB supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

Local (Digital) Loopback

This loopback mode checks the MII/RMII transmit and receive data paths between the KSZ8081MNX/RNB and the external MAC, and is supported for both speeds (10/100Mbps) at full-duplex.

The loopback data path is shown in Figure 8.

1. The MII/RMII MAC transmits frames to the KSZ8081MNX/RNB.
2. Frames are wrapped around inside the KSZ8081MNX/RNB.
3. The KSZ8081MNX/RNB transmits frames back to the MII/RMII MAC.

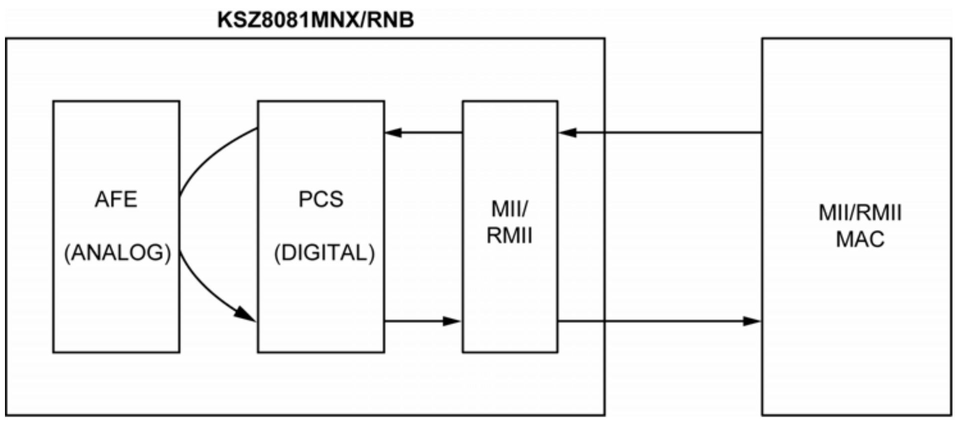


Figure 8. Local (Digital) Loopback

The following programming action and register settings are used for local loopback mode.

For 10/100Mbps loopback,

Set register 0h,

- Bit [14] = 1 // Enable local loopback mode
- Bit [13] = 0/1 // Select 10Mbps/100Mbps speed
- Bit [12] = 0 // Disable auto-negotiation
- Bit [8] = 1 // Select full-duplex mode

Remote (Analog) Loopback

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8081MNX/RNB and its link partner, and is supported for 100Base-TX full-duplex mode only.

The loopback data path is shown in Figure 9.

1. The Fast Ethernet (100Base-TX) PHY link partner transmits frames to the KSZ8081MNX/RNB.
2. Frames are wrapped around inside the KSZ8081MNX/RNB.
3. The KSZ8081MNX/RNB transmits frames back to the Fast Ethernet (100Base-TX) PHY link partner.

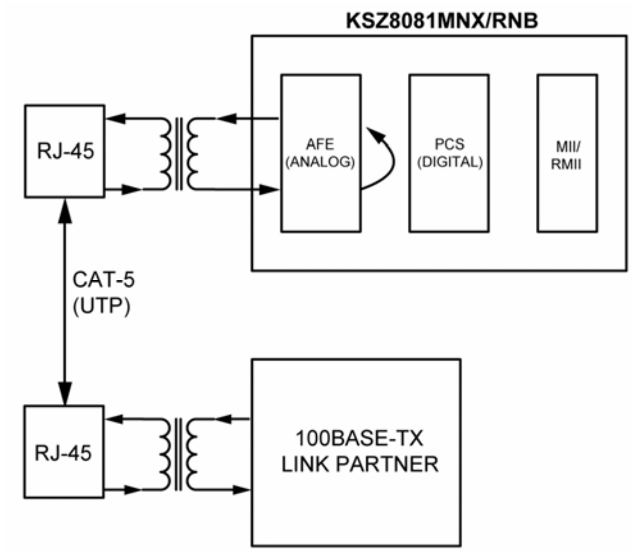


Figure 9. Remote (Analog) Loopback

The following programming steps and register settings are used for remote loopback mode.

1. Set Register 0h,
   - Bits [13] = 1 // Select 100Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

   Or just auto-negotiate and link up at 100Base-TX full-duplex mode with the link partner.

2. Set Register 1Fh,
   - Bit [2] = 1 // Enable remote loopback mode

LinkMD® Cable Diagnostic

The LinkMD function uses time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems. These include open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing register 1Dh, the LinkMD Control/Status register, in conjunction with register 1Fh, the PHY Control 2 register. The latter register is used to disable Auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

NAND Tree Support

The KSZ8081MNX/RNB provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8081MNX/RNB digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the CRS/CONFIG1 pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high

- Driving each NAND tree input pin low, sequentially, according to the NAND tree pin order
- Checking the NAND tree output to make sure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 7 and Table 8 list the NAND tree pin orders for KSZ8081MNX and KSZ8081RNB, respectively.

Pin Number	Pin Name	NAND Tree Description
11	MDIO	Input
12	MDC	Input
13	RXD3	Input
14	RXD2	Input
15	RXD1	Input
16	RXD0	Input
18	RXDV	Input
19	RXC	Input
20	RXER	Input
21	INTRP	Input
22	TXC	Input
23	TXEN	Input
24	TXD0	Input
25	TXD1	Input
26	TXD2	Input
27	TXD3	Input
30	LED0	Input
31	LED1	Input
28	COL	Input
29	CRS	Output

Table 7. NAND Tree Test Pin Order for KSZ8081MNX

Pin Number	Pin Name	NAND Tree Description
11	MDIO	Input
12	MDC	Input
13	PHYAD0	Input
14	PHYAD1	Input
15	RXD1	Input
16	RXD0	Input
18	CRS_DV	Input
19	REF_CLK	Input
20	RXER	Input
21	INTRP	Input
23	TXEN	Input
24	TXD0	Input
25	TXD1	Input
30	LED0	Input
31	LED1	Input
28	CONFIG0	Input
29	CONFIG1	Output

Table 8. NAND Tree Test Pin Order for KSZ8081RNB

NAND Tree I/O Testing

Use the following procedure to check for faults on the KSZ8081MNX/RNB digital I/O pin connections to the board:

1. Enable NAND tree mode using either hardware (NAND_Tree#, pin 21) or software (register 16h, bit [5]).
2. Use board logic to drive all KSZ8081MNX/RNB NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, in KSZ8081MNX/RNB NAND tree pin order, as follows:
    a. Toggle the first pin (MDIO) from high to low, and verify that the CRS/CONFIG1 pin switches from high to low to indicate that the first pin is connected properly.
    b. Leave the first pin (MDIO) low.
    c. Toggle the second pin (MDC) from high to low, and verify that the CRS/CONFIG1 pin switches from low to high to indicate that the second pin is connected properly.
    d. Leave the first pin (MDIO) and the second pin (MDC) low.
    e. Toggle the third pin (RXD3/PHYAD0)) from high to low, and verify that the CRS/CONFIG1 pin switches from high to low to indicate that the third pin is connected properly.
    f. Continue with this sequence until all KSZ8081MNX/RNB NAND tree input pins have been toggled.

Each KSZ8081MNX/RNB NAND tree input pin must cause the CRS/CONFIG1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the CRS pin fails to toggle when the KSZ8081MNX/RNB input pin toggles from high to low, the input pin has a fault.

Power Management

The KSZ8081MNX/RNB incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

Power-Saving Mode

Power-saving mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a ‘1’ to register 1Fh, bit [10], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ8081MNX/RNB shuts down all transceiver blocks, except for the transmitter, energy detect, and PLL circuits.

By default, power-saving mode is disabled after power-up.

Energy-Detect Power-Down Mode

Energy-detect power-down (EDPD) mode is used to further reduce transceiver power consumption when the cable is unplugged. It is enabled by writing a ‘0’ to register 18h, bit [11], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

EDPD mode works with the PLL off (set by writing a ‘1’ to register 10h, bit [4] to automatically turn the PLL off in EDPD mode) to turn off all KSZ8081MNX/RNB transceiver blocks except the transmitter and energy-detect circuits.

Power can be reduced further by extending the time interval between transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the KSZ8081MNX/RNB and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them.

By default, energy-detect power-down mode is disabled after power-up.

Power-Down Mode

Power-down mode is used to power down the KSZ8081MNX/RNB device when it is not in use after power-up. It is enabled by writing a ‘1’ to register 0h, bit [11].

In this mode, the KSZ8081MNX/RNB disables all internal functions except the MII management interface. The KSZ8081MNX/RNB exits (disables) power-down mode after register 0h, bit [11] is set back to ‘0’.

Slow-Oscillator Mode

Slow-oscillator mode is used to disconnect the input reference crystal/clock on XI (pin 8) and select the on-chip slow oscillator when the KSZ8081MNX/RNB device is not in use after power-up. It is enabled by writing a ‘1’ to register 11h, bit [5].

Slow-oscillator mode works in conjunction with power-down mode to put the KSZ8081MNX/RNB device in the lowest power state, with all internal functions disabled except the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable slow-oscillator mode by writing a ‘0’ to register 11h, bit [5].
2. Disable power-down mode by writing a ‘0’ to register 0h, bit [11].
3. Initiate software reset by writing a ‘1’ to register 0h, bit [15].

Reference Circuit for Power and Ground Connections

The KSZ8081MNX/RNB is a single 3.3V supply device with a built-in regulator to supply the 1.2V core. The power and ground connections are shown in Figure 10 and Table 9 for 3.3V VDDIO.

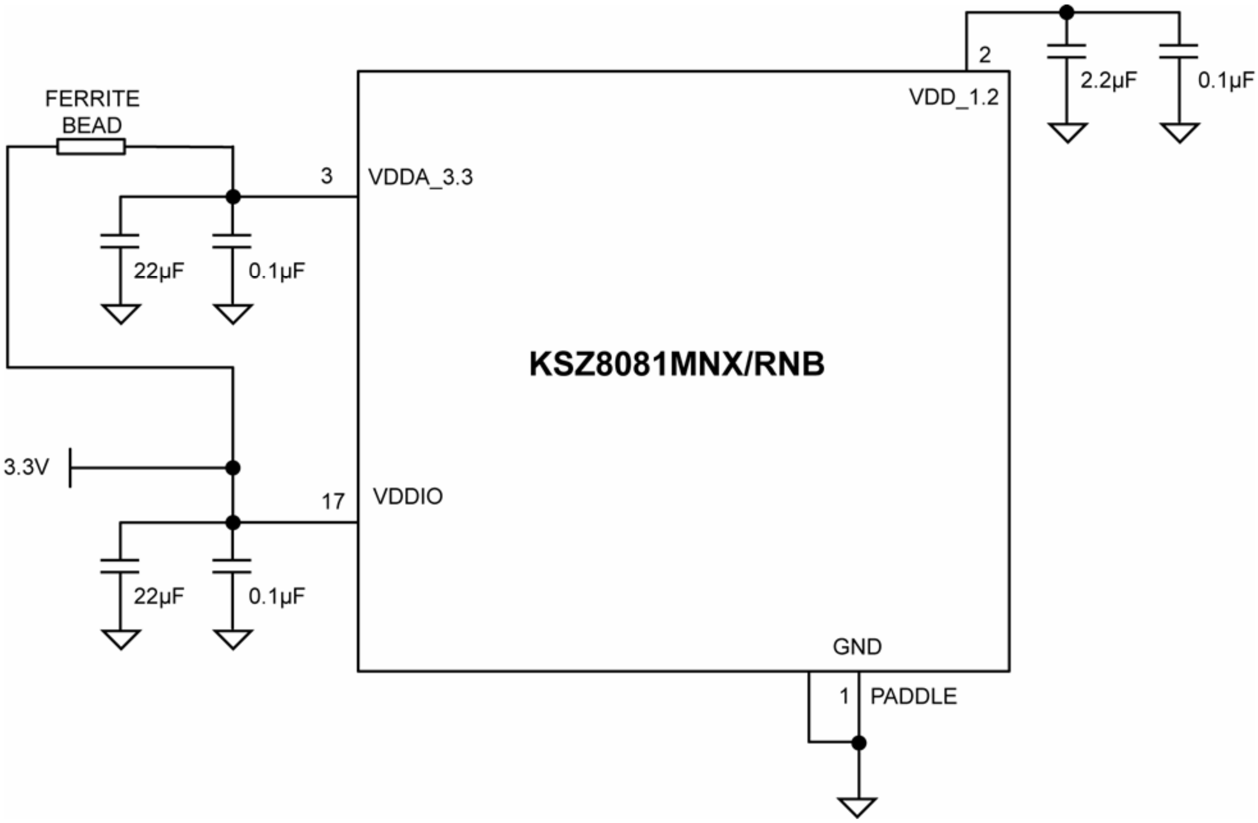


Figure 10. KSZ8081MNX/RNB Power and Ground Connections

Power Pin	Pin Number	Description
VDD_1.2	2	Decouple with 2.2µF and 0.1µF capacitors to ground.
VDDA_3.3	3	Connect to board's 3.3V supply through a ferrite bead. Decouple with 22µF and 0.1µF capacitors to ground.
VDDIO	17	Connect to board's 3.3V supply for 3.3V VDDIO. Decouple with 22µF and 0.1µF capacitors to ground.

Table 9. KSZ8081MNX/RNB Power Pin Description

Typical Current/Power Consumption

Table 10 through Table 12 show typical values for current consumption by the transceiver (VDDA_3.3) and digital I/O (VDDIO) power pins and typical values for power consumption by the KSZ8081MNX/RNB device for the indicated nominal operating voltages. These current and power consumption values include the transmit driver current and on-chip regulator current for the 1.2V core.

Transceiver (3.3V), Digital I/Os (3.3V)

Condition	3.3V Transceiver (VDDA_3.3)	3.3V Digital I/Os (VDDIO)	Total Chip Power
	mA	mA	mW
100Base-TX Link-up (no traffic)	34	12	152
100Base-TX Full-duplex @ 100% utilization	34	13	155
10Base-T Link-up (no traffic)	14	11	82.5
10Base-T Full-duplex @ 100% utilization	30	11	135
Power-saving mode (Reg. 1Fh, bit [10] = 1)	14	10	79.2
EDPD mode (Reg. 18h, bit [11] = 0)	10	10	66.0
EDPD mode (Reg. 18h, bit [11] = 0) and PLL off (Reg. 10h, bit [4] = 1)	3.77	1.54	17.5
Software power-down mode (Reg. 0h, bit [11] =1)	2.59	1.51	13.5
Software power-down mode (Reg. 0h, bit [11] =1) and slow-oscillator mode (Reg. 11h, bit [5] =1)	1.36	0.45	5.97

Table 10. Typical Current/Power Consumption (VDDA_3.3 = 3.3V, VDDIO = 3.3V)

Transceiver (3.3V), Digital I/Os (2.5V)

Condition	3.3V Transceiver (VDDA_3.3)	2.5V Digital I/Os (VDDIO)	Total Chip Power
	mA	mA	mW
100Base-TX Link-up (no traffic)	34	11	140
100Base-TX Full-duplex @ 100% utilization	34	12	142
10Base-T Link-up (no traffic)	15	10	74.5
10Base-T Full-duplex @ 100% utilization	27	10	114
Power-saving mode (Reg. 1Fh, bit [10] = 1)	15	10	74.5
EDPD mode (Reg. 18h, bit [11] = 0)	11	10	61.3
EDPD mode (Reg. 18h, bit [11] = 0) and PLL off (Reg. 10h, bit [4] = 1)	3.55	1.35	15.1
Software power-down mode (Reg. 0h, bit [11] =1)	2.29	1.34	10.9
Software power-down mode (Reg. 0h, bit [11] =1) and slow-oscillator mode (Reg. 11h, bit [5] =1)	1.15	0.29	4.52

Table 11. Typical Current/Power Consumption (VDDA_3.3 = 3.3V, VDDIO = 2.5V)

Transceiver (3.3V), Digital I/Os (1.8V)

Condition	3.3V Transceiver (VDDA_3.3)	1.8V Digital I/Os (VDDIO)	Total Chip Power
	mA	mA	mW
100Base-TX Link-up (no traffic)	34	11	132
100Base-TX Full-duplex @ 100% utilization	34	12	134
10Base-T Link-up (no traffic)	15	9.0	65.7
10Base-T Full-duplex @ 100% utilization	27	9.0	105
Power-saving mode (Reg. 1Fh, bit [10] = 1)	15	9.0	65.7
EDPD mode (Reg. 18h, bit [11] = 0)	11	9.0	52.5
EDPD mode (Reg. 18h, bit [11] = 0) and PLL off (Reg. 10h, bit [4] = 1)	4.05	1.21	15.5
Software power-down mode (Reg. 0h, bit [11] =1)	2.79	1.21	11.4
Software power-down mode (Reg. 0h, bit [11] =1) and slow-oscillator mode (Reg. 11h, bit [5] =1)	1.65	0.19	5.79

Table 12. Typical Current/Power Consumption (VDDA_3.3 = 3.3V, VDDIO = 1.8V)

Register Map

Register Number (Hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h	Reserved
10h	Digital Reserved Control
11h	AFE Control 1
12h – 14h	Reserved
15h	RXER Counter
16h	Operation Mode Strap Override
17h	Operation Mode Strap Status
18h	Expanded Control
19h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch	Reserved
1Dh	LinkMD Control/Status
1Eh	PHY Control 1
1Fh	PHY Control 2

Register Description

Address	Name	Description	Mode[1]	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.14	Loopback	1 = Loopback mode 0 = Normal operation	RW	0
0.13	Speed Select	1 = 100Mbps 0 = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	Set by the SPEED strapping pin. See the "Strapping Options" section for details.
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, the auto-negotiation result overrides the settings in registers 0.13 and 0.8.	RW	Set by the NWAYEN strapping pin. See the "Strapping Options" section for details.
0.11	Power-Down	1 = Power-down mode 0 = Normal operation If software reset (register 0.15) is used to exit power-down mode (register 0.11 = 1), two software reset writes (register 0.15 = 1) are required. The first write clears power-down mode; the second write resets the chip and re-latches the pin strapping pin values.	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII/RMII 0 = Normal operation	RW	Set by the ISO strapping pin. See the "Strapping Options" section for details.
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	The inverse of the DUPLEX strapping pin value. See the "Strapping Options" section for details.
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6:0	Reserved	Reserved	RO	000_0000
Register 1h – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full-Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex	RO	1
1.13	100Base-TX Half-Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex	RO	1
1.12	10Base-T Full-Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex	RO	1

Address	Name	Description	Mode[1]	Default
1.11	10Base-T Half-Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex	RO	1
1.10:7	Reserved	Reserved	RO	000_0
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Can perform auto-negotiation 0 = Cannot perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capability registers	RO	1
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex).	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex).	RO	0001_01
3.9:4	Model Number	Six-bit manufacturer's model number	RO	01_0110
3.3:0	Revision Number	Four-bit manufacturer's revision number	RO	Indicates silicon revision
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability	RW	0
4.14	Reserved	Reserved	RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved	Reserved	RO	0
4.11:10	Pause	[00] = No pause [10] = Asymmetric pause [01] = Symmetric pause [11] = Asymmetric and symmetric pause	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0

Address	Name	Description	Mode(1)	Default
4.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	Set by the SPEED strapping pin. See the "Strapping Options" section for details.
4.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	Set by the SPEED strapping pin. See the "Strapping Options" section for details.
4.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved	Reserved	RO	0
5.11:10	Pause	[00] = No pause [10] = Asymmetric pause [01] = Symmetric pause [11] = Asymmetric and symmetric pause	RO	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved	Reserved	RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1

Address	Name	Description	Mode(1)	Default
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next pages will follow 0 = Last page	RW	0
7.14	Reserved	Reserved	RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic 1 0 = Logic 0	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = Additional next pages will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Can act on the information 0 = Cannot act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic 0 0 = Previous value of transmitted link code word equal to logic 1	RO	0
8.10:0	Message Field	11-bit wide field to encode 2048 messages	RO	000_0000_0000
Register 10h – Digital Reserved Control				
10.15:5	Reserved	Reserved	RW	0000_0000_000
10.4	PLL Off	1 = Turn PLL off automatically in EDPD mode 0 = Keep PLL on in EDPD mode. See also register 18h, bit [11] for EDPD mode	RW	0
10.3:0	Reserved	Reserved	RW	0000
Register 11h – AFE Control 1				
11.15:6	Reserved	Reserved	RW	0000_0000_00

Address	Name	Description	Mode(1)	Default
11.5	Slow-Oscillator Mode Enable	Slow-oscillator mode is used to disconnect the input reference crystal/clock on the XI pin and select the on-chip slow oscillator when the KSZ8081MNX/RNB device is not in use after power-up. 1 = Enable 0 = Disable This bit automatically sets software power-down to the analog side when enabled.	RW	0
11.4:0	Reserved	Reserved	RW	0_0000
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for symbol error frames	RO/SC	0000h
Register 16h – Operation Mode Strap Override				
16.15:11	Reserved	Reserved	RW	0000_0
16.10	Reserved	Reserved	RO	0
16.9	B-CAST_OFF Override	1 = Override strap-in for B-CAST_OFF If bit is '1', PHY Address 0 is non-broadcast.	RW	0
16.8	Reserved	Reserved	RW	0
16.7	MII B-to-B Override	1 = Override strap-in for MII back-to-back mode (also set bit 0 of this register to '1') This bit applies only to KSZ8081MNX.	RW	0
16.6	RMII B-to-B Override	1 = Override strap-in for RMII Back-to-Back mode (also set bit 1 of this register to '1') This bit applies only to KSZ8081RNB.	RW	0
16.5	NAND Tree Override	1 = Override strap-in for NAND tree mode	RW	0
16.4:2	Reserved	Reserved	RW	0_00
16.1	RMII Override	1 = Override strap-in for RMII mode This bit applies only to KSZ8081RNB.	RW	0
16.0	MII Override	1 = Override strap-in for MII mode This bit applies only to KSZ8081MNX.	RW	1
Register 17h – Operation Mode Strap Status				
17.15:13	PHYAD[2:0] Strap-In Status	[000] = Strap to PHY Address 0 [001] = Strap to PHY Address 1 [010] = Strap to PHY Address 2 [011] = Strap to PHY Address 3 [100] = Strap to PHY Address 4 [101] = Strap to PHY Address 5 [110] = Strap to PHY Address 6 [111] = Strap to PHY Address 7	RO	
17.12:10	Reserved	Reserved	RO	
17.9	B-CAST_OFF Strap-In Status	1 = Strap to B-CAST_OFF If bit is '1', PHY Address 0 is non-broadcast.	RO	
17.8	Reserved	Reserved	RO	

Address	Name	Description	Mode(1)	Default
17.7	MII B-to-B Strap-In Status	1 = Strap to MII back-to-back mode This bit applies only to KSZ8081MNX.	RO	
17.6	RMII B-to-B Strap-In Status	1 = Strap to RMII Back-to-Back mode This bit applies only to KSZ8081RNB.	RO	
17.5	NAND Tree Strap-In Status	1 = Strap to NAND tree mode	RO	
17.4:2	Reserved	Reserved	RO	
17.1	RMII Strap-In Status	1 = Strap to RMII mode This bit applies only to KSZ8081RNB.	RO	
17.0	MII Strap-In Status	1 = Strap to MII mode This bit applies only to KSZ8081MNX.	RO	
Register 18h – Expanded Control				
18.15:12	Reserved	Reserved	RW	0000
18.11	EDPD Disabled	Energy-detect power-down mode 1 = Disable 0 = Enable See also register 10h, bit [4] for PLL off.	RW	1
18.10	100Base-TX Latency	1 = MII output is random latency 0 = MII output is fixed latency For both settings, all bytes of received preamble are passed to the MII output. This bit applies only to KSZ8081MNX.	RW	0
18.9:7	Reserved	Reserved	RW	00_0
18.6	10Base-T Preamble Restore	1 = Restore received preamble to MII output 0 = Remove all seven bytes of preamble before sending frame (starting with SFD) to MII output This bit applies only to KSZ8081MNX	RW	0
18.5:0	Reserved	Reserved	RW	00_0000
Register 1Bh – Interrupt Control/Status				
1B.15	Jabber Interrupt Enable	1 = Enable jabber interrupt 0 = Disable jabber interrupt	RW	0
1B.14	Receive Error Interrupt Enable	1 = Enable receive error interrupt 0 = Disable receive error interrupt	RW	0
1B.13	Page Received Interrupt Enable	1 = Enable page received interrupt 0 = Disable page received interrupt	RW	0
1B.12	Parallel Detect Fault Interrupt Enable	1 = Enable parallel detect fault interrupt 0 = Disable parallel detect fault interrupt	RW	0
1B.11	Link Partner Acknowledge Interrupt Enable	1 = Enable link partner acknowledge interrupt 0 = Disable link partner acknowledge interrupt	RW	0

Address	Name	Description	Mode(1)	Default
1B.10	Link-Down Interrupt Enable	1= Enable link-down interrupt 0 = Disable link-down interrupt	RW	0
1B.9	Remote Fault Interrupt Enable	1 = Enable remote fault interrupt 0 = Disable remote fault interrupt	RW	0
1B.8	Link-Up Interrupt Enable	1 = Enable link-up interrupt 0 = Disable link-up interrupt	RW	0
1B.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occur	RO/SC	0
1B.6	Receive Error Interrupt	1 = Receive error occurred 0 = Receive error did not occur	RO/SC	0
1B.5	Page Receive Interrupt	1 = Page receive occurred 0 = Page receive did not occur	RO/SC	0
1B.4	Parallel Detect Fault Interrupt	1 = Parallel detect fault occurred 0 = Parallel detect fault did not occur	RO/SC	0
1B.3	Link Partner Acknowledge Interrupt	1 = Link partner acknowledge occurred 0 = Link partner acknowledge did not occur	RO/SC	0
1B.2	Link-Down Interrupt	1 = Link-down occurred 0 = Link-down did not occur	RO/SC	0
1B.1	Remote Fault Interrupt	1 = Remote fault occurred 0 = Remote fault did not occur	RO/SC	0
1B.0	Link-Up Interrupt	1 = Link-up occurred 0 = Link-up did not occur	RO/SC	0
Register 1Dh – LinkMD Control/Status				
1D.15	Cable Diagnostic Test Enable	1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0
1D.14:13	Cable Diagnostic Test Result	[00] = Normal condition [01] = Open condition has been detected in cable [10] = Short condition has been detected in cable [11] = Cable diagnostic test has failed	RO	00
1D.12	Short Cable Indicator	1 = Short cable (<10 meter) has been detected by LinkMD	RO	0
1D.11:9	Reserved	Reserved	RW	000
1D.8:0	Cable Fault Counter	Distance to fault	RO	0_0000_0000
Register 1Eh – PHY Control 1				
1E.15:10	Reserved	Reserved	RO	0000_00
1E.9	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0

Address	Name	Description	Mode(1)	Default
1E.8	Link Status	1 = Link is up 0 = Link is down	RO	0
1E.7	Polarity Status	1 = Polarity is reversed 0 = Polarity is not reversed	RO	
1E.6	Reserved	Reserved	RO	0
1E.5	MDI/MDI-X State	1 = MDI-X 0 = MDI	RO	
1E.4	Energy Detect	1 = Signal present on receive differential pair 0 = No signal detected on receive differential pair	RO	0
1E.3	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RW	0
1E.2:0	Operation Mode Indication	[000] = Still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = Reserved [100] = Reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = Reserved	RO	000
Register 1Fh – PHY Control 2				
1F.15	HP_MDIX	1 = HP Auto MDI/MDI-X mode 0 = Micrel Auto MDI/MDI-X mode	RW	1
1F.14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 1 = MDI-X mode Transmit on RXP,RXM (pins 5, 4) and Receive on TXP,TXM (pins 7, 6) 0 = MDI mode Transmit on TXP,TXM (pins 7, 6) and Receive on RXP,RXM (pins 5, 4)	RW	0
1F.13	Pair Swap Disable	1 = Disable Auto MDI/MDI-X 0 = Enable Auto MDI/MDI-X	RW	0
1F.12	Reserved	Reserved	RW	0
1F.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allows the transmitter to send a pattern even if there is no link.	RW	0
1F.10	Power Saving	1 = Enable power saving 0 = Disable power saving	RW	0
1F.9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1F.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1

Address	Name	Description	Mode[(1)]	Default
1F.7	RMII Reference Clock Select	1 = RMII 50MHz clock mode; clock input to XI (pin 9) is 50MHz 0 = RMII 25MHz clock mode; clock input to XI (pin 9) is 25MHz This bit applies only to KSZ8081RNB.	RW	0
1F.6	Reserved	Reserved	RW	0
1F.5:4	LED Mode	[00] = LED1: Speed LED0: Link/Activity [01] = LED1: Activity LED0: Link [10], [11] = Reserved	RW	00
1F.3	Disable Transmitter	1 = Disable transmitter 0 = Enable transmitter	RW	0
1F.2	Remote Loopback	1 = Remote (analog) loopback is enabled 0 = Normal mode	RW	0
1F.1	Enable SQE Test	1 = Enable SQE test 0 = Disable SQE test	RW	0
1F.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Note:

1. RW = Read/Write.
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.
   LL = Latch low.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN})
- ($V_{DD\_1.2}$) .... –0.5V to +1.8V
- (V_{DDIO}, $V_{DDA\_3.3}$) .... –0.5V to +5.0V

Input Voltage (all inputs) .... –0.5V to +5.0V
Output Voltage (all outputs) .... –0.5V to +5.0V
Lead Temperature (soldering, 10sec.) .... 260°C
Storage Temperature (T_s) .... –55°C to +150°C

Operating Ratings[2]

Supply Voltage
- ($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) .... +3.135V to +3.465V
- ($V_{DDIO\_2.5}$) .... +2.375V to +2.625V
- ($V_{DDIO\_1.8}$) .... +1.710V to +1.890V

Ambient Temperature
- (T_A , Commercial) .... 0°C to +70°C
- (T_A , Industrial) .... –40°C to +85°C

Maximum Junction Temperature (T_J max.) .... 125°C
Thermal Resistance (θ_{JA}) .... 34°C/W
Thermal Resistance (θ_{JC}) .... 6°C/W

Electrical Characteristics[3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current (V_{DDIO}, $V_{DDA\_3.3}$ = 3.3V)[4]						
$I_{DD1\_3.3V}$	10Base-T	Full-duplex traffic @ 100% utilization		41		mA
$I_{DD2\_3.3V}$	100Base-TX	Full-duplex traffic @ 100% utilization		47		mA
$I_{DD3\_3.3V}$	EDPD Mode	Ethernet cable disconnected (reg. 18h.11 = 0)		20		mA
$I_{DD4\_3.3V}$	Power-Down Mode	Software power-down (reg. 0h.11 = 1)		4		mA
CMOS Level Inputs						
V_{IH}	Input High Voltage	V_{DDIO} = 3.3V	2.0			V
		V_{DDIO} = 2.5V	1.8			V
		V_{DDIO} = 1.8V	1.3			V
V_{IL}	Input Low Voltage	V_{DDIO} = 3.3V			0.8	V
		V_{DDIO} = 2.5V			0.7	V
		V_{DDIO} = 1.8V			0.5	V
$\|I_{IN}\|$	Input Current	V_{IN} = GND ~ VDDIO			10	µA
CMOS Level Outputs						
V_{OH}	Output High Voltage	V_{DDIO} = 3.3V	2.4			V
		V_{DDIO} = 2.5V	2.0			V
		V_{DDIO} = 1.8V	1.5			V
V_{OL}	Output Low Voltage	V_{DDIO} = 3.3V			0.4	V
		V_{DDIO} = 2.5V			0.4	V
		V_{DDIO} = 1.8V			0.3	V
$\|I_{oz}\|$	Output Tri-State Leakage				10	µA
LED Output						
I_{LED}	Output Drive Current	Each LED pin (LED0, LED1)		8		mA

Notes:

1. Exceeding the absolute maximum rating can damage the device. Stresses greater than the absolute maximum rating can cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. The device is not guaranteed to function outside its operating rating.
3. T_A = 25°C. Specification is for packaged product only.
4. Current consumption is for the single 3.3V supply KSZ8081MNX/RNB device only, and includes the transmit driver current and the 1.2V supply voltage ($V_{DD\_1.2}$) that are supplied by the KSZ8081MNX/RNB.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
All Pull-Up/Pull-Down Pins (including Strapping Pins)						
pu	Internal Pull-Up Resistance	V_{DDIO} = 3.3V	30	45	73	kΩ
		V_{DDIO} = 2.5V	39	61	102	kΩ
		V_{DDIO} = 1.8V	48	99	178	kΩ
pd	Internal Pull-Down Resistance	V_{DDIO} = 3.3V	26	43	79	kΩ
		V_{DDIO} = 2.5V	34	59	113	kΩ
		V_{DDIO} = 1.8V	53	99	200	kΩ
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				±0.25	ns
	Overshoot				5	%
	Output Jitter	Peak-to-peak		0.7		ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
t_r, t_f	Rise/Fall Time			25		ns
10Base-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
Transmitter – Drive Setting						
V_{SET}	Reference Voltage of I_{SET}	$R(I_{SET})$ = 6.49kΩ		0.65		V
REF_CLK Output						
	50MHz RMII Clock Output Jitter	Peak-to-peak (Applies only to KSZ8081RNB in RMII – 25MHz clock mode)		300		ps
100Mbps Mode – Industrial Applications Parameters						
	Clock Phase Delay – XI Input to MII TXC Output	XI (25MHz clock input) to MII TXC (25MHz clock output) delay, referenced to rising edges of both clocks. (Applies only to KSZ8081MNX in MII mode)	15	20	25	ns
t_{llr}	Link Loss Reaction (Indication) Time	Link loss detected at receive differential inputs to PHY signal indication time for each of the following: 1. For LED mode 00, Speed LED output changes from low (100Mbps) to high (10Mbps, default state for link-down). 2. For LED mode 01, Link LED output changes from low (link-up) to high (link-down). 3. INTRP pin asserts for link-down status change.		4.4		μs

Timing Diagrams

MII SQE Timing (10Base-T)

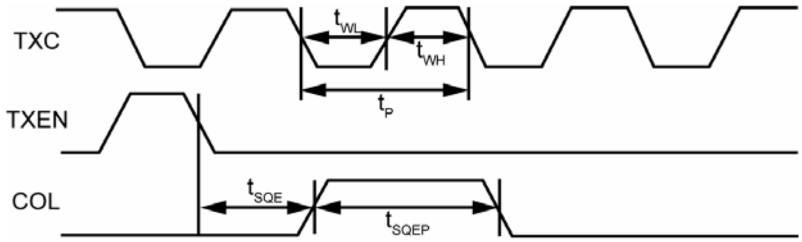


Figure 11. MII SQE Timing (10Base-T)

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	TXC period		400		ns
t_{WL}	TXC pulse width low		200		ns
t_{WH}	TXC pulse width high		200		ns
t_{SQE}	COL (SQE) delay after TXEN de-asserted		2.2		µs
t_{SQEP}	COL (SQE) pulse duration		1.0		µs

Table 13. MII SQE Timing (10Base-T) Parameters

MII Transmit Timing (10Base-T)

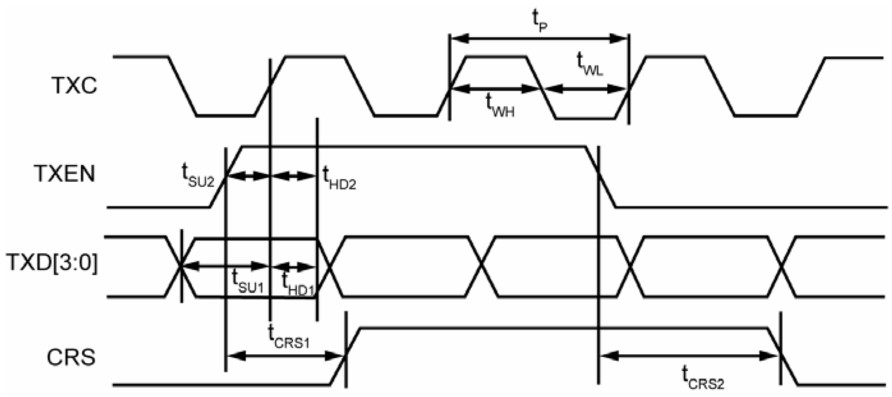


Figure 12. MII Transmit Timing (10Base-T)

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	TXC period		400		ns
t_{WL}	TXC pulse width low		200		ns
t_{WH}	TXC pulse width high		200		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	120			ns
t_{SU2}	TXEN setup to rising edge of TXC	120			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		600		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		1.0		μs

Table 14. MII Transmit Timing (10Base-T) Parameters

MII Receive Timing (10Base-T)

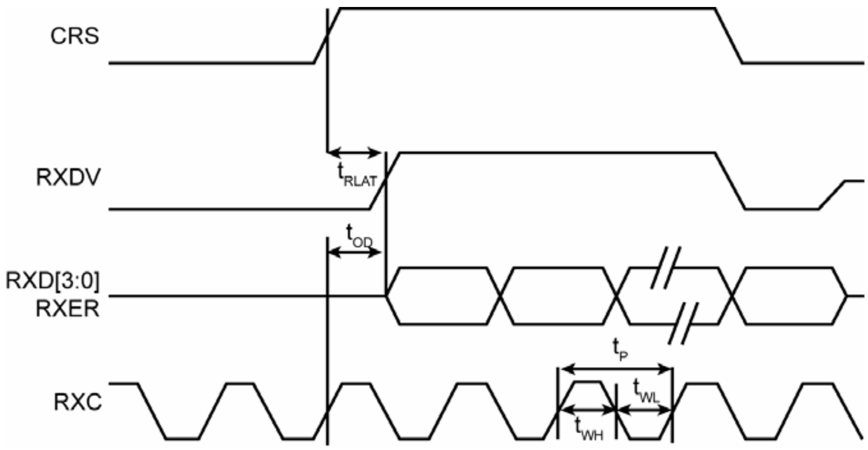


Figure 13. MII Receive Timing (10Base-T)

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	RXC period		400		ns
t_{WL}	RXC pulse width low		200		ns
t_{WH}	RXC pulse width high		200		ns
t_{OD}	(RXDV, RXD[3:0], RXER) output delay from rising edge of RXC		205		ns
t_{RLAT}	CRS to (RXDV, RXD[3:0]) latency		7.2		µs

Table 15. MII Receive Timing (10Base-T) Parameters

MII Transmit Timing (100Base-TX)

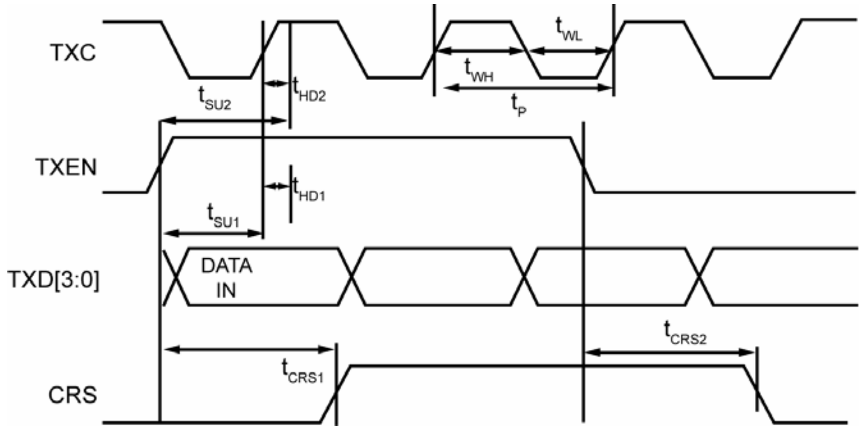


Figure 14. MII Transmit Timing (100Base-TX)

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	TXC period		40		ns
t_{WL}	TXC pulse width low		20		ns
t_{WH}	TXC pulse width high		20		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	10			ns
t_{SU2}	TXEN setup to rising edge of TXC	10			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		72		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		72		ns

Table 16. MII Transmit Timing (100Base-TX) Parameters

MII Receive Timing (100Base-TX)

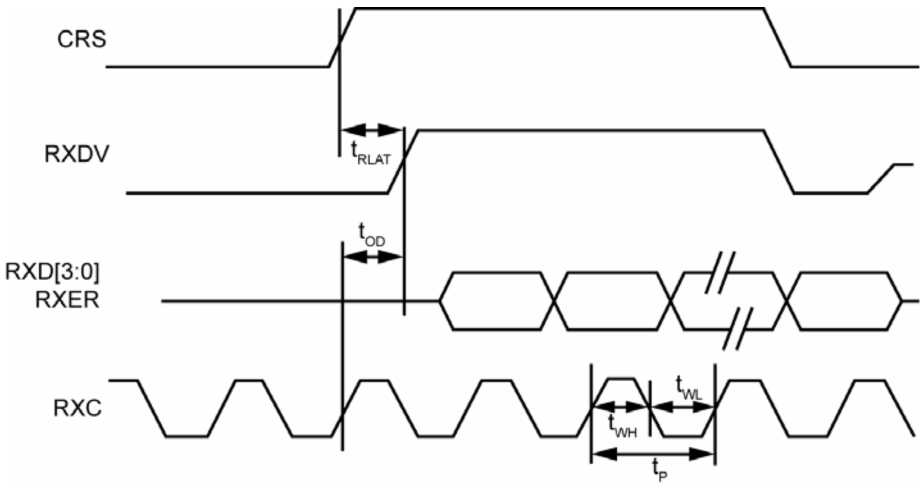


Figure 15. MII Receive Timing (100Base-TX)

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	RXC period		40		ns
t_{WL}	RXC pulse width low		20		ns
t_{WH}	RXC pulse width high		20		ns
t_{OD}	(RXDV, RXD[3:0], RXER) output delay from rising edge of RXC		25		ns
t_{RLAT}	CRS to (RXDV, RXD[3:0] latency		170		ns

Table 17. MII Receive Timing (100Base-TX) Parameters

RMII Timing

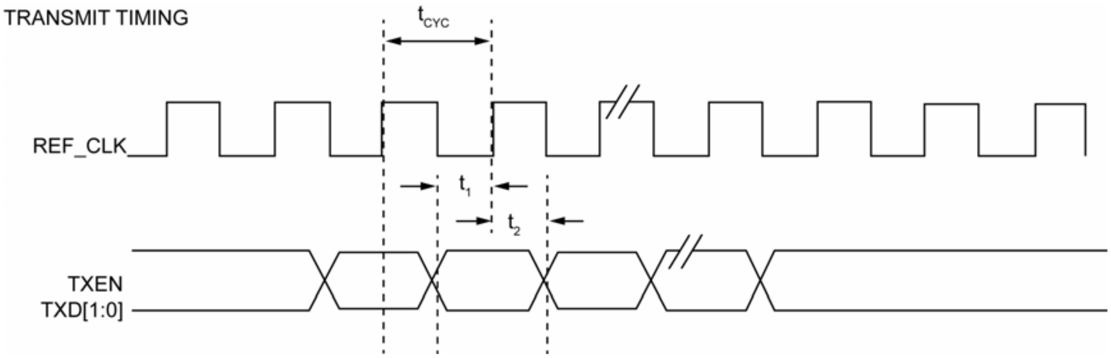


Figure 16. RMII Timing – Data Received from RMII

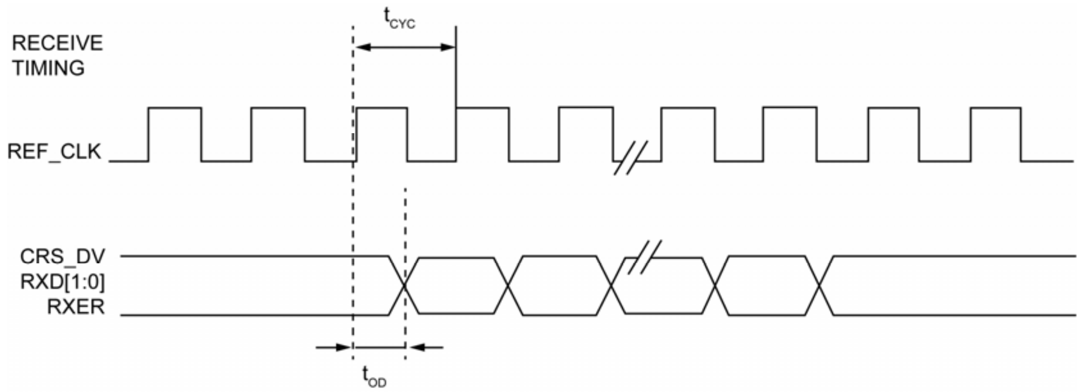


Figure 17. RMII Timing – Data Input to RMII

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_{CYC}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{OD}	Output delay	7	10	13	ns

Table 18. RMII Timing Parameters – KSZ8081RNB (25MHz input to XI pin, 50MHz output from REF_CLK pin)

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_{CYC}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{OD}	Output delay	8	11	13	ns

Table 19. RMII Timing Parameters – KSZ8081RNB (50MHz input to XI pin)

Auto-Negotiation Timing

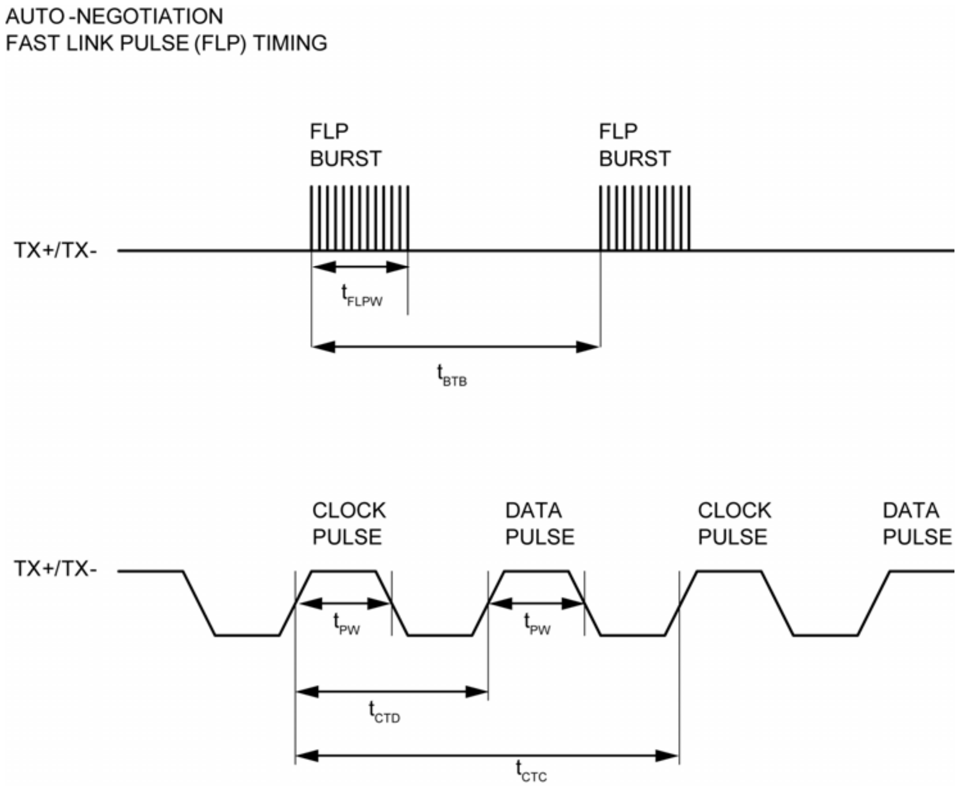


Figure 18. Auto-Negotiation Fast Link Pulse (FLP) Timing

Timing Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of clock/data pulses per FLP burst	17		33	

Table 20. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing

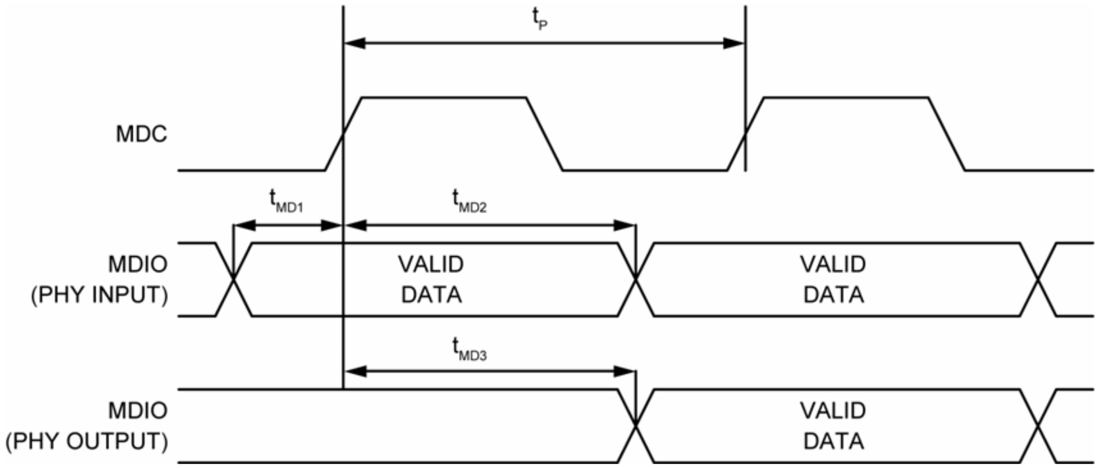


Figure 19. MDC/MDIO Timing

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	MDC period		400		ns
t_{MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	5			ns

Table 21. MDC/MDIO Timing Parameters

Power-Up/Reset Timing

The KSZ8081MNX/RNB reset timing requirement is summarized in Figure 20 and Table 22.

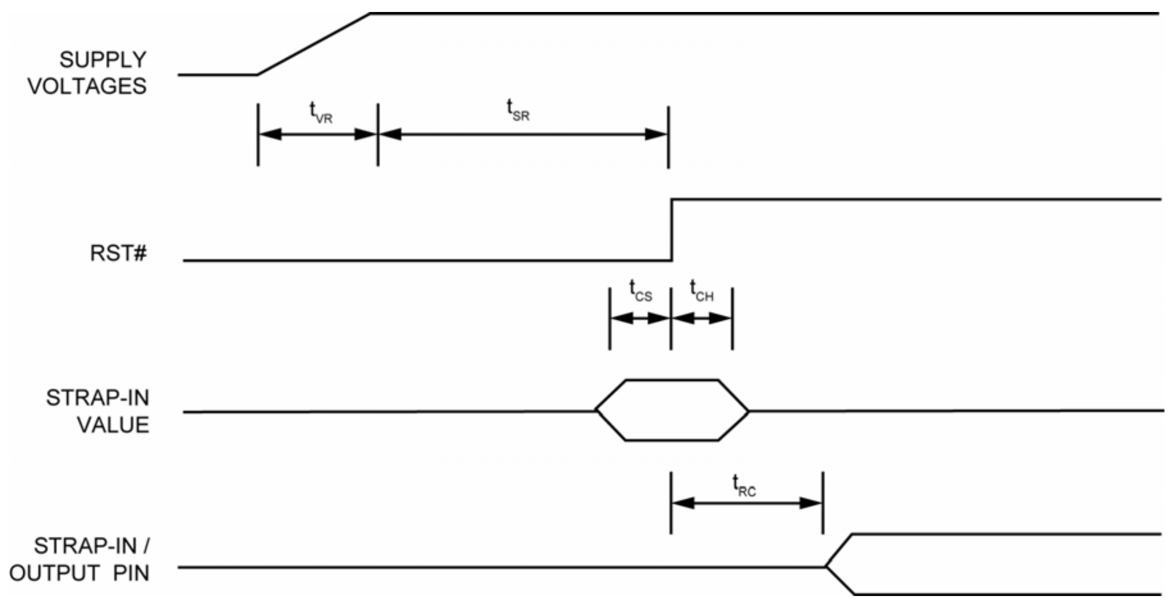


Figure 20. Power-Up/Reset Timing

Parameter	Description	Min.	Max.	Units
t_{VR}	Supply voltage (V_{DDIO}, $V_{DDA\_3.3}$) rise time	300		µs
t_{SR}	Stable supply voltage (V_{DDIO}, $V_{DDA\_3.3}$) to reset high	10		ms
t_{CS}	Configuration setup time	5		ns
t_{CH}	Configuration hold time	5		ns
t_{RC}	Reset to strap-in pin output	6		ns

Table 22. Power-Up/Reset Timing Parameters

The supply voltage (V_{DDIO} and $V_{DDA\_3.3}$) power-up waveform should be monotonic. The 300µs minimum rise time is from 10% to 90%.

For warm reset, the reset (RST#) pin should be asserted low for a minimum of 500µs. The strap-in pin values are read and updated at the de-assertion of reset.

After the de-assertion of reset, wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) interface.

Reset Circuit

Figure 21 shows a reset circuit recommended for powering up the KSZ8081MNX/RNB if reset is triggered by the power supply.

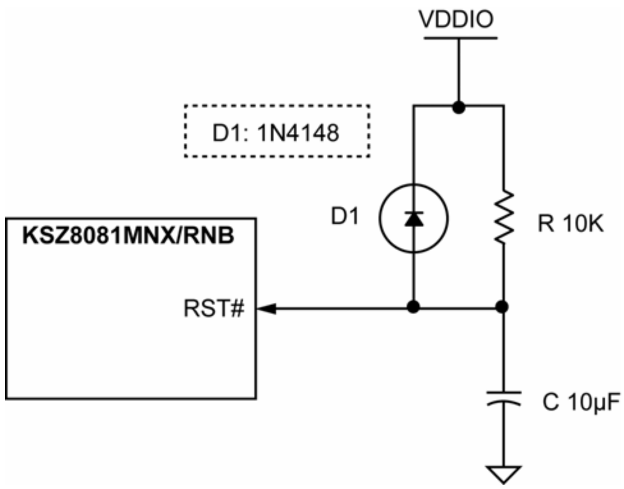


Figure 21. Recommended Reset Circuit

Figure 22 shows a reset circuit recommended for applications where reset is driven by another device (for example, the CPU or an FPGA). At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the KSZ8081MNX/RNB device. The RST_OUT_N from the CPU/FPGA provides the warm reset after power-up.

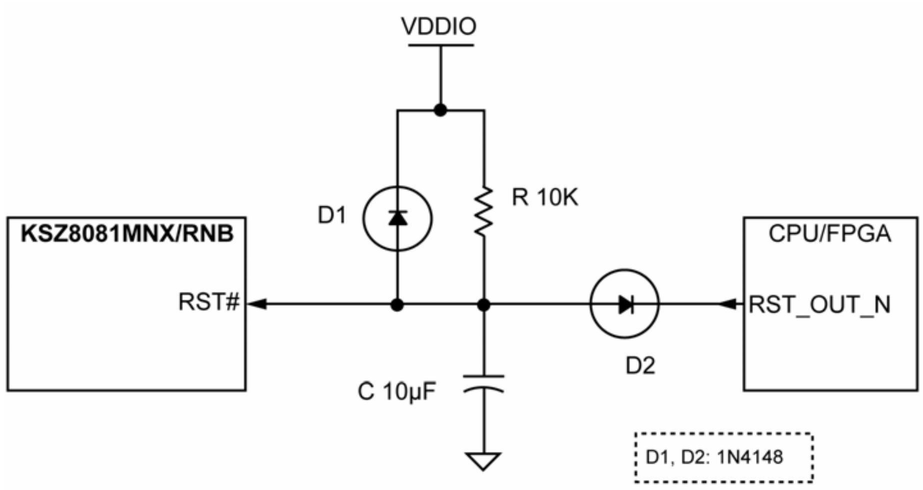


Figure 22. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output

Reference Circuits – LED Strap-In Pins

The pull-up, float, and pull-down reference circuits for the LED1/SPEED and LED0/NWAYEN strapping pins are shown in Figure 23 for 3.3V and 2.5V VDDIO.

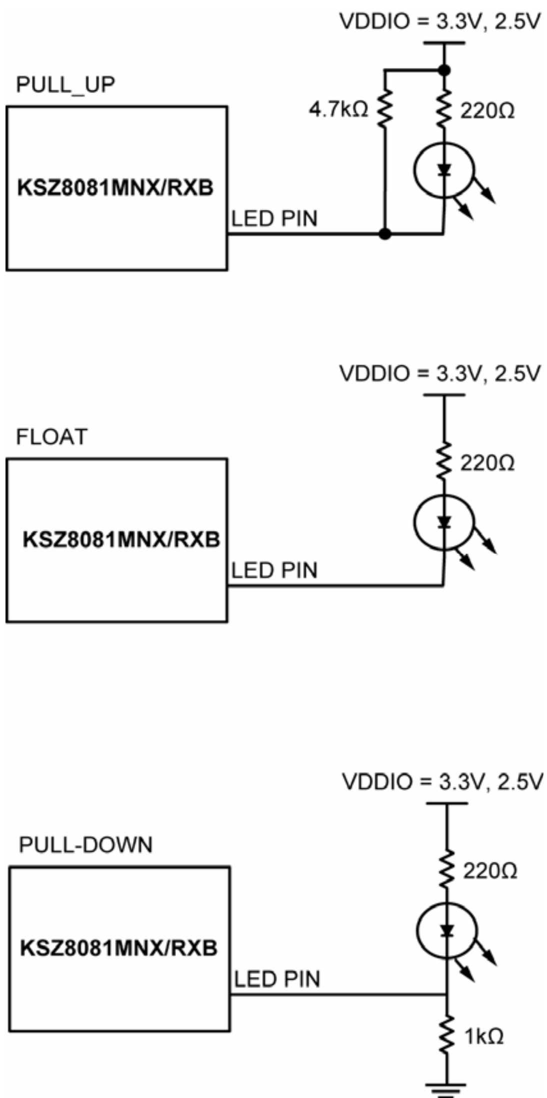


Figure 23. Reference Circuits for LED Strapping Pins

For 1.8V VDDIO, LED indication support is not recommended due to the low voltage. Without the LED indicator, the SPEED and NWAYEN strapping pins are functional with a 4.7kΩ pull-up to 1.8V VDDIO or float for a value of ‘1’, and with a 1.0kΩ pull-down to ground for a value of ‘0’.

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8081MNX/RNB. For the KSZ8081MNX in all operating modes and for the KSZ8081RNB in RMII – 25MHz Clock Mode, the reference clock is 25 MHz. The reference clock connections to XI (pin 9) and XO (pin 8), and the reference clock selection criteria, are provided in Figure 24 and Table 23.

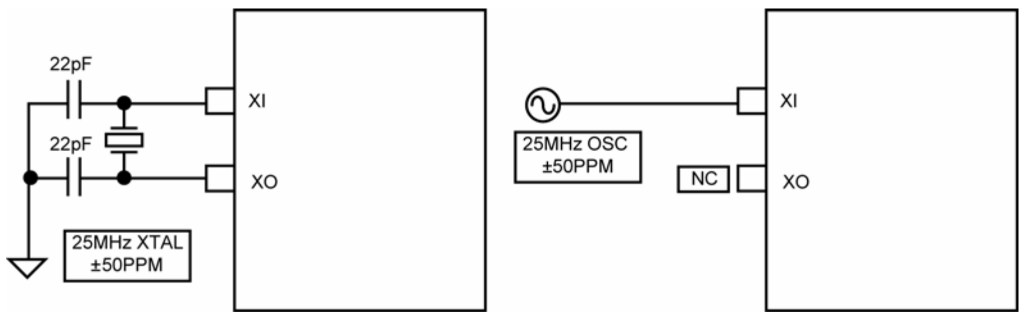


Figure 24. 25MHz Crystal/Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max.)	±50	ppm

Table 23. 25MHz Crystal / Reference Clock Selection Criteria

For the KSZ8081RNB in RMII – 50MHz clock mode, the reference clock is 50MHz. The reference clock connections to XI (pin 9), and the reference clock selection criteria are provided in Figure 25 and Table 24.

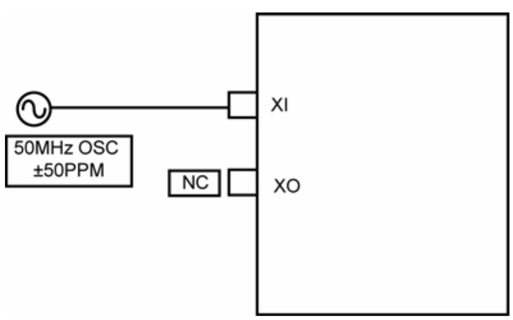


Figure 25. 50MHz Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	50	MHz
Frequency tolerance (max)	±50	ppm

Table 24. 50MHz Oscillator / Reference Clock Selection Criteria

Magnetic – Connection and Selection

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements.

The KSZ8081MNX/RNB design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the two differential pairs. Therefore, the two transformer center tap pins on the KSZ8081MNX/RNB side should not be connected to any power supply source on the board; instead, the center tap pins should be separated from one another and connected through separate 0.1µF common-mode capacitors to ground. Separation is required because the common-mode voltage is different between transmitting and receiving differential pairs.

Figure 26 shows the typical magnetic interface circuit for the KSZ8081MNX/RNB.

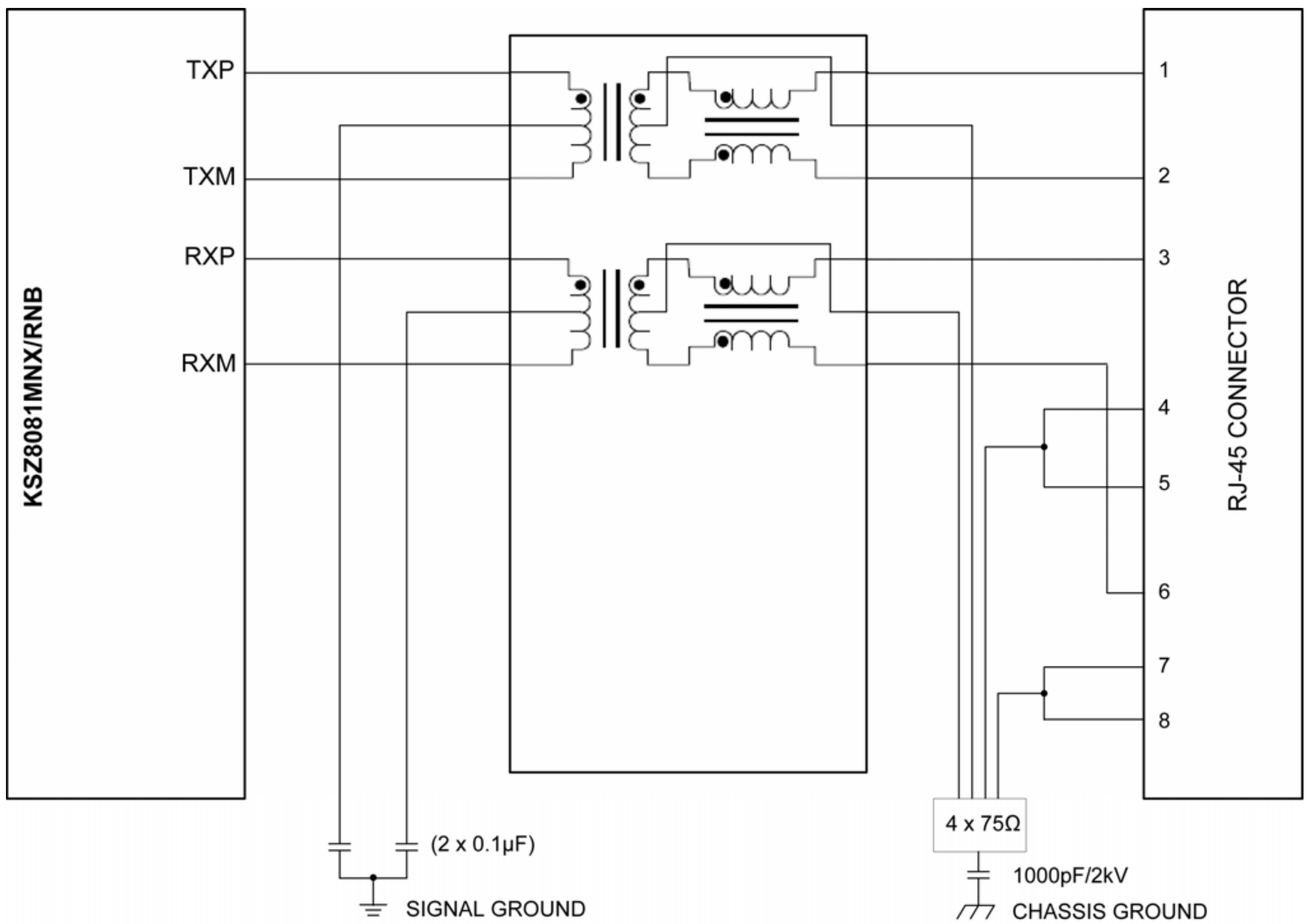


Figure 26. Typical Magnetic Interface Circuit

Table 25 lists recommended magnetic characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350µH	100mV, 100kHz, 8mA
Insertion loss (typ.)	–1.1dB	100kHz to 100MHz
HIPOT (min.)	1500Vrms	

Table 25. Magnetics Selection Criteria

Table 26 is a list of compatible single-port magnetics with separated transformer center tap pins on the PHY chip side that can be used with the KSZ8081MNX/RNB.

Manufacturer	Part Number	Temperature Range	Magnetic + RJ-45
Bel Fuse	S558-5999-U7	0°C to 70°C	No
Bel Fuse	SI-46001-F	0°C to 70°C	Yes
Bel Fuse	SI-50170-F	0°C to 70°C	Yes
Delta	LF8505	0°C to 70°C	No
HALO	HFJ11-2450E	0°C to 70°C	Yes
HALO	TG110-E055N5	–40°C to 85°C	No
LANKom	LF-H41S-1	0°C to 70°C	No
Pulse	H1102	0°C to 70°C	No
Pulse	H1260	0°C to 70°C	No
Pulse	HX1188	–40°C to 85°C	No
Pulse	J00-0014	0°C to 70°C	Yes
Pulse	JX0011D21NL	–40°C to 85°C	Yes
TDK	TLA-6T718A	0°C to 70°C	Yes
Transpower	HB726	0°C to 70°C	No
Wurth/Midcom	000-7090-37R-LF1	–40°C to 85°C	No

Table 26. Compatible Single-Port 10/100 Magnetics

Recommended Land Pattern

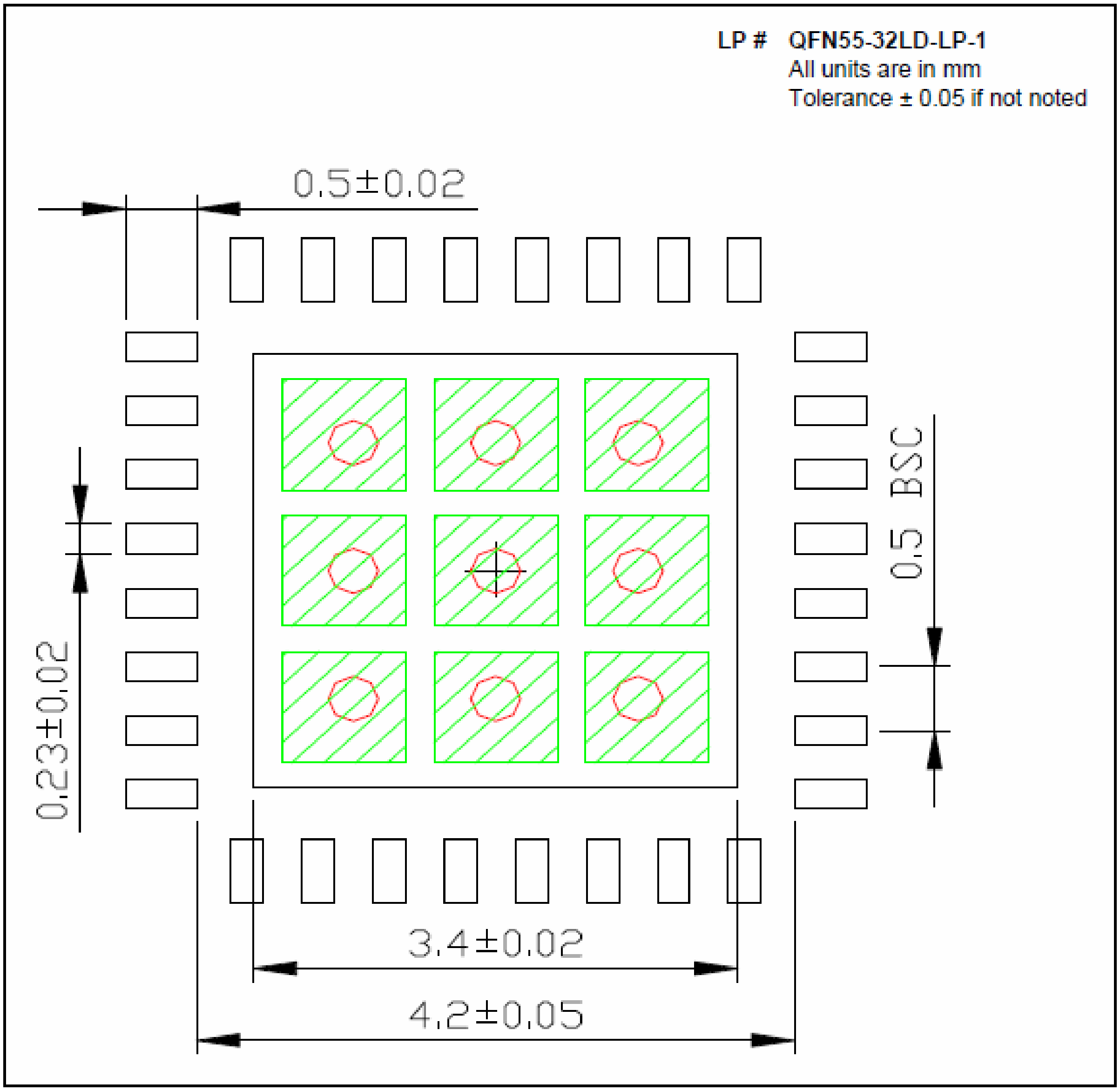
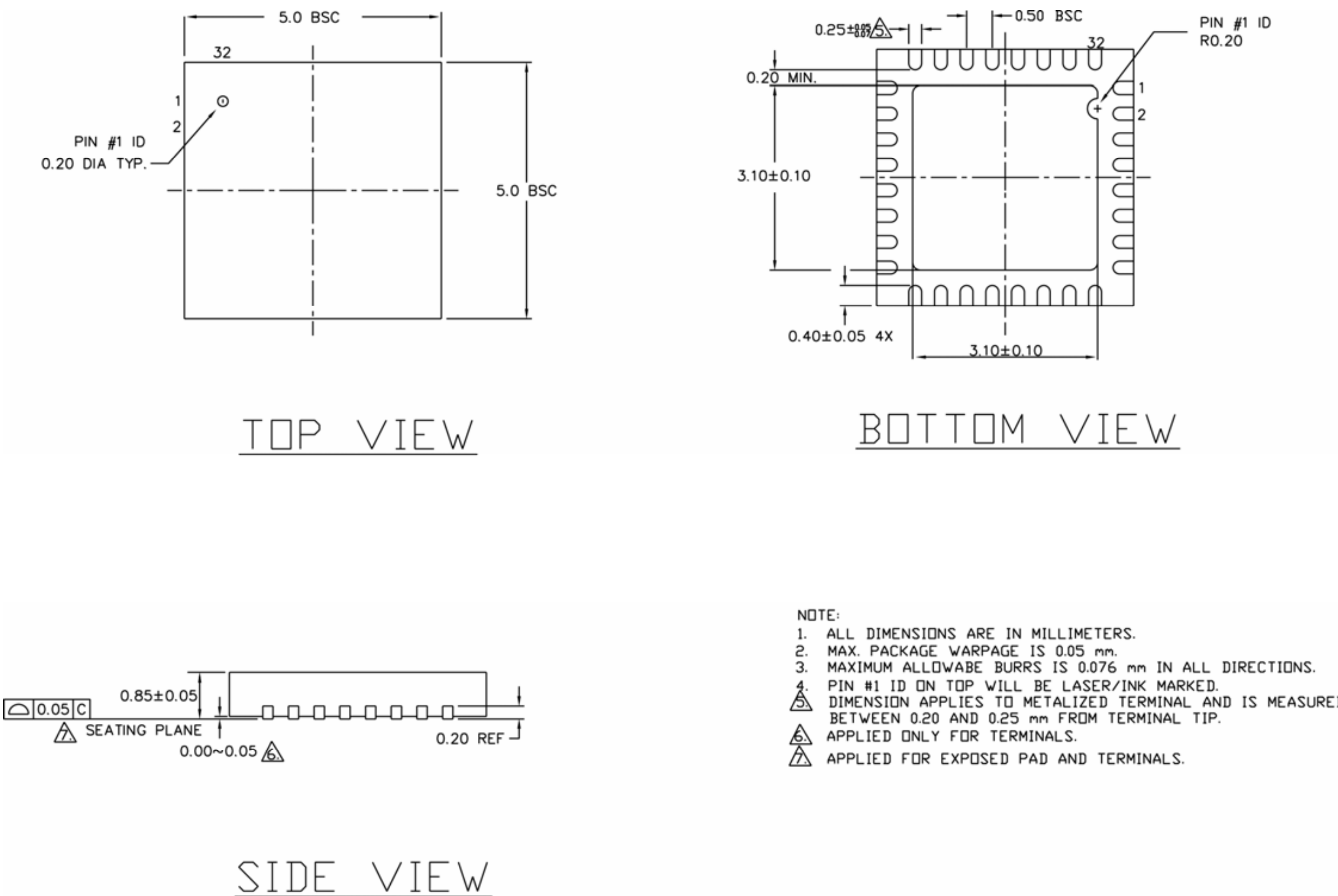


Figure 27. Recommended Land Pattern, 32-Pin (5mm x 5mm) QFN

Red circles indicate thermal vias. They should be 0.350mm in diameter and be connected to the GND plane for maximum thermal performance.

Green rectangles (with shaded area) indicate solder stencil openings on the exposed pad area. They should be 0.87 x 0.87mm in size, 1.07mm pitch.

Package Information[1]



32-Pin (5mm x 5mm) QFN

Note:

1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com. (Micrel note body)

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