MC74HC4094A

8-Bit Shift and Store Register

High−Performance Silicon−Gate CMOS

The MC74HC4094A is a high speed CMOS 8−bit serial shift and storage register. This device consists of an 8−bit shift register and latch with 3−state output buffers. Data is shifted on positive clock (CP) transitions. The data in the shift register is transferred to the storage register when the Strobe (STR) input is high. The output buffers are enabled when the Output Enable (OE) input is set high. Two serial outputs (QS_1, QS_2) are available for cascading multiple devices.

Features

- Wide Operating Voltage Range: 2.0 to 6.0 V
- Low Power Dissipation: I_{CC} = < 10 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Serial−to−Parallel Conversion
- Remote Control Storage Register

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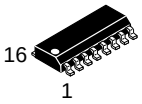
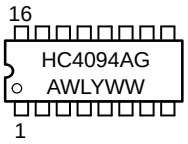
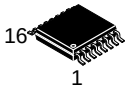
MARKING DIAGRAMS

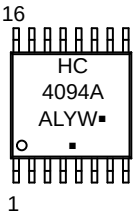


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G, ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

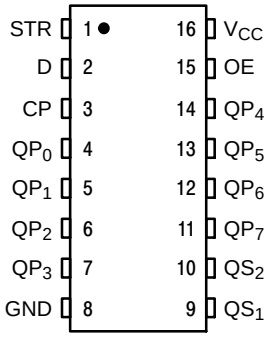


Figure 1. Pin Assignment

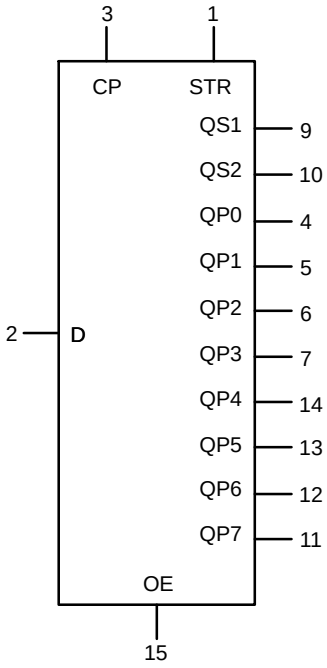


Figure 2. Logic Symbol

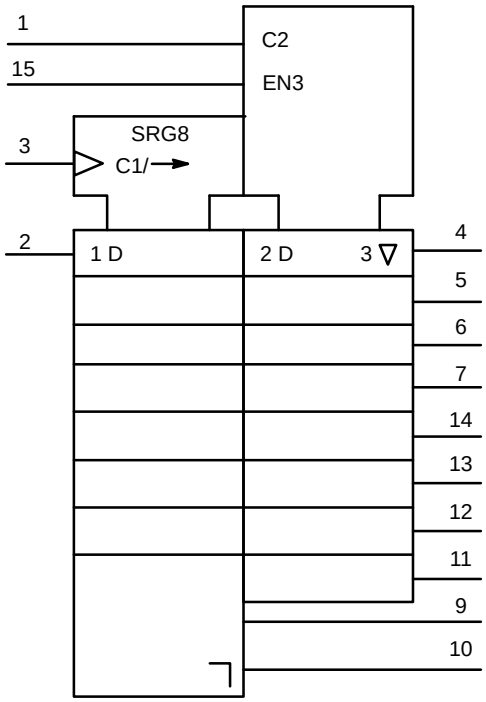


Figure 3. IEC Logic Symbol

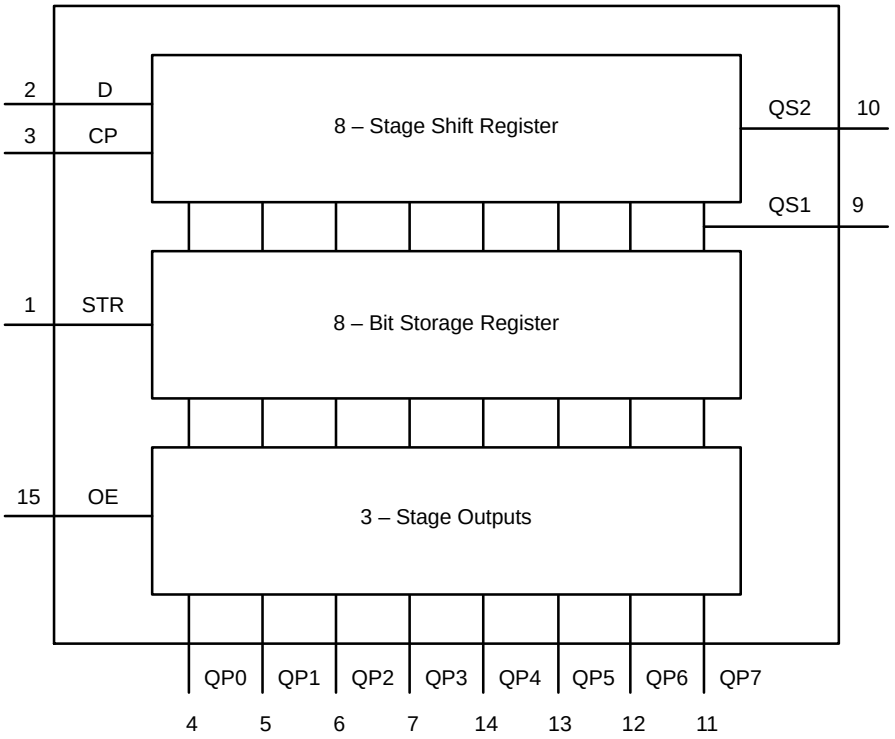


Figure 4. Functional Diagram

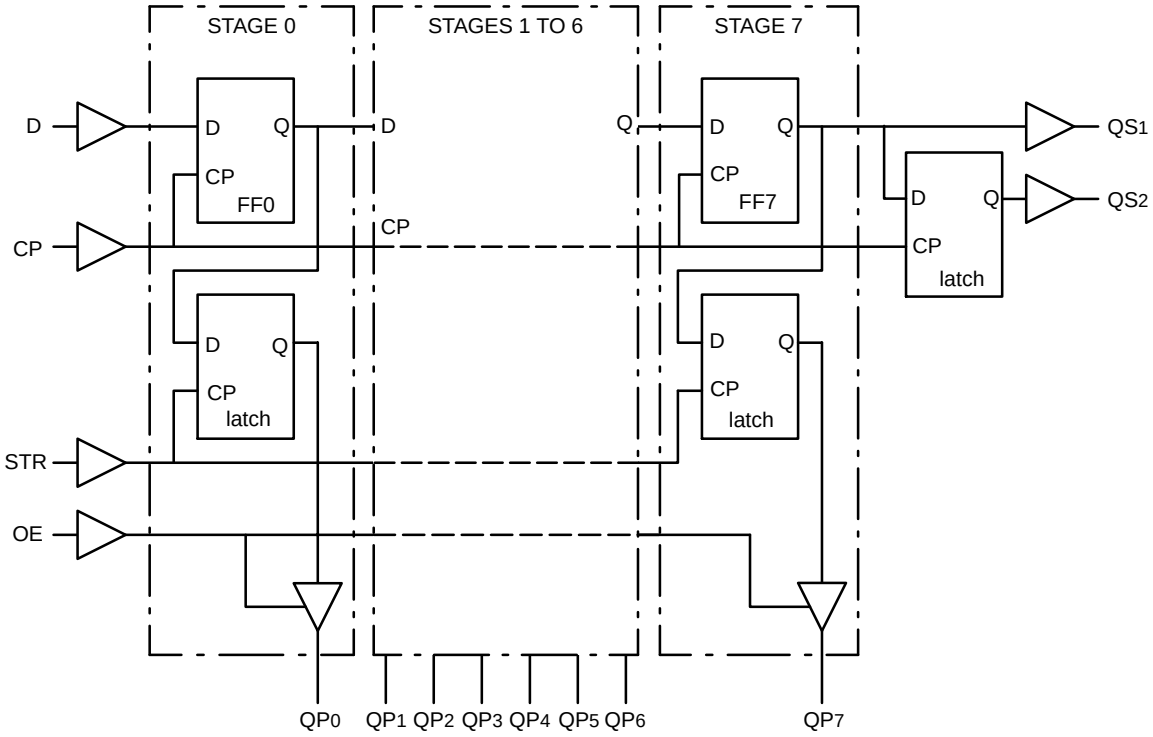


Figure 5. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating − SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

FUNCTIONAL TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	QP7
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	QPn−1	Q'6	NC
↑	H	H	H	H	QPn−1	Q'6	NC
↓	H	H	H	NC	NC	NC	QP7

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   Z = high impedance OFF−state
   NC = no change
   ↑ = LOW−to−HIGH CP transition
   ↓ = HIGH−to−LOW CP transition
   Q'6 = the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

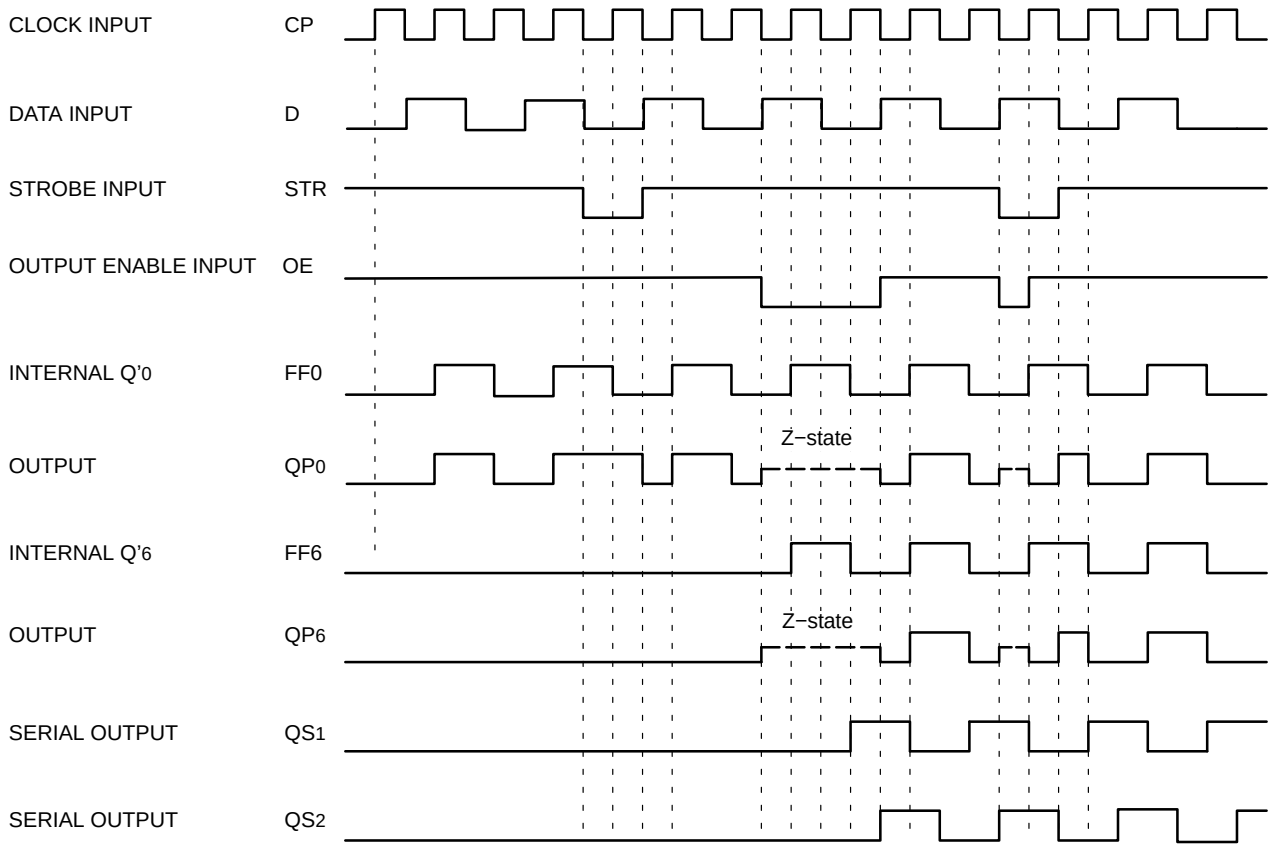


Figure 6. Timing Diagram

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				−55°C to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V_{OH}	Minimum High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20 μA	2.0	1.9	1.9	1.9	V
			3.0	2.9	2.9	2.9	
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 2.4 mA	3.0	2.75	2.7	2.6	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4 mA	4.5	4.25	4.2	4.1	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 5.2 mA	6.0	5.75	5.7	5.6	
V_{OL}	Maximum Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ ≤ 20 μA	2.0	0.1	0.1	0.1	V
			3.0	0.1	0.1	0.1	
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 2.4 mA	3.0	0.25	0.3	0.4	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4 mA	4.5	0.25	0.3	0.4	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 5.2 mA	6.0	0.25	0.3	0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	6.0	±0.1	±1	±1	μA
I_{OZ}	Maximum Tri−State Output Leakage Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC} or GND	6.0	±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0	4.0	40	80	μA

AC CHARACTERISTICS ($t_f = t_r$ = 6 ns, C_L = 50 pF)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				−55°C to 25°C	≤ 85°C	≤ 125°C	
t_{PHL}, t_{PLH}	Maximum Propagation Delay CP to QS_1	Figure 7	2.0	120	150	170	ns
			3.0	90	100	110	
			4.5	30	38	45	
			6.0	26	33	38	
t_{PHL}, t_{PLH}	Maximum Propagation Delay CP to QS_2	Figure 7	2.0	120	150	170	ns
			3.0	90	100	110	
			4.5	27	34	41	
			6.0	23	29	35	
t_{PHL}, t_{PLH}	Maximum Propagation Delay CP to QP_n	Figure 7	2.0	120	150	170	ns
			3.0	90	100	110	
			4.5	39	49	59	
			6.0	33	42	50	
t_{PHL}, t_{PLH}	Maximum Propagation Delay STR to QP_n	Figure 8	2.0	120	150	170	ns
			3.0	90	100	110	
			4.5	36	45	54	
			6.0	31	38	46	
t_{PZH}, t_{PZL}	Maximum 3−State Output Enable Time OE to QP_n	Figure 9	2.0	120	140	160	ns
			3.0	80	100	120	
			4.5	35	44	53	
			6.0	30	37	45	
t_{PHZ}, t_{PLZ}	Maximum 3−State Output Enable Time OE to QP_n	Figure 9	2.0	100	120	140	ns
			3.0	70	90	110	
			4.5	25	31	38	
			6.0	21	26	32	
t_{THL}, t_{TLH}	Maximum Output Transition Time	Figure 7	2.0	70	90	110	ns
			3.0	40	60	80	
			4.5	18	22	25	
			6.0	16	19	22	
t_W	Minimum Clock Pulse Width High or Low	Figure 7	2.0	80	100	120	ns
			3.0	50	60	80	
			4.5	16	20	24	
			6.0	14	17	20	
t_W	Minimum Strobe Pulse Width High	Figure 8	2.0	80	100	120	ns
			3.0	50	60	80	
			4.5	16	20	24	
			6.0	14	17	20	
t_{SU}	Minimum Set−up Time D to CP	Figure 10	2.0	50	65	75	ns
			3.0	30	35	45	
			4.5	10	13	15	
			6.0	9	11	13	

AC CHARACTERISTICS ($t_f = t_r$ = 6 ns, C_L = 50 pF)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				−55°C to 25°C	≤ 85°C	≤ 125°C	
t_{SU}	Minimum Set−up Time CP to STR	Figure 8	2.0	100	125	150	ns
			3.0	60	75	90	
			4.5	20	25	30	
			6.0	17	21	26	
t_h	Minimum Hold Time D to CP	Figure 10	2.0	3	3	3	ns
			3.0	3	3	3	
			4.5	3	3	3	
			6.0	3	3	3	
t_h	Minimum Hold Time CP to STR	Figure 8	2.0	0	0	0	ns
			3.0	0	0	0	
			4.5	0	0	0	
			6.0	0	0	0	
f_{MAX}	Minimum Clock Pulse Frequency	Figure 7	2.0	6	5	4	MHz
			3.0	18	14	12	
			4.5	30	24	20	
			6.0	35	28	24	
C_{in}	Maximum Input Capacitance		−	10	10	10	pF
C_{out}	Maximum Output Capacitance		−	15	15	15	pF
C_{PD}	Power Dissipation Capacitance (Note 2)		−	140	140	140	pF

2. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC}(\text{operating}) \approx C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where N_{SW} = total number of outputs switching and f_{IN} = switching frequency.

AC WAVEFORMS

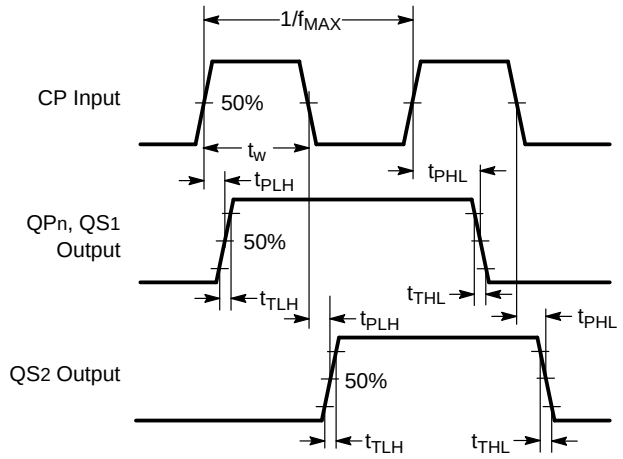


Figure 7. Waveforms showing the clock (CP) to output (QPn, QS1, QS2) propagation delays, the clock pulse width and the maximum clock frequency.

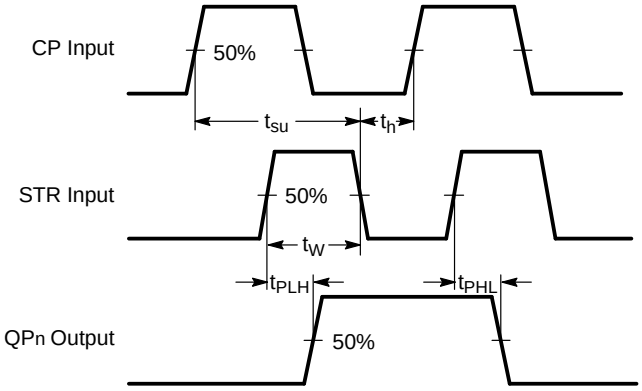


Figure 8. Waveforms showing the strobe (STR) to output (QPn) propagation delays, the strobe pulse width, the clock set−up and hold times for the strobe input.

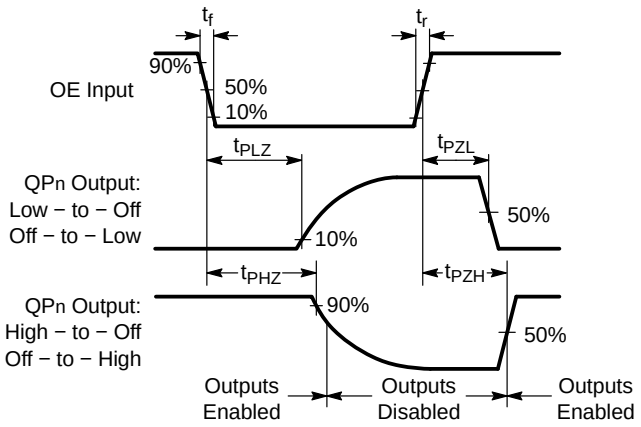
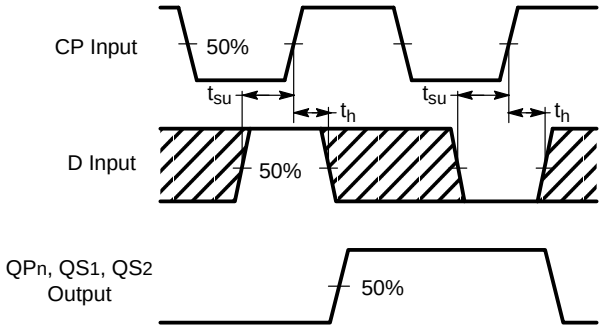


Figure 9. Waveforms showing the 3−state enable and disable times for input OE.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 10. Waveforms showing the data set−up and hold times for the data input.

TEST CIRCUITS

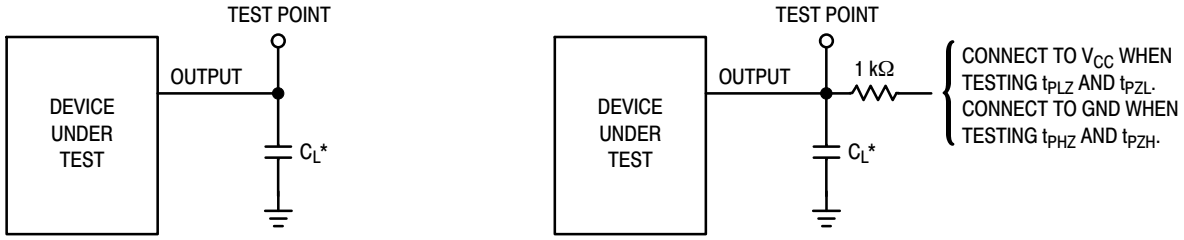


Figure 11. AC Characteristics Load Circuits

ORDERING INFORMATION

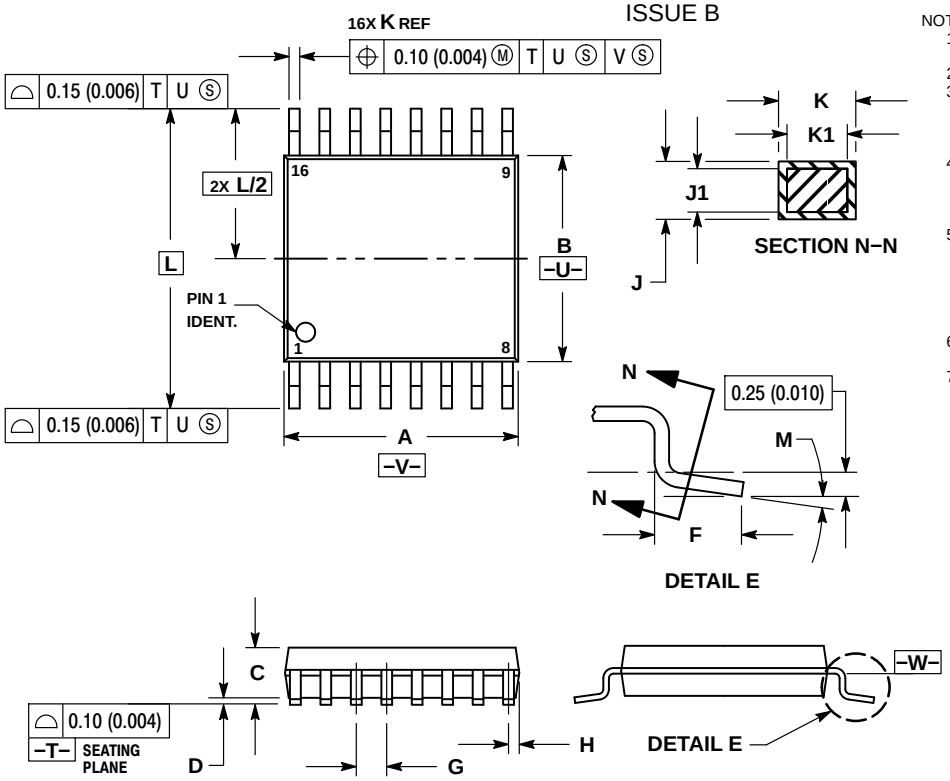
Device	Package	Shipping†
MC74HC4094ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC4094ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
MC74HC4094ADTG	TSSOP−16 (Pb−Free)	96 Units / Rail
MC74HC4094ADTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
NLVHC4094BDTR2G*	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

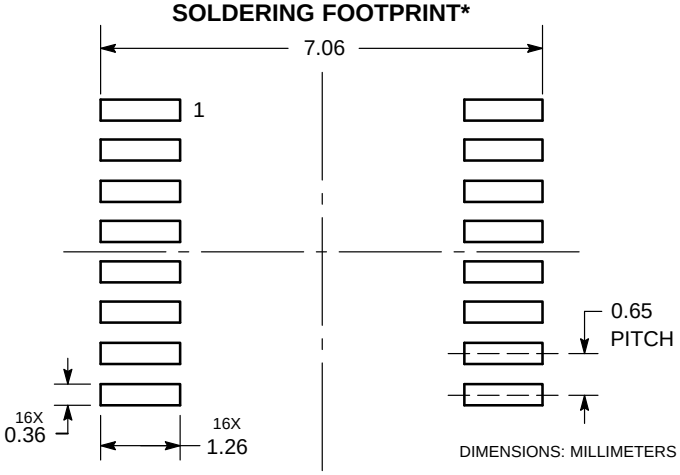
TSSOP−16
DT SUFFIX
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

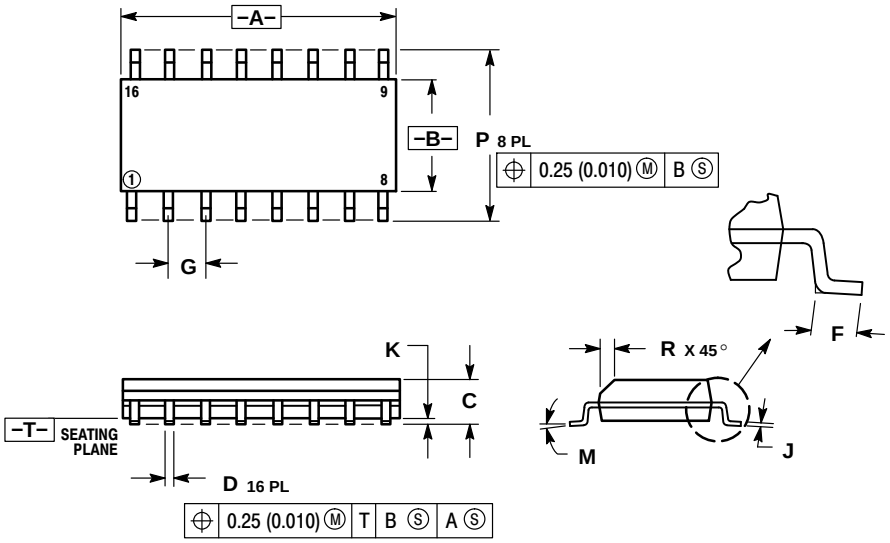
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

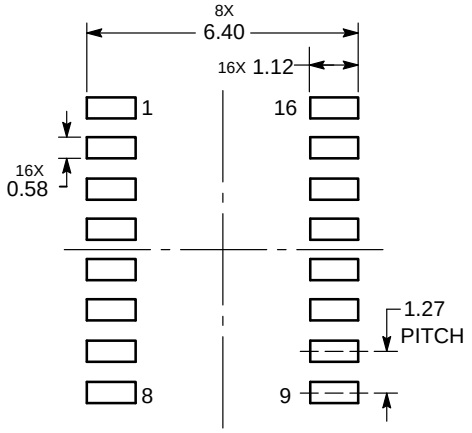
SOIC−16
CASE 751B−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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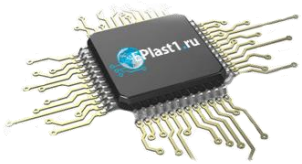
- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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