Single Channel, 128-/256-Position, I²C/SPI, Nonvolatile Digital Potentiometer

Data Sheet

AD5121/AD5141

FEATURES

10 kΩ and 100 kΩ resistance options
Resistor tolerance: 8% maximum
Wiper current: ±6 mA
Low temperature coefficient: 35 ppm/°C
Wide bandwidth: 3 MHz
Fast start-up time < 75 µs
Linear gain setting mode
Single- and dual-supply operation
Independent logic supply: 1.8 V to 5.5 V
Wide operating temperature: −40°C to +125°C
3 mm × 3 mm LFCSP package
4 kV ESD protection

APPLICATIONS

Portable electronics level adjustment
LCD panel brightness and contrast controls
Programmable filters, delays, and time constants
Programmable power supplies

GENERAL DESCRIPTION

The AD5121/AD5141 potentiometers provide a nonvolatile solution for 128-/256-position adjustment applications, offering guaranteed low resistor tolerance errors of ±8% and up to ±6 mA current density in the A, B, and W pins.

The low resistor tolerance and low nominal temperature coefficient simplify open-loop applications as well as applications requiring tolerance matching.

The linear gain setting mode allows independent programming of the resistance between the digital potentiometer terminals, through R_{AW} and R_{WB} string resistors, allowing very accurate resistor matching.

The high bandwidth and low total harmonic distortion (THD) ensure optimal performance for ac signals, making it suitable for filter design.

The low wiper resistance of only 40 Ω at the ends of the resistor array allows for pin-to-pin connection.

The wiper values can be set through an SPI-/I²C-compatible digital interface that is also used to read back the wiper register and EEPROM contents.

The AD5121/AD5141 is available in a compact, 16-lead, 3 mm × 3 mm LFCSP. The parts are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

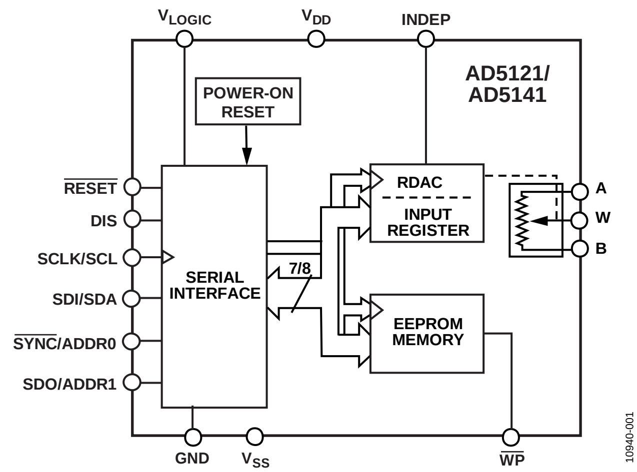

Figure 1.

Table 1. Family Models

Model	Channel	Position	Interface	Package
AD5123[1]	Quad	128	I²C	LFCSP
AD5124	Quad	128	SPI/I²C	LFCSP
AD5124	Quad	128	SPI	TSSOP
AD5143[1]	Quad	256	I²C	LFCSP
AD5144	Quad	256	SPI/I²C	LFCSP
AD5144	Quad	256	SPI	TSSOP
AD5144A	Quad	256	I²C	TSSOP
AD5122	Dual	128	SPI	LFCSP/TSSOP
AD5122A	Dual	128	I²C	LFCSP/TSSOP
AD5142	Dual	256	SPI	LFCSP/TSSOP
AD5142A	Dual	256	I²C	LFCSP/TSSOP
AD5121	Single	128	SPI/I²C	LFCSP
AD5141	Single	256	SPI/I²C	LFCSP

[1] Two potentiometers and two rheostats.

Rev. A Document Feedback
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12/12—Rev. 0 to Rev. A

Changes to Table 10 ... 22

10/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5121

V_{DD} = 2.3 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.25 V to 2.75 V, V_{SS} = −2.25 V to −2.75 V; V_{LOGIC} = 1.8 V to 5.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		7			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ				
		V_{DD} ≥ 2.7 V	−1	±0.1	+1	LSB
		V_{DD} < 2.7 V	−2.5	±1	+2.5	LSB
		R_{AB} = 100 kΩ				
		V_{DD} ≥ 2.7 V	−0.5	±0.1	+0.5	LSB
		V_{DD} < 2.7 V	−1	±0.25	+1	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.5	±0.1	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8	±1	+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance[3]	R_W	Code = zero scale				
		R_{AB} = 10 kΩ		55	125	Ω
		R_{AB} = 100 kΩ		130	400	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}					
		R_{AB} = 10 kΩ		40	80	Ω
		R_{AB} = 100 kΩ		60	230	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity[4]	INL					
		R_{AB} = 10 kΩ	−0.5	±0.1	+0.5	LSB
		R_{AB} = 100 kΩ	−0.25	±0.1	+0.25	LSB
Differential Nonlinearity[4]	DNL		−0.25	±0.1	+0.25	LSB
Full-Scale Error	V_{WFSE}					
		R_{AB} = 10 kΩ	−1.5	−0.1		LSB
		R_{AB} = 100 kΩ	−0.5	±0.1	+0.5	LSB
Zero-Scale Error	V_{WZSE}					
		R_{AB} = 10 kΩ		1	1.5	LSB
		R_{AB} = 100 kΩ		0.25	0.5	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W					
		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 100 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		25		pF
		R_{AB} = 100 kΩ		12		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		12		pF
		R_{AB} = 100 kΩ		5		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}				0.2 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_{IN}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUTS						
Output High Voltage[3]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.4	V
		I_{SINK} = 6 mA, V_{LOGIC} > 2.3 V			0.6	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Power Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND	1.8		V_{DD}	V
		Dual supply, V_{SS} < GND	2.25		V_{DD}	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND				
		V_{DD} = 5.5 V		0.7	5.5	µA
		V_{DD} = 2.3 V		400		nA
Negative Supply Current	I_{SS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND	−5.5	−0.7		µA
EEPROM Store Current[3, 6]	$I_{DD\_EEPROM\_STORE}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		2		mA
EEPROM Read Current[3, 7]	$I_{DD\_EEPROM\_READ}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		320		µA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		1	120	nA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		3.5		µW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = V_{DD} \pm 10\%$, code = full scale		−66	−60	dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[9]						
Bandwidth	BW	−3 dB				
		R_{AB} = 10 kΩ		3		MHz
		R_{AB} = 100 kΩ		0.43		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 100 kΩ		−90		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz				
		R_{AB} = 10 kΩ		7		nV/√Hz
		R_{AB} = 100 kΩ		20		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2		µs
		R_{AB} = 100 kΩ		12		µs
Endurance[10]		T_A = 25°C		1		Mcycles
			100			kcycles
Data Retention[11]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor integral nonlinearity (R-INL) error is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to (0.7 × V_{DD})/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[6] Different from operating current; supply current for EEPROM program lasts approximately 30 ms.
[7] Different from operating current; supply current for EEPROM read lasts approximately 20 µs.
[8] P_{DISS} is calculated from (I_{DD} × V_{DD}) + (I_{LOGIC} × V_{LOGIC}).
[9] All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.
[10] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C to +125°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.

ELECTRICAL CHARACTERISTICS—AD5141

V_{DD} = 2.3 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.25 V to 2.75 V, V_{SS} = −2.25 V to −2.75 V; V_{LOGIC} = 1.8 V to 5.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		8			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ				
		V_{DD} ≥ 2.7 V	−2	±0.2	+2	LSB
		V_{DD} < 2.7 V	−5	±1.5	+5	LSB
		R_{AB} = 100 kΩ				
		V_{DD} ≥ 2.7 V	−1	±0.1	+1	LSB
		V_{DD} < 2.7 V	−2	±0.5	+2	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.5	±0.2	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8	±1	+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance[3]	R_W	Code = zero scale				
		R_{AB} = 10 kΩ		55	125	Ω
		R_{AB} = 100 kΩ		130	400	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}					
		R_{AB} = 10 kΩ		40	80	Ω
		R_{AB} = 100 kΩ		60	230	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity[4]	INL					
		R_{AB} = 10 kΩ	−1	±0.2	+1	LSB
		R_{AB} = 100 kΩ	−0.5	±0.1	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.2	+0.5	LSB
Full-Scale Error	V_{WFSE}					
		R_{AB} = 10 kΩ	−2.5	−0.1		LSB
		R_{AB} = 100 kΩ	−1	±0.2	+1	LSB
Zero-Scale Error	V_{WZSE}					
		R_{AB} = 10 kΩ		1.2	3	LSB
		R_{AB} = 100 kΩ		0.5	1	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W					
		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 100 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		25		pF
		R_{AB} = 100 kΩ		12		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		12		pF
		R_{AB} = 100 kΩ		5		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}				0.2 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_{IN}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUTS						
Output High Voltage[3]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.4	V
		I_{SINK} = 6 mA, V_{LOGIC} > 2.3V			0.6	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Power Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND	1.8		V_{DD}	V
		Dual supply, V_{SS} < GND	2.25		V_{DD}	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND				
		V_{DD} = 5.5 V		0.7	5.5	µA
		V_{DD} = 2.3 V		400		nA
Negative Supply Current	I_{SS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND	−5.5	−0.7		µA
EEPROM Store Current[3, 6]	$I_{DD\_EEPROM\_STORE}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		2		mA
EEPROM Read Current[3, 7]	$I_{DD\_EEPROM\_READ}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		320		µA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		1	120	nA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		3.5		µW
Power Supply Rejection Ratio	PSR	$\Delta V_{DD}/\Delta V_{SS} = V_{DD} \pm 10\%$, code = full scale		−66	−60	dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[9]						
Bandwidth	BW	−3 dB				
		R_{AB} = 10 kΩ		3		MHz
		R_{AB} = 100 kΩ		0.43		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 100 kΩ		−90		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz				
		R_{AB} = 10 kΩ		7		nV/√Hz
		R_{AB} = 100 kΩ		20		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2		µs
		R_{AB} = 100 kΩ		12		µs
Endurance[10]		T_A = 25°C		1		Mcycles
			100			kcycles
Data Retention[11]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor integral nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to (0.7 × V_{DD})/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[6] Different from operating current; supply current for EEPROM program lasts approximately 30 ms.
[7] Different from operating current; supply current for EEPROM read lasts approximately 20 µs.
[8] P_{DISS} is calculated from (I_{DD} × V_{DD}) + (I_{LOGIC} × V_{LOGIC}).
[9] All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.
[10] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C to +125°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.

INTERFACE TIMING SPECIFICATIONS

V_{LOGIC} = 1.8 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. SPI Interface

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t_1	V_{LOGIC} > 1.8 V	20			ns	SCLK cycle time
	V_{LOGIC} = 1.8 V	30			ns	
t_2	V_{LOGIC} > 1.8 V	10			ns	SCLK high time
	V_{LOGIC} = 1.8 V	15			ns	
t_3	V_{LOGIC} > 1.8 V	10			ns	SCLK low time
	V_{LOGIC} = 1.8 V	15			ns	
t_4		10			ns	$\overline{\text{SYNC}}$-to-SCLK falling edge setup time
t_5		5			ns	Data setup time
t_6		5			ns	Data hold time
t_7		10			ns	$\overline{\text{SYNC}}$ rising edge to next SCLK fall ignored
t_8[2]		20			ns	Minimum $\overline{\text{SYNC}}$ high time
t_9[3]			50		ns	SCLK rising edge to SDO valid
t_{10}				500	ns	$\overline{\text{SYNC}}$ rising edge to SDO pin disable

[1] All input signals are specified with $t_r = t_f$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Refer to $t_{EEPROM\_PROGRAM}$ and $t_{EEPROM\_READBACK}$ for memory commands operations (see Table 6).
[3] R_{PULL_UP} = 2.2 kΩ to V_{DD} with a capacitance load of 168 pF.

Table 5. I²C Interface

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
f_{SCL}[2]	Standard mode			100	kHz	Serial clock frequency
	Fast mode			400	kHz	
t_1	Standard mode	4.0			µs	SCL high time, t_{HIGH}
	Fast mode	0.6			µs	
t_2	Standard mode	4.7			µs	SCL low time, t_{LOW}
	Fast mode	1.3			µs	
t_3	Standard mode	250			ns	Data setup time, $t_{SU; DAT}$
	Fast mode	100			ns	
t_4	Standard mode	0		3.45	µs	Data hold time, $t_{HD; DAT}$
	Fast mode	0		0.9	µs	
t_5	Standard mode	4.7			µs	Setup time for a repeated start condition, $t_{SU; STA}$
	Fast mode	0.6			µs	
t_6	Standard mode	4			µs	Hold time (repeated) for a start condition, $t_{HD; STA}$
	Fast mode	0.6			µs	
t_7	Standard mode	4.7			µs	Bus free time between a stop and a start condition, t_{BUF}
	Fast mode	1.3			µs	
t_8	Standard mode	4			µs	Setup time for a stop condition, $t_{SU; STO}$
	Fast mode	0.6			µs	
t_9	Standard mode			1000	ns	Rise time of SDA signal, t_{RDA}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{10}	Standard mode			300	ns	Fall time of SDA signal, t_{FDA}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{11}	Standard mode			1000	ns	Rise time of SCL signal, t_{RCL}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{11A}	Standard mode			1000	ns	Rise time of SCL signal after a repeated start condition and after an acknowledge bit, t_{RCL1} (not shown in Figure 3)
	Fast mode	20 + 0.1 C_L		300	ns	

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t_{12}	Standard mode			300	ns	Fall time of SCL signal, t_{FCL}
	Fast mode	20 + 0.1 C_L		300	ns	
t_{SP}[3]	Fast mode	0		50	ns	Pulse width of suppressed spike (not shown in Figure 3)

[1] Maximum bus capacitance is limited to 400 pF.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate; however, it has a negative effect on the EMC behavior of the part.
[3] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode.

Table 6. Control Pins

Parameter	Min	Typ	Max	Unit	Description
t_1	1			µs	End command to $\overline{\text{LRDAC}}$ falling edge
t_2	50			ns	Minimum $\overline{\text{LRDAC}}$ low time
t_3	0.1		10	µs	$\overline{\text{RESET}}$ low time
$t_{EEPROM\_PROGRAM}$[1]		15	50	ms	Memory program time (not shown in Figure 6)
$t_{EEPROM\_READBACK}$		7	30	µs	Memory readback time (not shown in Figure 6)
t_{POWER_UP}[2]			75	µs	Power-on EEPROM restore time (not shown in Figure 6)
t_{RESET}		30		µs	Reset EEPROM restore time (not shown in Figure 6)

[1] EEPROM program time depends on the temperature and EEPROM write cycles. Higher timing is expected at lower temperatures and higher write cycles.
[2] Maximum time after $V_{DD} - V_{SS}$ is equal to 2.3 V.

SHIFT REGISTER AND TIMING DIAGRAMS

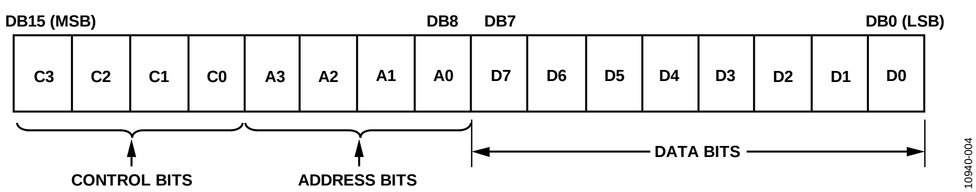

Figure 2. Input Shift Register Contents

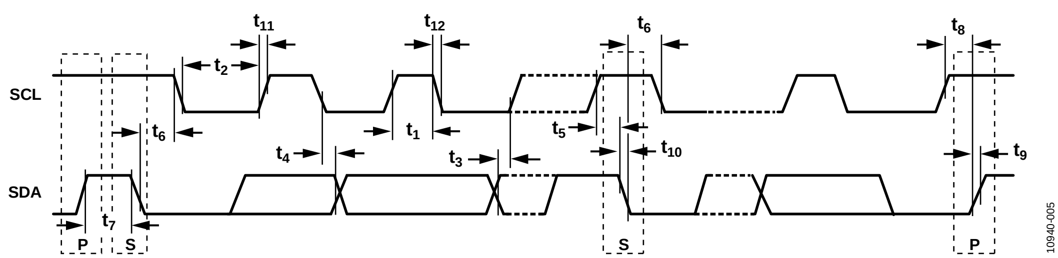

Figure 3. I²C Serial Interface Timing Diagram (Typical Write Sequence)

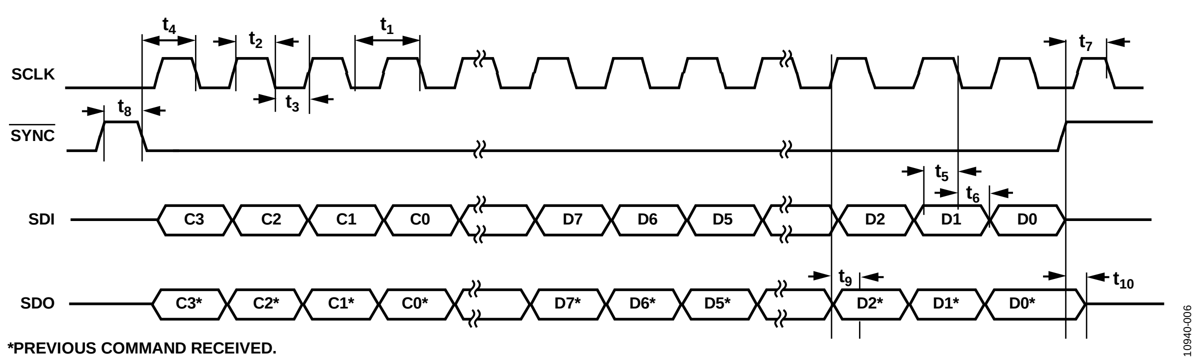

Figure 4. SPI Serial Interface Timing Diagram, CPOL = 0, CPHA = 1

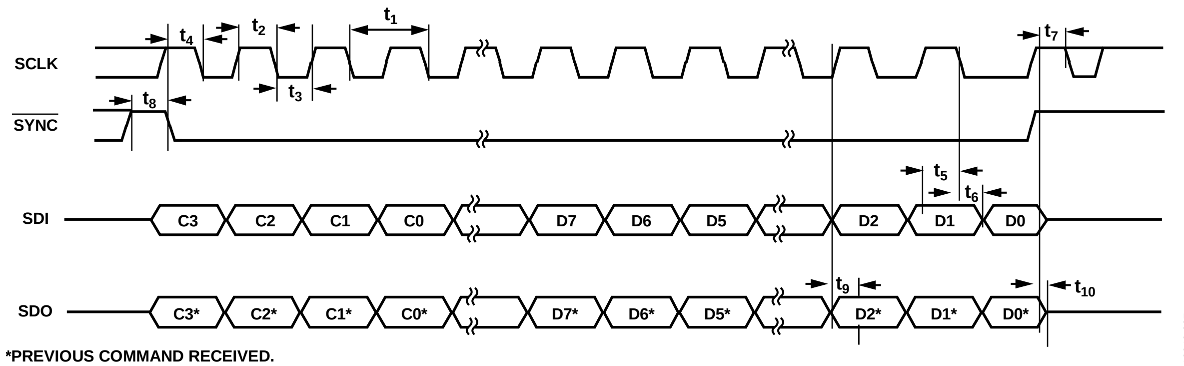

Figure 5. SPI Serial Interface Timing Diagram, CPOL = 1, CPHA = 0

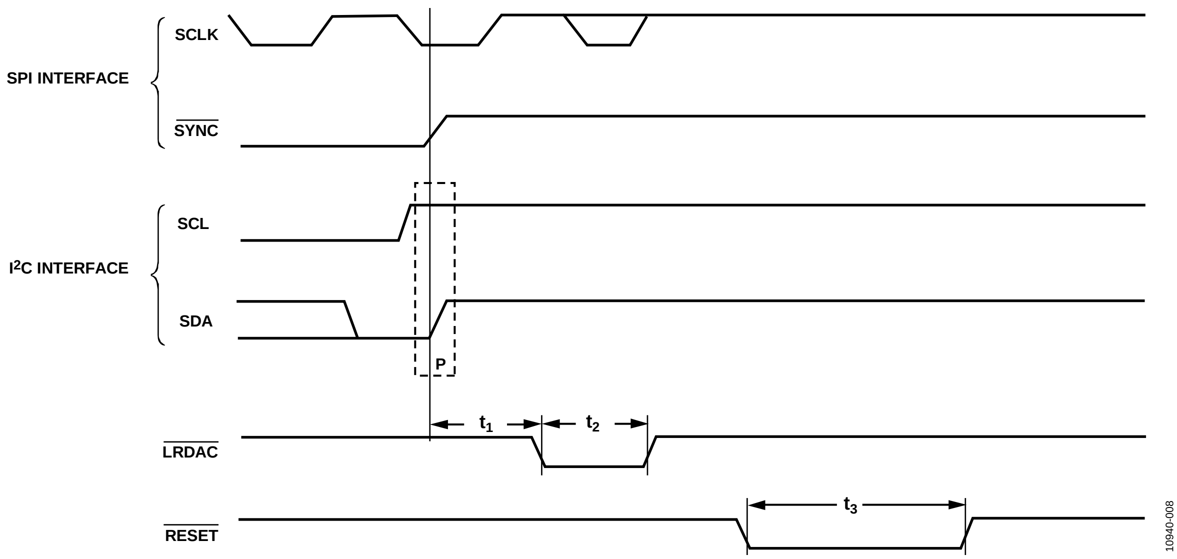

Figure 6. Control Pins Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{SS} to GND	+0.3 V to −7.0 V
V_{DD} to V_{SS}	7 V
V_{LOGIC} to GND	−0.3 V to V_{DD} + 0.3 V or +7.0 V (whichever is less)
V_A, V_W, V_B to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V or +7.0 V (whichever is less)
I_A, I_W, I_B	
Pulsed[1]	
Frequency > 10 kHz	
R_{AW} = 10 kΩ	±6 mA/d[2]
R_{AW} = 100 kΩ	±1.5 mA/d[2]
Frequency ≤ 10 kHz	
R_{AW} = 10 kΩ	±6 mA/√d[2]
R_{AW} = 100 kΩ	±1.5 mA/√d[2]
Digital Inputs	−0.3 V to V_{LOGIC} + 0.3 V or +7 V (whichever is less)
Operating Temperature Range, T_A[3]	−40°C to +125°C
Maximum Junction Temperature, T_J Maximum	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \max - T_A)/\theta_{JA}$

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] d = pulse duty factor.
[3] Includes programming of EEPROM memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is defined by the JEDEC JESD51 standard, and the value is dependent on the test board and test environment.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead LFCSP	89.5[1]	3	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

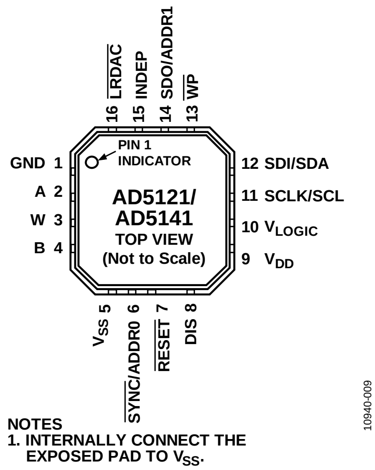

Figure 7. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Pin, Logic Ground Reference.
2	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$.
3	W	Wiper terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$.
4	B	Terminal B of RDAC. $V_{SS} \le V_B \le V_{DD}$.
5	V_{SS}	Negative Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
6	$\overline{\text{SYNC}}$/ADDR0	Programmable Address (ADDR0) for Multiple Package Decoding, DIS = 1.
		Synchronization Data Input, Active Low. When $\overline{\text{SYNC}}$ returns high, data is loaded into the RDAC register, DIS = 0.
7	$\overline{\text{RESET}}$	Hardware Reset Pin. Refresh the RDAC registers from EEPROM. $\overline{\text{RESET}}$ is activated at logic low. If this pin is not used, tie $\overline{\text{RESET}}$ to V_{LOGIC}.
8	DIS	Digital Interface Select (SPI/I²C Select). SPI when DIS = 0 (GND), I²C when DIS = 1 (V_{LOGIC}). This pin cannot be left floating.
9	V_{DD}	Positive Power Supply. Decouple this pin with 0.1µF ceramic capacitors and 10 µF capacitors.
10	V_{LOGIC}	Logic Power Supply; 1.8 V to VDD. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
11	SCLK/SCL	SPI Serial Clock Line (SCLK). Data is clocked in at logic low transition.
		I²C Serial Clock Line (SCL). Data is clocked in at logic low transition.
12	SDI/SDA	Serial Data Input/Output (SDA), When DIS = 1.
		Serial Data Input (SDI), When DIS = 0.
13	$\overline{\text{WP}}$	Optional Write Protect. This pin prevents any changes to the present RDAC and EEPROM contents, except when reloading the content of the EEPROM into the RDAC register. $\overline{\text{WP}}$ is activated at logic low. If this pin is not used, tie $\overline{\text{WP}}$ to V_{LOGIC}
14	SDO/ADDR1	Programmable Address (ADDR1) for Multiple Package Decoding, When DIS = 1.
		Serial Data Output (SDO). This is an open-drain output pin, and it needs an external pull-up resistor when DIS = 0.
15	INDEP	Linear Gain Setting Mode at Power-Up. Each string resistor is loaded from its associate memory location. If INDEP is enabled, it cannot be disabled by the software.
16	$\overline{\text{LRDAC}}$	Load RDAC. Transfers the contents of the input register to the RDAC register. This allows asynchronous RDAC update. $\overline{\text{LRDAC}}$ is activated low. If this pin is not used, tie $\overline{\text{LRDAC}}$ to V_{LOGIC}.
	EPAD	Internally Connect the Exposed Pad to V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

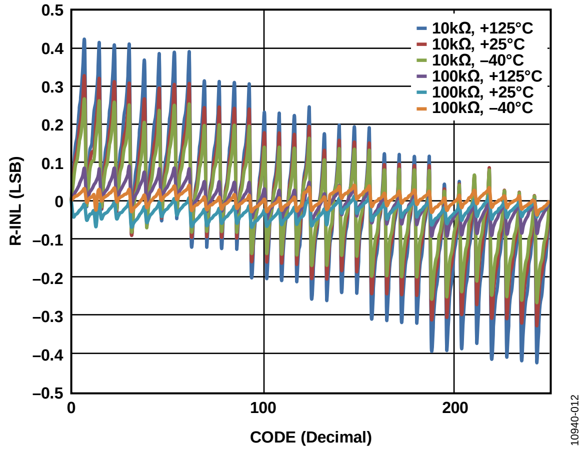

Figure 8. R-INL vs. Code (AD5141)

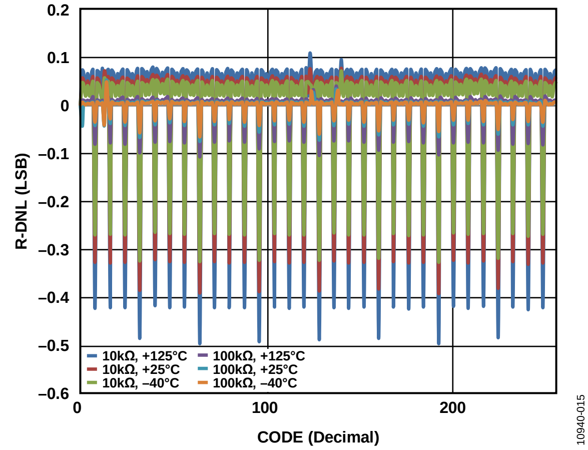

Figure 11. R-DNL vs. Code (AD5141)

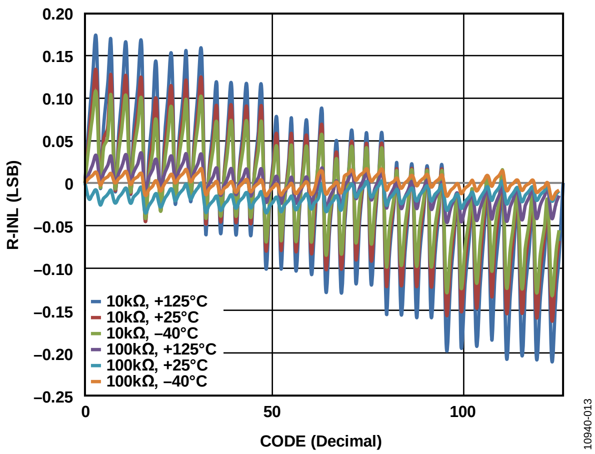

Figure 9. R-INL vs. Code (AD5121)

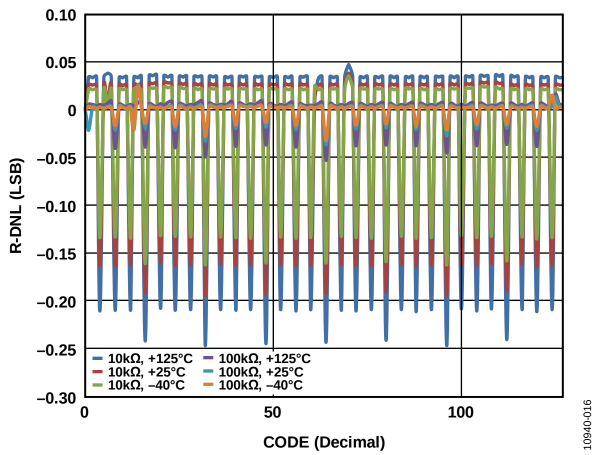

Figure 12. R-DNL vs. Code (AD5121)

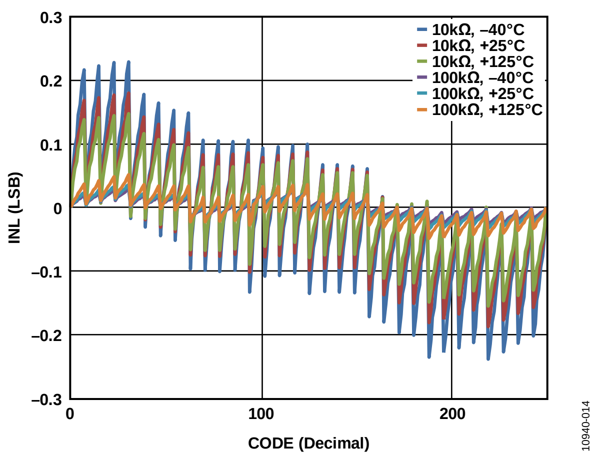

Figure 10. INL vs. Code (AD5141)

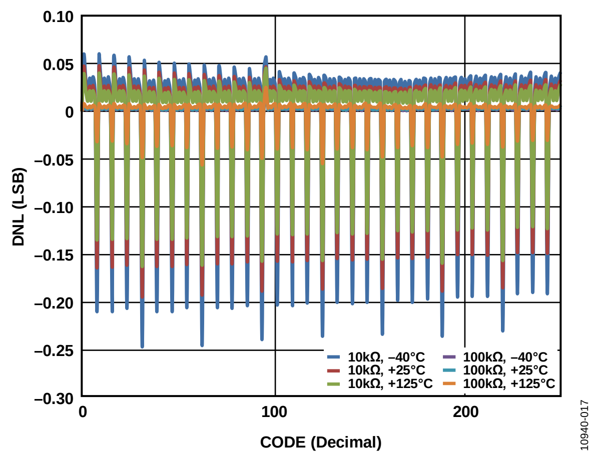

Figure 13. DNL vs. Code (AD5141)

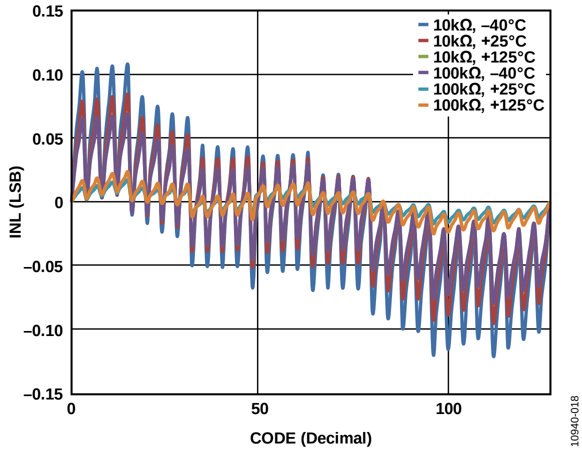

Figure 14. INL vs. Code (AD5121)

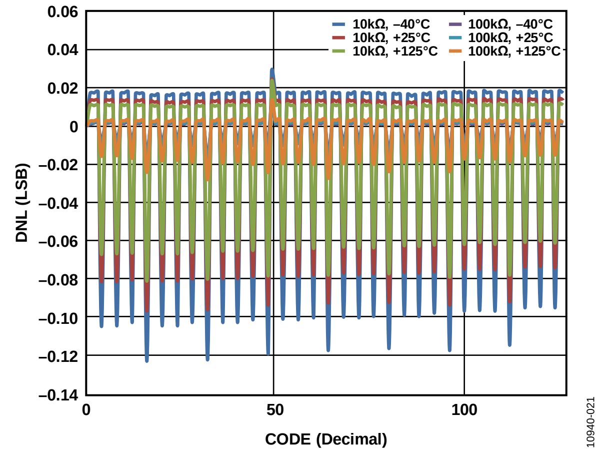

Figure 17. DNL vs. Code (AD5121)

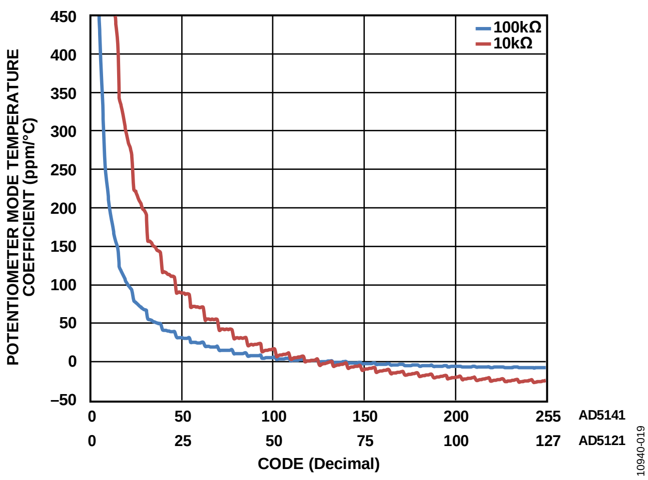

Figure 15. Potentiometer Mode Temperature Coefficient (($\Delta V_W/V_W$)/$\Delta T \times 10^6$) vs. Code

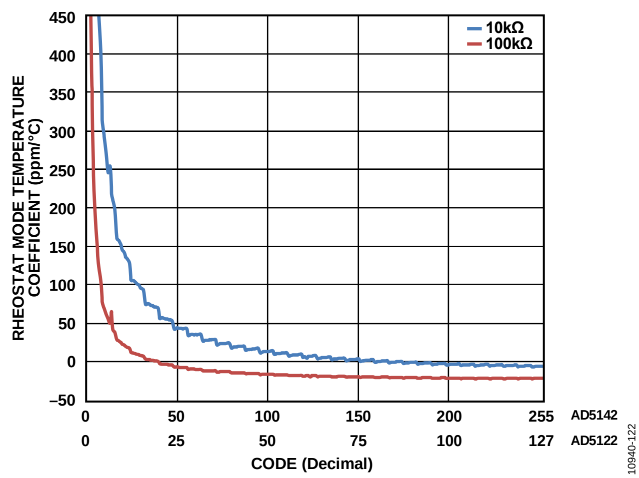

Figure 18. Rheostat Mode Temperature Coefficient (($\Delta R_{WB}/R_{WB}$)/$\Delta T \times 10^6$) vs. Code

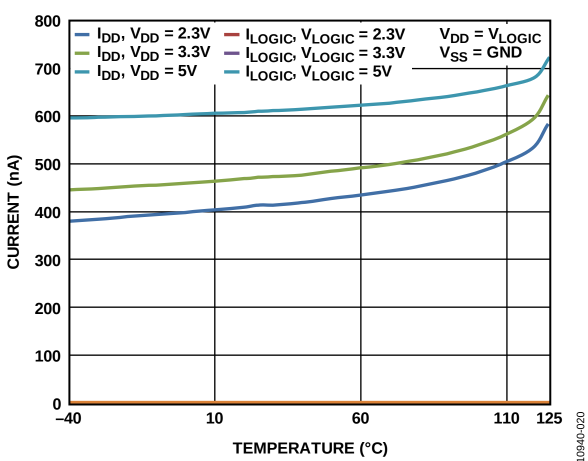

Figure 16. Supply Current vs. Temperature

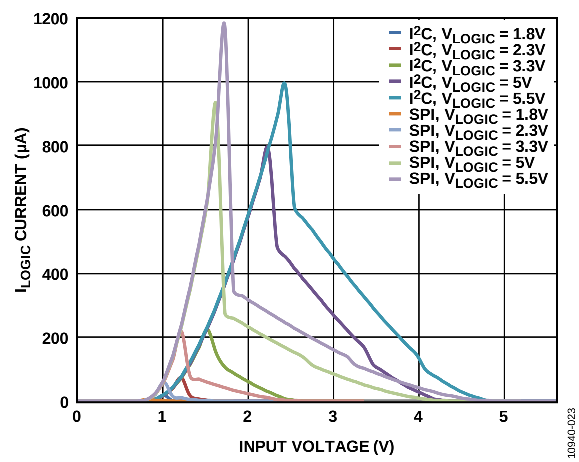

Figure 19. I_{LOGIC} Current vs. Digital Input Voltage

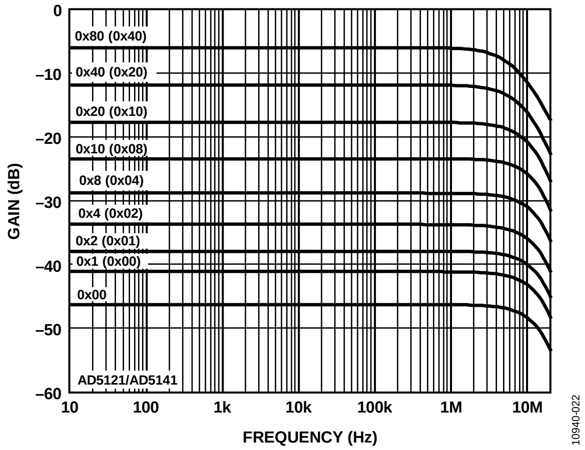

Figure 20. 10 kΩ Gain vs. Frequency vs. Code

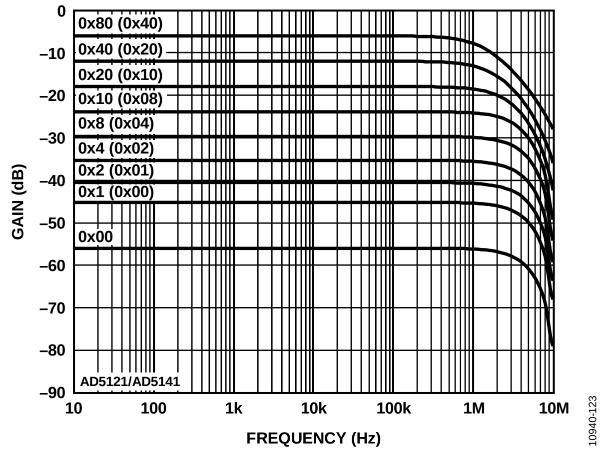

Figure 23. 100 kΩ Gain vs. Frequency vs. Code

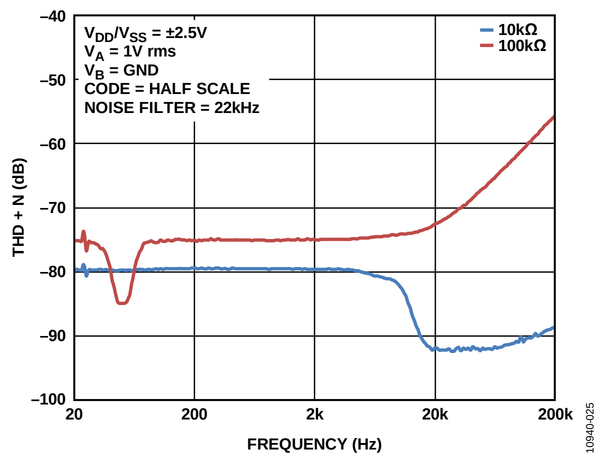

Figure 21. Total Harmonic Distortion Plus Noise (THD + N) vs. Frequency

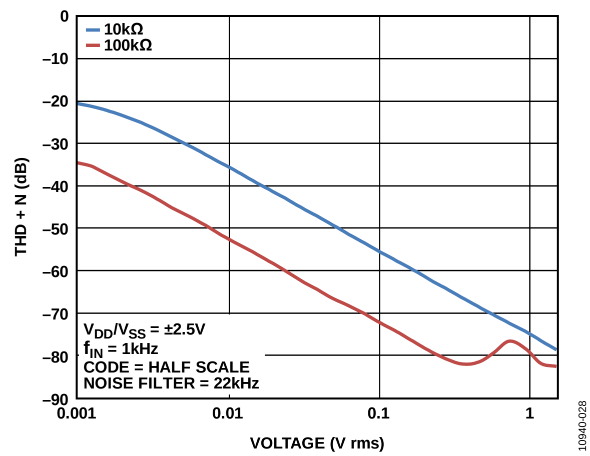

Figure 24. Total Harmonic Distortion Plus Noise (THD + N) vs. Amplitude

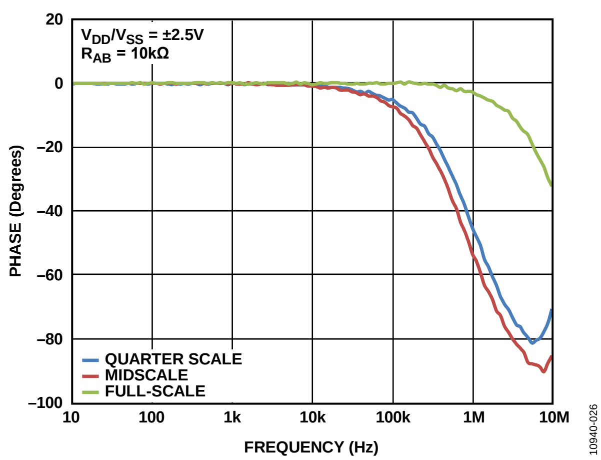

Figure 22. Normalized Phase Flatness vs. Frequency, R_{AB} = 10 kΩ

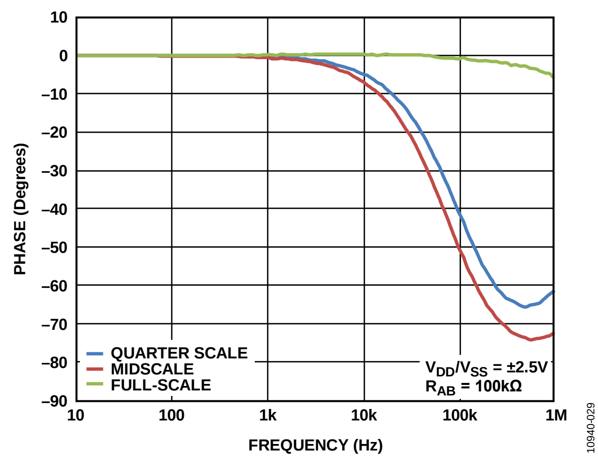

Figure 25. Normalized Phase Flatness vs. Frequency, R_{AB} = 100 kΩ

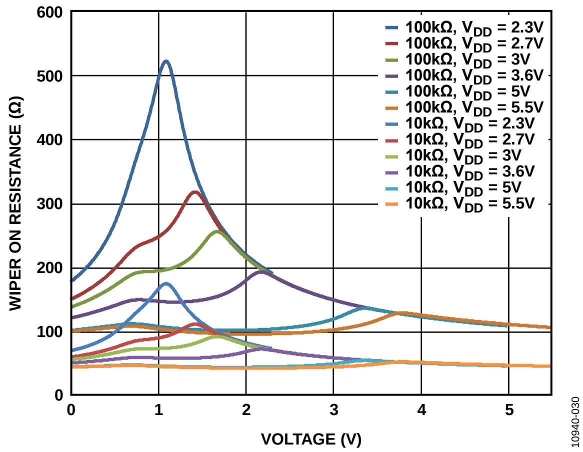

Figure 26. Incremental Wiper On Resistance vs. V_{DD}

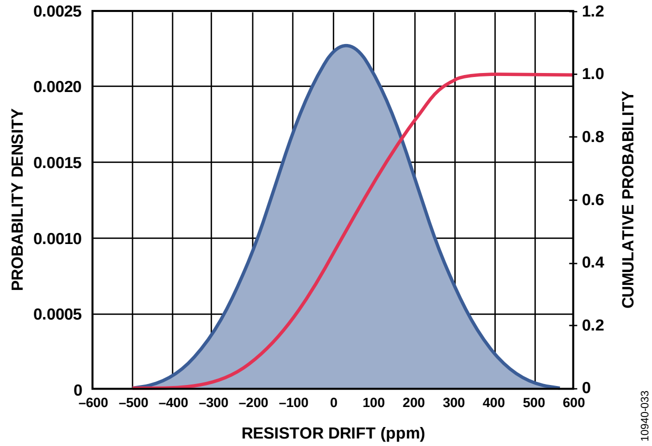

Figure 29. Resistor Lifetime Drift

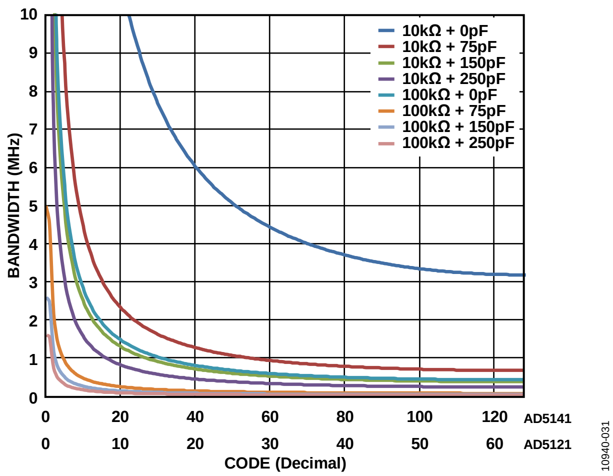

Figure 27. Maximum Bandwidth vs. Code vs. Net Capacitance

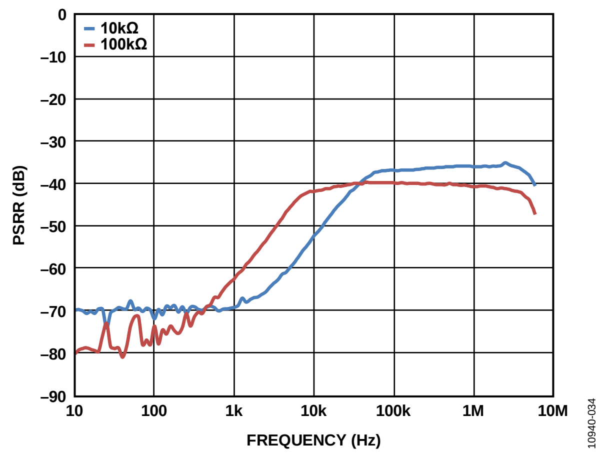

Figure 30. Power Supply Rejection Ratio (PSRR) vs. Frequency

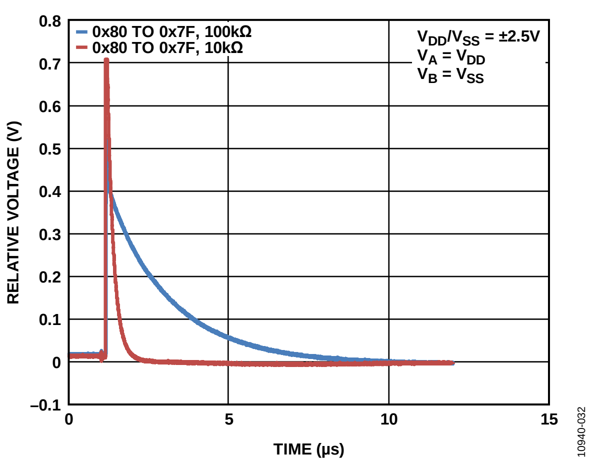

Figure 28. Maximum Transition Glitch

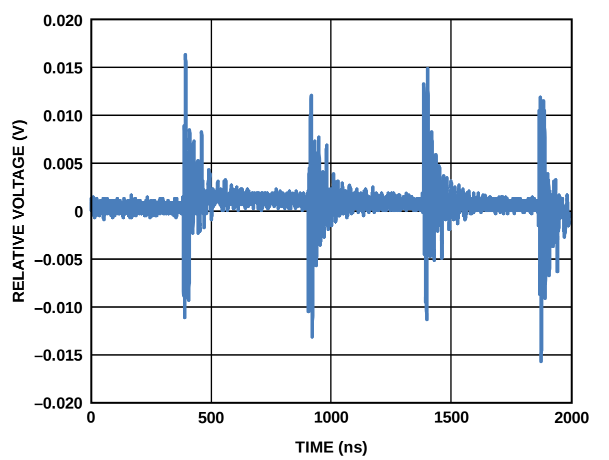

Figure 31. Digital Feedthrough

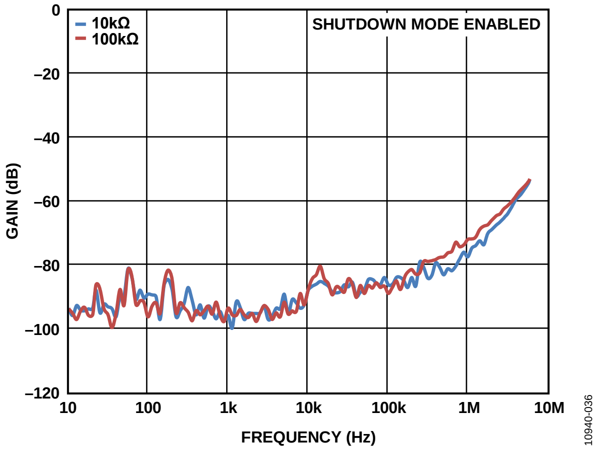

Figure 32. Shutdown Isolation vs. Frequency

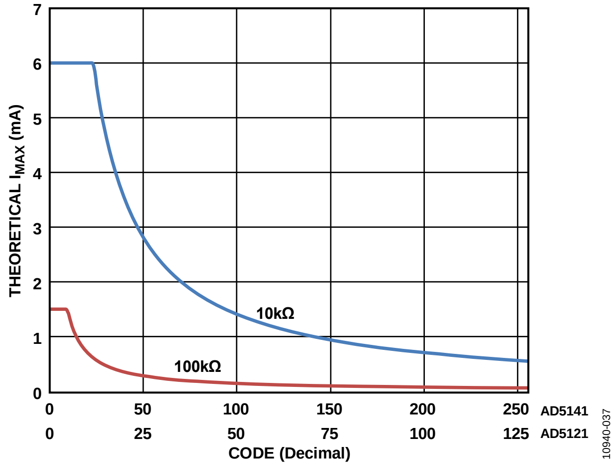

Figure 33. Theoretical Maximum Current vs. Code

TEST CIRCUITS

Figure 34 to Figure 38 define the test conditions used in the Specifications section.

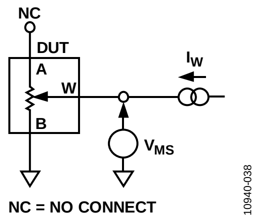

Figure 34. Resistor Integral Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

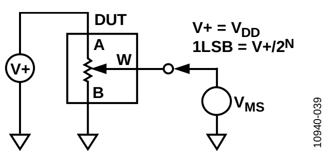

Figure 35. Potentiometer Divider Nonlinearity Error (INL, DNL)

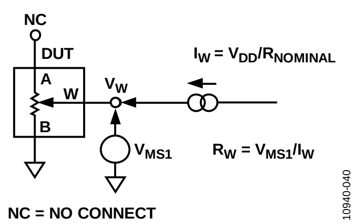

Figure 36. Wiper Resistance

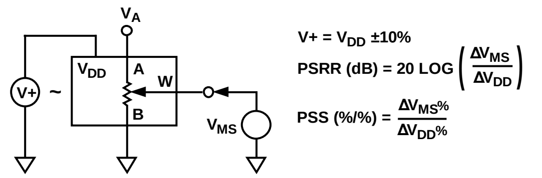

Figure 37. Power Supply Sensitivity and Power Supply Rejection Ratio (PSS and PSRR)

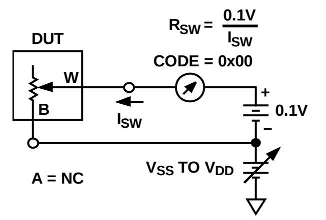

Figure 38. Incremental on Resistance

THEORY OF OPERATION

The AD5121/AD5141 digital programmable potentiometers are designed to operate as true variable resistors for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register that allows unlimited changes of resistance settings. A secondary register (the input register) can be used to preload the RDAC register data.

The RDAC register can be programmed with any position setting using the I²C or SPI interface (depending on the model). When a desirable wiper position is found, this value can be stored in the EEPROM memory. Thereafter, the wiper position is always restored to that position for subsequent power-ups. The storing of EEPROM data takes approximately 18 ms; during this time, the device is locked and does not acknowledge any new command, preventing any changes from taking place.

RDAC REGISTER AND EEPROM

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with 0x80 (AD5141, 256 taps), the wiper is connected to half scale of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

It is possible to both write to and read from the RDAC register using the digital interface (see Table 16).

The contents of the RDAC register can be stored to the EEPROM using Command 9 (see Table 16). Thereafter, the RDAC register always sets at that position for any future on-off-on power supply sequence. It is possible to read back data saved into the EEPROM with Command 3 (see Table 16).

Alternatively, the EEPROM can be written to independently using Command 1 (see Table 16).

INPUT SHIFT REGISTER

For the AD5121/AD5141, the input shift register is 16 bits wide, as shown in Figure 2. The 16-bit word consists of four control bits, followed by four address bits and by eight data bits

If the AD5121 RDAC or EEPROM registers are read from or written to the lowest data bit (Bit 0) is ignored.

Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command, as listed in Table 11 and Table 16.

SERIAL DATA DIGITAL INTERFACE SELECTION, DIS

The AD5121/AD5141 LFSCP provides the flexibility of a selectable interface. When the digital interface select (DIS) pin is tied low, the SPI mode is engaged. When the DIS pin is tied high, the I²C mode is engaged.

SPI SERIAL DATA INTERFACE

The AD5121/AD5141 contain a 4-wire, SPI-compatible digital interface (SDI, $\overline{\text{SYNC}}$, SDO, and SCLK). The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word is loaded from the SDI pin. Data is loaded in at the SCLK falling edge transition, as shown in Figure 4. When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded according to the instructions in Table 16.

The AD5121/AD5141 do not require a continuous SCLK when $\overline{\text{SYNC}}$ is high. To minimize power consumption in the digital input buffers when the part is enabled, operate all serial interface pins close to the V_{LOGIC} supply rails.

$\overline{\text{SYNC}}$ Interruption

In a standalone write sequence for the AD5121/AD5141, the $\overline{\text{SYNC}}$ line is kept low for 16 falling edges of SCLK, and the instruction is decoded when $\overline{\text{SYNC}}$ is pulled high. However, if the $\overline{\text{SYNC}}$ line is kept low for less than 16 falling edges of SCLK, the input shift register content is ignored, and the write sequence is considered invalid.

SDO Pin

The serial data output pin (SDO) serves two purposes: to read back the contents of the control, EEPROM, RDAC, and input registers using Command 3 (see Table 11 and Table 16), and to connect the AD5121/AD5141 to daisy-chain mode.

The SDO pin contains an internal open-drain output that needs an external pull-up resistor. The SDO pin is enabled when $\overline{\text{SYNC}}$ is pulled low, and the data is clocked out of SDO on the rising edge of SCLK.

Daisy-Chain Connection

Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 39, the SDO pin of one package must be tied to the SDI pin of the next package. The clock period may need to be increased because the propagation delay of the line between subsequent devices. When two AD5121/AD5141 devices are daisy chained, 32 bits of data are required. The first 16 bits assigned to U2, and the second 16 bits assigned to U1, as shown in Figure 40. Keep the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation. A typical connection is shown in Figure 39.

To prevent data from mislocking (for example, due to noise) the part includes an internal counter, if the clock falling edges count is not a multiple of 8, the part ignores the command. A valid clock count is 16, 24, or 32. The counter resets when $\overline{\text{SYNC}}$ returns high.

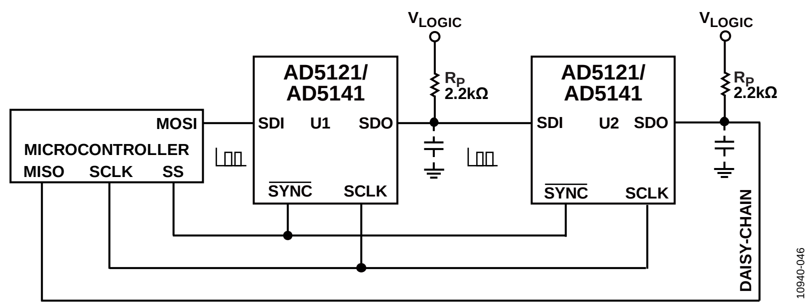

Figure 39. Daisy-Chain Configuration

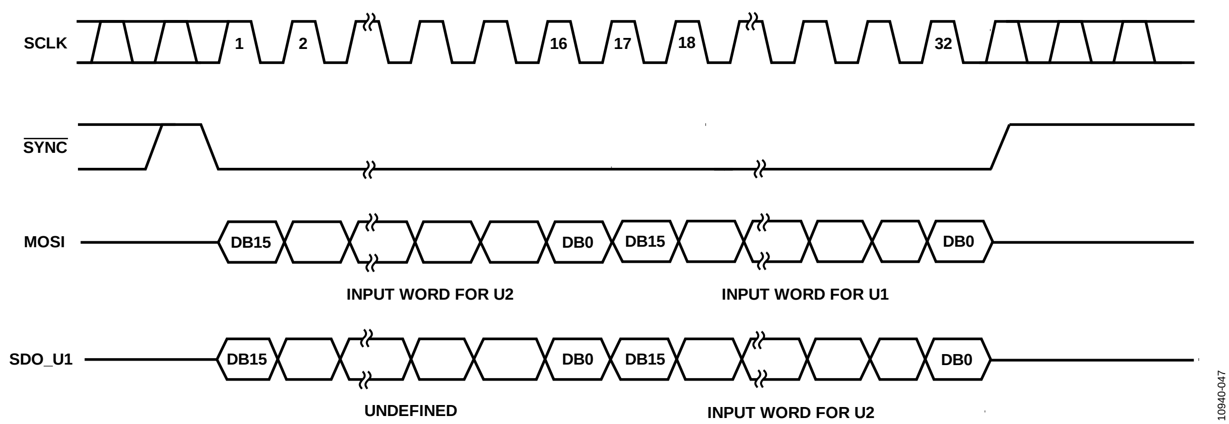

Figure 40. Daisy-Chain Diagram

I²C SERIAL DATA INTERFACE

The AD5141 has 2-wire, I²C-compatible serial interface. These devices can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 3 for a timing diagram of a typical write sequence.

The AD5141 supports standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The 2-wire serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address and an R/$\overline{W}$ bit. The slave device corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
   If the R/$\overline{W}$ bit is set high, the master reads from the slave device. However, if the R/$\overline{W}$ bit is set low, the master writes to the slave device.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read from or written to, a stop condition is established. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, and then high again during the tenth clock pulse to establish a stop condition.

I²C ADDRESS

The AD5141 has two different pin address options available, as shown in Table 10.

Table 10. 24-Lead LFCSP Device Address Selection

ADDR0 Pin	ADDR1 Pin	7-Bit I²C Device Address
V_{LOGIC}	V_{LOGIC}	0100000
No connect[1]	V_{LOGIC}	0100010
GND	V_{LOGIC}	0100011
V_{LOGIC}	No connect[1]	0101000
No connect[1]	No connect[1]	0101010
GND	No connect[1]	0101011
V_{LOGIC}	GND	0101100
No connect[1]	GND	0101110
GND	GND	0101111

[1] Not available in bipolar mode (V_{SS} < 0 V) or in low voltage mode (V_{LOGIC} = 1.8 V).

Table 11. Simple Command Operation Truth Table

<table>
<tr><th rowspan="2">Command Number</th><th colspan="4">Control Bits[DB15:DB12]</th><th colspan="4">Address Bits[DB11:DB8][1]</th><th colspan="8">Data Bits[DB7:DB0][1]</th><th rowspan="2">Operation</th></tr>
<tr><th>C3</th><th>C2</th><th>C1</th><th>C0</th><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>NOP: do nothing</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Write contents of serial register data to RDAC</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Write contents of serial register data to input register</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>X</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>D1</td><td>D0</td><td>Read back contents<table><tr><th>D1</th><th>D0</th><th>Data</th></tr><tr><td>0</td><td>1</td><td>EEPROM</td></tr><tr><td>1</td><td>1</td><td>RDAC</td></tr></table></td></tr>
<tr><td>9</td><td>0</td><td>1</td><td>1</td><td>1</td><td>X</td><td>X</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>Copy RDAC register to EEPROM</td></tr>
<tr><td>10</td><td>0</td><td>1</td><td>1</td><td>1</td><td>X</td><td>X</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>Copy EEPROM into RDAC</td></tr>
<tr><td>14</td><td>1</td><td>0</td><td>1</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>Software reset</td></tr>
<tr><td>15</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>D0</td><td>Software shutdown<table><tr><th>D0</th><th>Condition</th></tr><tr><td>0</td><td>Normal mode</td></tr><tr><td>1</td><td>Shutdown mode</td></tr></table></td></tr>
</table>

[1] X = don't care.

ADVANCED CONTROL MODES

The AD5121/AD5141 digital potentiometers include a set of user programming features to address the wide number of applications for these universal adjustment devices (see Table 16 and Table 18).

Key programming features include the following:

- Input register
- Linear gain setting mode
- Low wiper resistance feature
- Linear increment and decrement instructions
- ±6 dB increment and decrement instructions
- Burst mode (I^2C only)
- Reset
- Shutdown mode

Input Register

The AD5121/AD5141 include one input register per RDAC register. This register allows preloading of the value for the associated RDAC register.

This feature allows a synchronous and asynchronous update of one or all the RDAC registers at the same time.

These registers can be written to using Command 2 and read back from using Command 3 (see Table 16).

The transfer from the input register to the RDAC register is done asynchronously by the $\overline{\text{LRDAC}}$ pin or synchronously by Command 8 (see Table 16).

If new data is loaded in an RDAC register, this RDAC register automatically overwrites the associated input register.

Linear Gain Setting Mode

The patented architecture of the AD5121/AD5141 allows the independent control of each string resistor, R_{AW} and R_{WB}. To enable this feature, use Command 16 (see Table 16) to set Bit D2 of the control register (see Table 18).

This mode of operation can control the potentiometer as two independent rheostats connected at a single point, W terminal, as opposed to potentiometer mode where each resistor is complementary, $R_{AW} = R_{AB} − R_{WB}$.

This feature enables a second input and an RDAC register per channel, as shown in Table 16; however, the actual RDAC contents remain unchanged. The same operations are valid for potentiometer and linear gain setting modes.

If the INDEP pin is pulled high, the device powers up in linear gain setting mode and loads the values stored in the associated memory locations for each channel (see Table 17). The INDEP pin and D2 bit are connected internally to a logic OR gate, if any or both are 1, the parts cannot operate in potentiometer mode.

Low Wiper Resistance Feature

The AD5121/AD5141 include two commands to reduce the wiper resistance between the terminals when they achieve full scale or zero scale. These extra positions are called bottom scale, BS, and top scale, TS. The resistance between Terminal A and Terminal W at top scale is specified as R_{TS}. Similarly, the bottom scale resistance between Terminal B and Terminal W is specified as R_{BS}.

The contents of the RDAC registers are unchanged by entering in these positions. There are two ways to exit from top scale and bottom scale: by using Command 12 or Command 13 (see Table 16); or by loading new data in an RDAC register, which includes increment/decrement operations and a shutdown command.

Table 12 and Table 13 show the truth tables for the top scale position and the bottom scale position, respectively, when linear gain setting mode is enabled.

Table 12. Top Scale Truth Table

Linear Gain Setting Mode		Potentiometer Mode	
R_{AW}	R_{WB}	R_{AW}	R_{WB}
R_{AB}	R_{AB}	R_{TS}	R_{AB}

Table 13. Bottom Scale Truth Table

Linear Gain Setting Mode		Potentiometer Mode	
R_{AW}	R_{WB}	R_{AW}	R_{WB}
R_{TS}	R_{BS}	R_{AB}	R_{BS}

Linear Increment and Decrement Instructions

The increment and decrement commands (Command 4 and Command 5 in Table 16) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send an increment or decrement command to the device. The adjustment can be individual or in a ganged potentiometer arrangement, where all wiper positions are changed at the same time.

For an increment command, executing Command 4 automatically moves the wiper to the next resistance segment position. This command can be executed in a single channel or multiple channels.

±6 dB Increment and Decrement Instructions

Two programming instructions produce logarithmic taper increment or decrement of the wiper position control by an individual potentiometer or by a ganged potentiometer arrangement where all RDAC register positions are changed simultaneously. The +6 dB increment is activated by Command 6, and the −6 dB decrement is activated by Command 7 (see Table 16). For example, starting with the zero-scale position and executing Command 6 ten times moves the wiper in 6 dB steps to the full-scale position. When the wiper position is near the maximum setting, the last 6 dB increment instruction causes the wiper to go to the full-scale position (see Table 14).

Incrementing the wiper position by +6 dB essentially doubles the RDAC register value, whereas decrementing the wiper position by −6 dB halves the register content. Internally, the AD5121/AD5141 use shift registers to shift the bits left and right to achieve a ±6 dB increment or decrement. These functions are useful for various audio/video level adjustments, especially for white LED brightness settings in which human visual responses are more sensitive to large adjustments than to small adjustments.

Table 14. Detailed Left Shift and Right Shift Functions for the ±6 dB Step Increment and Decrement

Left Shift (+6 dB/Step)	Right Shift (−6 dB/Step)
0000 0000	1111 1111
0000 0001	0111 1111
0000 0010	0011 1111
0000 0100	0001 1111
0000 1000	0000 1111
0001 0000	0000 0111
0010 0000	0000 0011
0100 0000	0000 0001
1000 0000	0000 0000
1111 1111	0000 0000

Burst Mode (I^2C Only)

By enabling the burst mode, multiple data bytes can be sent to the part consecutively. After the command byte, the part interprets the consecutive bytes as data bytes for the first command.

A new command can be sent by generating a repeat start or by a stop and start condition.

The burst mode is activated by setting Bit D3 of the control register (see Table 18), and if a reset or power-down is performed, it automatically resets.

Reset

The AD5121/AD5141 can be reset through software by executing Command 14 (see Table 16) or through hardware on the low pulse of the $\overline{\text{RESET}}$ pin. The reset command loads the RDAC register with the contents of the EEPROM and takes approximately 30 µs. The EEPROM is preloaded to midscale at the factory, and initial power-up is, accordingly, at midscale. Tie $\overline{\text{RESET}}$ to V_{DD} if the $\overline{\text{RESET}}$ pin is not used.

Shutdown Mode

The AD5121/AD5141 can be placed in shutdown mode by executing the software shutdown command, Command 15 (see Table 16); and by setting the LSB (D0) to 1. This feature places the RDAC in a special state. The contents of the RDAC register are unchanged by entering shutdown mode. However, all commands listed in Table 16 are supported while in shutdown mode. Execute Command 15 (see Table 16) and set the LSB (D0) to 0 to exit shutdown mode.

Table 15. Truth Table for Shutdown Mode

	Linear Gain Setting Mode		Potentiometer Mode	
A2	AW	WB	AW	WB
0	N/A[1]	Open	Open	R_{BS}
1	Open	N/A[1]	N/A[1]	N/A[1]

[1] N/A = not applicable.

EEPROM OR RDAC REGISTER PROTECTION

The EEPROM and RDAC registers can be protected by disabling any update to these registers. This can be done by using software or by using hardware. If these registers are protected by software, set Bit D0 and/or Bit D1 (see Table 18), which protects the RDAC and EEPROM registers independently.

If the registers are protected by hardware, pull the $\overline{\text{WP}}$ pin low. If the $\overline{\text{WP}}$ pin is pulled low when the part is executing a command, the protection is not enabled until the command is completed.

When RDAC is protected, the only operation allowed is to copy the EEPROM into the RDAC register.

LOAD RDAC INPUT REGISTER ($\overline{\text{LRDAC}}$)

$\overline{\text{LRDAC}}$ software or hardware transfers data from the input register to the RDAC register (and therefore updates the wiper position). By default, the input register has the same value as the RDAC register; therefore, only the input register that has been updated using Command 2 is updated.

Software $\overline{\text{LRDAC}}$, Command 8, allows updating of a single RDAC register or all of the channels at once (see Table 16). This is a synchronous update.

The hardware $\overline{\text{LRDAC}}$ is completely asynchronous and copies the content of all the input registers into the associated RDAC registers. If a command is executed, to avoid data corruption, any transition in the $\overline{\text{LRDAC}}$ pin is ignored by the part.

INDEP PIN

If the INDEP pin is pulled high at power-up, the part operates in linear gain setting mode, loading each string resistor, R_{AW} and R_{WB}, with the value stored into the EEPROM (see Table 17). If the pin is pulled low, the part powers up in potentiometer mode.

The INDEP pin and the D2 bit are connected internally to a logic OR gate, if any or both are 1, the part cannot operate in potentiometer mode (see Table 18).

Table 16. Advance Commands Operation Truth Table

Command Number	Control Bits[DB15:DB12]				Address Bits[DB11:DB8][1]				Data Bits[DB7:DB0][1]								Operation
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: do nothing
1	0	0	0	1	0	A2	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC
2	0	0	1	0	0	A2	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to input register
3	0	0	1	1	X	A2	A1	A0	X	X	X	X	X	X	D1	D0	Read back contents D1 / D0 / Data 0 / 0 / Input register 0 / 1 / EEPROM 1 / 0 / Control register 1 / 1 / RDAC
4	0	1	0	0	A3	A2	0	A0	X	X	X	X	X	X	X	1	Linear RDAC increment
5	0	1	0	0	A3	A2	0	A0	X	X	X	X	X	X	X	0	Linear RDAC decrement
6	0	1	0	1	A3	A2	0	A0	X	X	X	X	X	X	X	1	+6 dB RDAC increment
7	0	1	0	1	A3	A2	0	A0	X	X	X	X	X	X	X	0	−6 dB RDAC decrement
8	0	1	1	0	A3	A2	0	A0	X	X	X	X	X	X	X	X	Copy input register to RDAC (software LRDAC)
9	0	1	1	1	0	A2	0	A0	X	X	X	X	X	X	X	1	Copy RDAC register to EEPROM
10	0	1	1	1	0	A2	0	A0	X	X	X	X	X	X	X	0	Copy EEPROM into RDAC
11	1	0	0	0	0	A2	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to EEPROM
12	1	0	0	1	A3	A2	0	A0	1	X	X	X	X	X	X	D0	Top scale D0 = 0; normal mode D0 = 1; shutdown mode
13	1	0	0	1	A3	A2	0	A0	0	X	X	X	X	X	X	D0	Bottom scale D0 = 1; enter D0 = 0; exit
14	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Software reset
15	1	1	0	0	A3	A2	0	A0	X	X	X	X	X	X	X	D0	Software shutdown D0 = 0; normal mode D0 = 1; device placed in shutdown mode
16	1	1	0	1	X	X	X	X	X	X	X	X	D3	D2	D1	D0	Copy serial register data to control register

[1] X = don't care.

Table 17. Address Bits

A3	A2	A1	A0	Potentiometer Mode		Linear Gain Setting Mode		Stored RDAC Memory
				Input Register	RDAC Register	Input Register	RDAC Register	
1	X[1]	X[1]	X[1]	All channels	All channels	All channels	All channels	Not applicable
0	0	0	0	RDAC	RDAC	R_{WB}	R_{WB}	RDAC/R_{WB}
0	1	0	0	Not applicable	Not applicable	R_{AW}	R_{AW}	Not applicable
0	0	0	1	Not applicable	Not applicable	Not applicable	Not applicable	R_{AW}
0	0	1	0	Not applicable	Not applicable	Not applicable	Not applicable	MSB tolerance
0	0	1	1	Not applicable	Not applicable	Not applicable	Not applicable	LSB tolerance

[1] X = don't care.

Table 18. Control Register Bit Descriptions

Bit Name	Description
D0	RDAC register write protect 0 = wiper position frozen to value in EEPROM memory 1 = allows update of wiper position through digital interface (default)
D1	EEPROM program enable 0 = EEPROM program disabled 1 = enables device for EEPROM program (default)
D2	Linear setting mode/potentiometer mode 0 = potentiometer mode (default) 1 = linear gain setting mode
D3	Burst mode (I^2C only) 0 = disabled (default) 1 = enabled (no disable after stop or repeat start condition)

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5121/AD5141 employ a three-stage segmentation approach, as shown in Figure 41. The AD5121/AD5141 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from V_{DD} and V_{SS}.

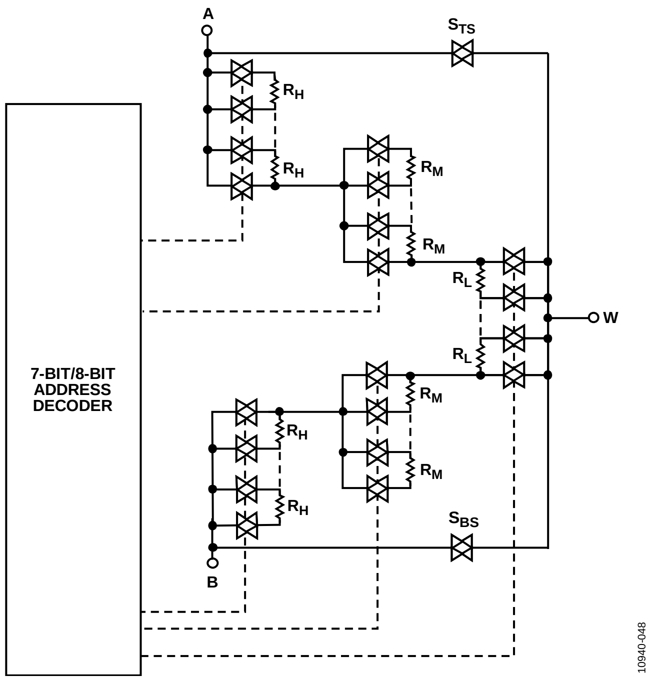

Figure 41. AD5121/AD5141 Simplified RDAC Circuit

Top Scale/Bottom Scale Architecture

In addition, the AD5121/AD5141 include new positions to reduce the resistance between terminals. These positions are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 130 Ω to 60 Ω (R_{AB} = 100 kΩ). At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB, and the total resistance is reduced to 60 Ω (R_{AB} = 100 kΩ).

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—±8% Resistor Tolerance

The AD5121/AD5141 operate in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating, or it can be tied to Terminal W, as shown in Figure 42.

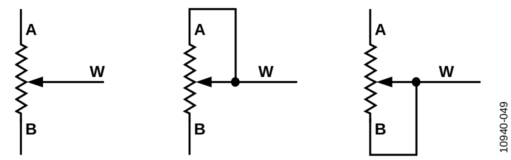

Figure 42. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is 10 kΩ or 100 kΩ, and has 128/256 tap points accessed by the wiper terminal. The 7-bit/8-bit data in the RDAC latch is decoded to select one of the 128/256 possible wiper settings. The general equations for determining the digitally programmed output resistance between Terminal W and Terminal B are

AD5121:

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + R_W \qquad \text{From 0x00 to 0x7F} \qquad (1)$$

AD5141:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \qquad \text{From 0x00 to 0xFF} \qquad (2)$$

where:
D is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.

In potentiometer mode, similar to the mechanical potentiometer, the resistance of the RDAC between Terminal W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} also gives a maximum of 8% absolute resistance error. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

AD5121:

$$R_{AW}(D) = \frac{128 - D}{128} \times R_{AB} + R_W \qquad \text{From 0x00 to 0x7F} \qquad (3)$$

AD5141:

$$R_{AW}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \qquad \text{From 0x00 to 0xFF} \qquad (4)$$

where:
D is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.

If the part is configured in linear gain setting mode, the resistance between Terminal W and Terminal A is directly proportional to the code loaded in the associate RDAC register. The general equations for this operation are

AD5121:

$$R_{AW}(D) = \frac{D}{128} \times R_{AB} + R_W \quad \text{From 0x00 to 0x7F} \quad (5)$$

AD5141:

$$R_{AW}(D) = \frac{D}{256} \times R_{AB} + R_W \quad \text{From 0x00 to 0xFF} \quad (6)$$

where:
D is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.

In the bottom scale condition or top scale condition, a finite total wiper resistance of 40 Ω is present. Regardless of which setting the part is operating in, limit the current between Terminal A to Terminal B, Terminal W to Terminal A, and Terminal W to Terminal B, to the maximum continuous current of ±6 mA or to the pulse current specified in Table 7. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Calculate the Actual End-to-End Resistance

The resistance tolerance is stored in the internal memory during factory testing. Therefore, the actual end-to-end resistance can be calculated (which is valuable for calibration, tolerance matching, and precision applications).

The resistance tolerance (in percentage) is stored in fixed point format, using a 16-bit sign magnitude binary. The sign bit (0 = negative and 1 = positive) and the integer part are located in Address 0x02, as shown in Table 19. Address 0x03 contains the fractional part, as shown in Table 19.

That is, if the data readback from Address 0x02 is 00000010, and the data readback from Address 0x03 is 10110000, the end-to-end resistance can be calculated as follows.

For Memory Map Address 0x02, DB[7] = 0 = negative, and DB[6:0] = 0000010 = 2.

For Memory Map Address 0x03, DB[7:0] = 10110000 = 176 × 2^{-8} = 0.6875, and therefore, tolerance = −2.6875%, and R_{AB} = 9.731 kΩ.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B, as shown in Figure 43.

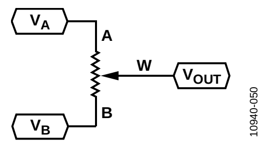

Figure 43. Potentiometer Mode Configuration

Connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 5 V. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B \quad (7)$$

where:
$R_{WB}(D)$ can be obtained from Equation 1 and Equation 2.
$R_{AW}(D)$ can be obtained from Equation 3 and Equation 4.

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{AW} and R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

Table 19. End-to-End Resistance Tolerance Bytes

	Data Byte							
Memory Map Address	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0x02	Sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0x03	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

TERMINAL VOLTAGE OPERATING RANGE

The AD5121/AD5141 are designed with internal ESD diodes for protection. These diodes also set the voltage boundary of the terminal operating voltages. Positive signals present on Terminal A, Terminal B, or Terminal W that exceed V_{DD} are clamped by the forward-biased diode. There is no polarity constraint between V_A, V_W, and V_B, but they cannot be higher than V_{DD} or lower than V_{SS}.

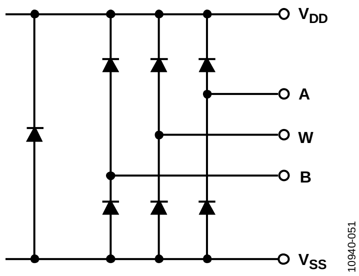

Figure 44. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 44), it is important to power up V_{DD} first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally. The ideal power-up sequence is V_{SS}, V_{DD}, V_{LOGIC}, digital inputs, and V_A, V_B, and V_W. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{SS}, V_{DD}, and V_{LOGIC}. Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{LOGIC} is powered, the power-on preset activates, which restores EEPROM values to the RDAC registers.

LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use a compact, minimum lead length layout design. Ensure that the leads to the input are as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Apply low equivalent series resistance (ESR) 1 µF to 10 µF tantalum or electrolytic capacitors at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 45 illustrates the basic supply bypassing configuration for the AD5121/AD5141.

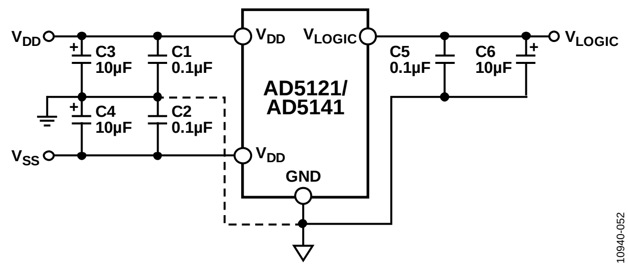

Figure 45. Power Supply Bypassing

OUTLINE DIMENSIONS

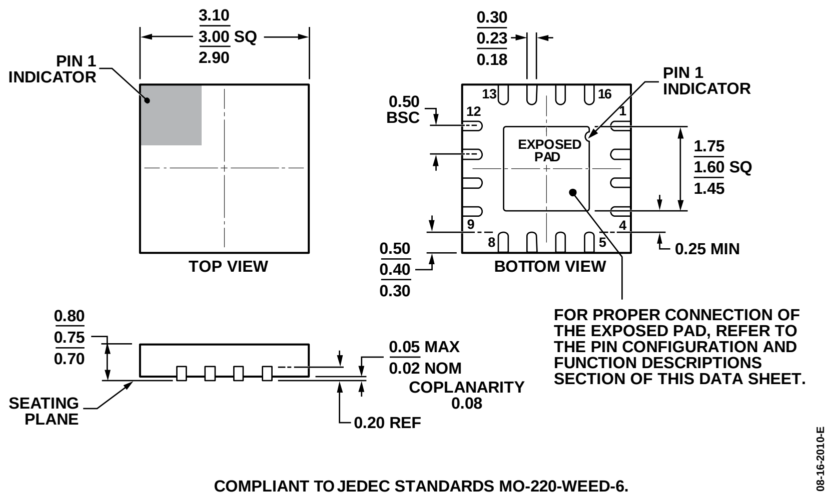

Figure 46. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{AB} (kΩ)	Resolution	Interface	Temperature Range	Package Description	Package Option	Branding
AD5121BCPZ10-RL7	10	128	SPI/I²C	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DHE
AD5121BCPZ100-RL7	100	128	SPI/I²C	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DHF
AD5141BCPZ10-RL7	10	256	SPI/I²C	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DHC
AD5141BCPZ100-RL7	100	256	SPI/I²C	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DHD
EVAL-AD5141DBZ					Evaluation Board		

[1] Z = RoHS Compliant Part
[2] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with both of the available resistor value options.

NOTES

NOTES

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D10940-0-12/12(A)

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- Подбор аналогов;
- Консультации по применению компонента;
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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