



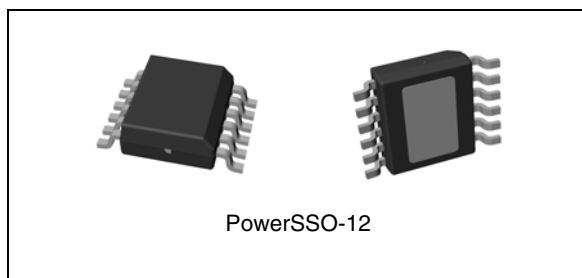
# VN750PEP-E

## High side driver

### Features

Type	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VN750PEP-E	60 m $\Omega$	6 A	36 V

- ECOPACK<sup>®</sup> : lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protection (see [Application schematic on page 13](#))
- In compliance with the 2002/95/EC european directive



### Description

The VN750PEP-E is a monolithic device designed in STMicroelectronics VIPower™ M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart help protect the device against overload.

The device detects open load condition in on and off-state. Output shorted to  $V_{CC}$  is detected in the off-state. Device automatically turns off in case of ground pin disconnection.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VN750PEP-E	VN750PEPTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

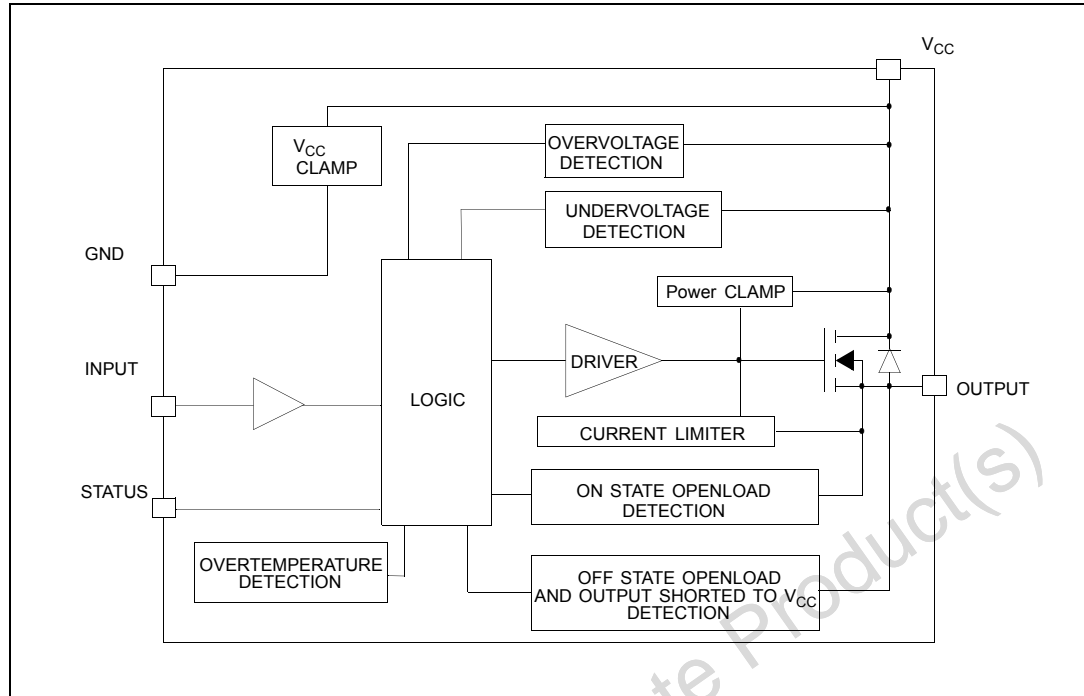


Figure 2. Configuration diagram (top view)

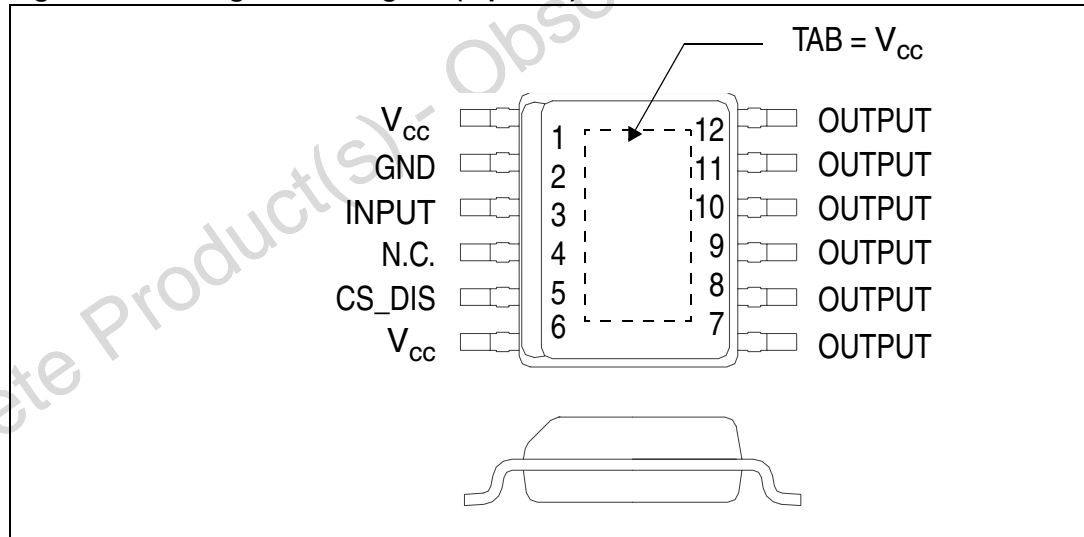
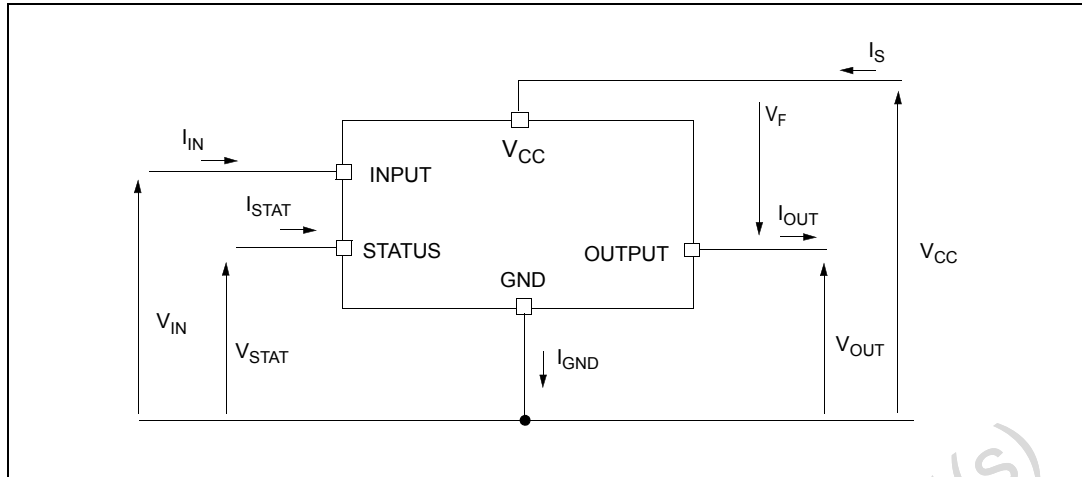


Table 2. Suggested connections for unused and not connected pins

Connection/pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 KΩ resistor

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stress values that exceed those listed in the “Absolute maximum ratings” table can cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions greater than those, indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	- 0.3	V
$-I_{gnd}$	DC reverse ground pin current	- 200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	- 6	A
$I_{IN}$	DC input current	+/- 10	mA
$I_{STAT}$	DC status current	+/- 10	mA
$V_{ESD}$	Electrostatic discharge (human body model: R=1.5 K $\Omega$ ; C=100pF)		
	- Input	4000	V
	- Status	4000	V
	- Output	5000	V
	- $V_{CC}$	5000	V
$P_{tot}$	Power dissipation $T_C=25^\circ C$	74	W

**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
$T_j$	Junction operating temperature	Internally limited	°C
$T_c$	Case operating temperature	- 40 to 150	°C
$T_{stg}$	Storage temperature	- 55 to 150	°C

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Max. value		Unit
$R_{thj-case}$	Thermal resistance junction-case	1.7		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	61 <sup>(1)</sup>	50 <sup>(2)</sup>	°C/W

- When mounted on a standard single-sided FR-4 board with 1cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins.
- When mounted on a standard single-sided FR-4 board with 8cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins.

## 2.3 Electrical characteristics

Values specified in this section are for 8 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>j</sub> < 150 °C, unless otherwise stated.

**Table 5. Power**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Operating supply voltage		5.5	13	36	V
V <sub>USD</sub>	Undervoltage shutdown		3	4	5.5	V
V <sub>USDhyst</sub>	Undervoltage shutdown hysteresis			0.5		V
V <sub>OV</sub>	Overvoltage shutdown		36			V
R <sub>ON</sub>	On-state resistance	I <sub>OUT</sub> =2 A; T <sub>j</sub> =25 °C; V <sub>CC</sub> > 8 V I <sub>OUT</sub> =2 A; V <sub>CC</sub> > 8 V			60 120	mΩ mΩ
I <sub>S</sub>	Supply current	Off-state; V <sub>CC</sub> =13 V; V <sub>IN</sub> =V <sub>OUT</sub> =0 V Off-state; V <sub>CC</sub> =13 V; V <sub>IN</sub> =V <sub>OUT</sub> =0 V; T <sub>j</sub> =25 °C On-state; V <sub>CC</sub> =13 V; V <sub>IN</sub> =5 V; I <sub>OUT</sub> =0 A		10 10 2	25 20 3.5	µA µA mA
I <sub>L(off1)</sub>	Off-state output current	V <sub>IN</sub> =V <sub>OUT</sub> =0 V	0		50	µA
I <sub>L(off2)</sub>	Off-state output current	V <sub>IN</sub> =0V; V <sub>OUT</sub> =3.5 V	-75		0	µA
I <sub>L(off3)</sub>	Off-state output current	V <sub>IN</sub> =V <sub>OUT</sub> =0 V; V <sub>CC</sub> =13 V; T <sub>j</sub> =125 °C			5	µA
I <sub>L(off4)</sub>	Off-state output current	V <sub>IN</sub> =V <sub>OUT</sub> =0 V; V <sub>CC</sub> =13 V; T <sub>j</sub> =25 °C			3	µA

Table 6. Switching ( $V_{CC}=13\text{ V}$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=6.5\ \Omega$ from $V_{IN}$ rising edge to $V_{OUT}=1.3\text{ V}$	-	40	-	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time	$R_L=6.5\ \Omega$ from $V_{IN}$ falling edge to $V_{OUT}=11.7\text{ V}$	-	30	-	$\mu\text{s}$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L=6.5\ \Omega$ from $V_{OUT}=1.3\text{ V}$ to $V_{OUT}=10.4\text{ V}$	-	0.5	-	$\text{V}/\mu\text{s}$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L=6.5\ \Omega$ from $V_{OUT}=11.7\text{ V}$ to $V_{OUT}=1.3\text{ V}$	-	0.2	-	$\text{V}/\mu\text{s}$

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level				1.25	V
$I_{IL}$	Low level input current	$V_{IN}=1.25\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level		3.25			V
$I_{IH}$	High level input current	$V_{IN}=3.25\text{ V}$			10	$\mu\text{A}$
$V_{hyst}$	Input hysteresis voltage		0.5			V
$V_{ICL}$	Input clamp voltage	$I_{IN}=1\text{ mA}$ $I_{IN}=-1\text{ mA}$	6	6.8 -0.7	8	V V

Table 8.  $V_{CC}$  output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT}=1.3\text{ A}$ ; $T_j=150\text{ }^\circ\text{C}$			0.6	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT}=1.6\text{ mA}$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT}=5\text{ V}$			10	$\mu\text{A}$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT}=5\text{ V}$			100	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT}=1\text{ mA}$ $I_{STAT}=-1\text{ mA}$	6	6.8 -0.7	8	V V

Table 10. Protections<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	175	200	$^\circ\text{C}$
$T_R$	Reset temperature		135			$^\circ\text{C}$



**Table 10. Protections<sup>(1)</sup> (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{hyst}$	Thermal hysteresis		7	15		°C
$t_{SDL}$	Status delay in overload condition	$T_j > T_{jsh}$			20	ms
$I_{lim}$	Current limitation	$9 V < V_{CC} < 36 V$ $5 V < V_{CC} < 36 V$	6	9	15 15	A A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2 A; V_{IN} = 0 V; L = 6 mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

**Table 11. Open-load detection**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{OL}$	Open-load on-state detection threshold	$V_{IN} = 5 V$	50	100	200	mA
$t_{DOL(on)}$	Open-load on-state detection delay	$I_{OUT} = 0 A$			200	µs
$V_{OL}$	Open-load off-state voltage detection threshold	$V_{IN} = 0 V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	µs

**Figure 4. Status timings**

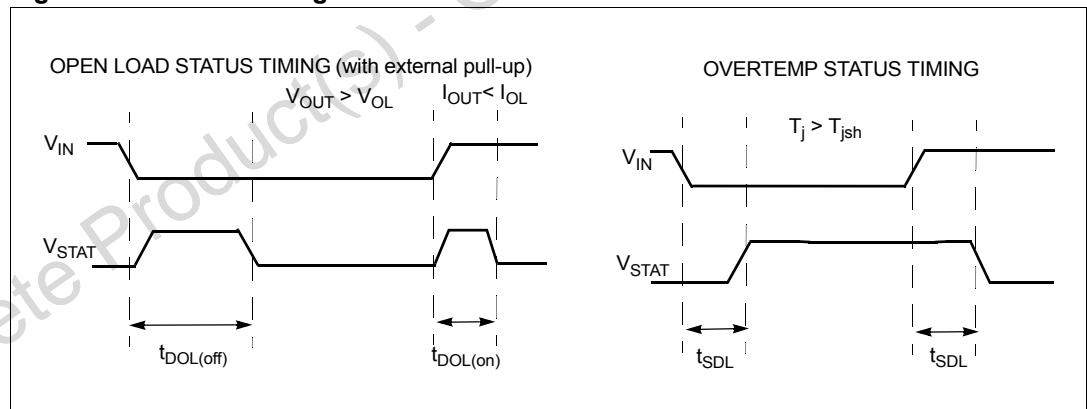


Figure 5. Switching time waveforms

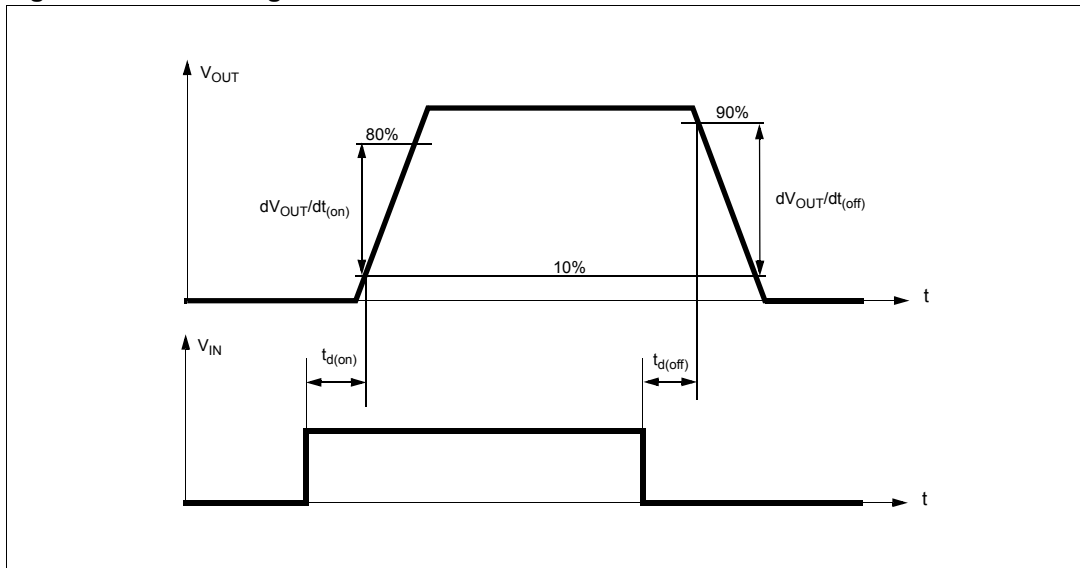


Table 12. Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	( $T_j < T_{TSD}$ ) H ( $T_j > T_{TSD}$ ) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage > $V_{OL}$	L	H	L
	H	H	H
Output current < $I_{OL}$	L	L	H
	H	H	L

Table 13. Electrical transient requirements on  $V_{CC}$  pin (part 1/3)

ISO T/R 7637/1 test pulse	Test levels				Delays and impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 $\Omega$
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 $\Omega$
3a	-25 V	-50 V	-100 V	-150 V	0.1 $\mu$ s 50 $\Omega$

**Table 13. Electrical transient requirements on V<sub>CC</sub> pin (part 1/3) (continued)**

ISO T/R 7637/1 test pulse	Test levels				Delays and impedance
	I	II	III	IV	
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

**Table 14. Electrical transient requirements on V<sub>CC</sub> pin (part 2/3)**

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

**Table 15. Electrical transient requirements on V<sub>CC</sub> pin (part 3/3)**

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms

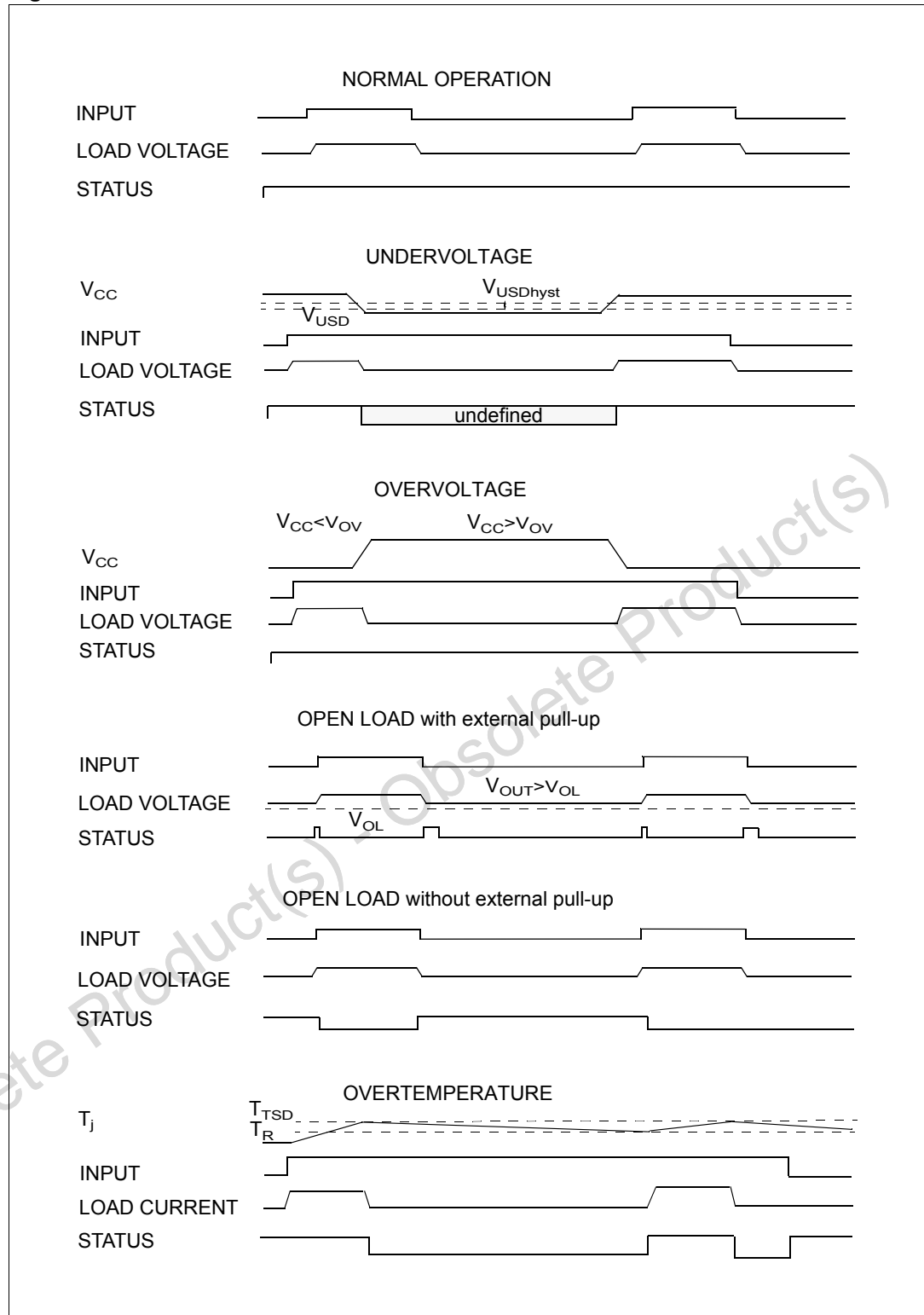
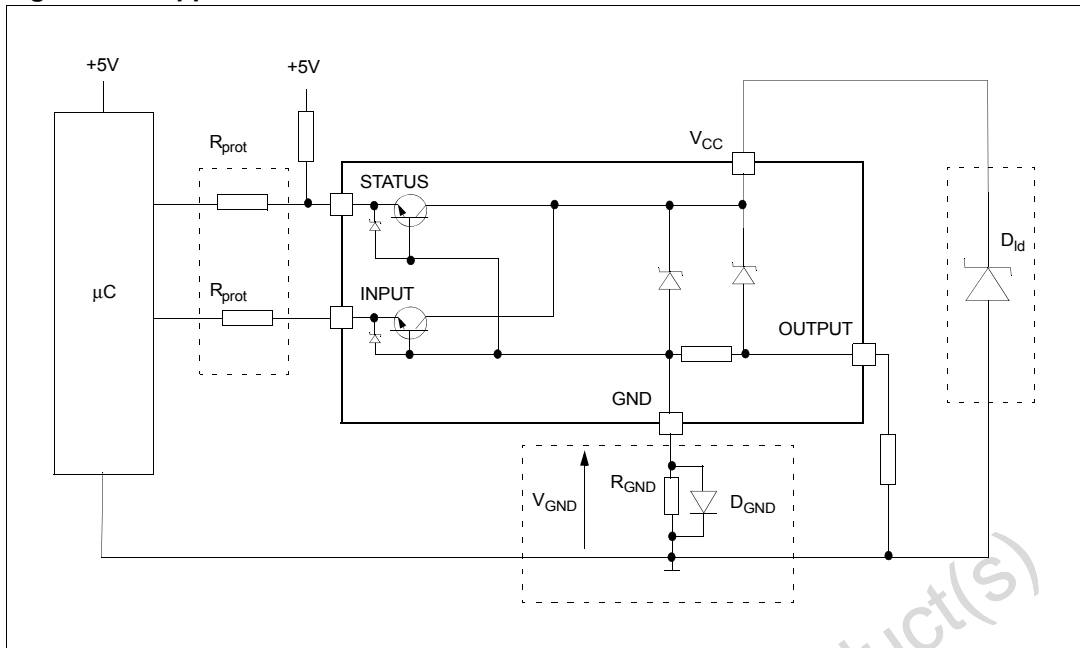


Figure 7. Application schematic



## 2.4 GND protection network against reverse battery

### 2.4.1 Solution 1: resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

1.  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R<sub>GND</sub> (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R<sub>GND</sub> produces a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

### 2.4.2 Solution 2: diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND}=1\text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ( $\approx 600\text{mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

Series resistor in input and status lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused input and status pin is to leave them unconnected.

## 2.5 Load dump protection

$D_{ld}$  is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 2.6 Microcontroller I/Os protection

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins is pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu\text{C}$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu\text{C}$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu\text{C}$  I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

$$\text{For } V_{CCpeak} = -100\text{ V and } I_{latchup} \geq 20\text{ mA; } V_{OH\mu C} \geq 4.5\text{ V}$$

$$5\text{ k}\Omega \leq R_{prot} \leq 65\text{ k}\Omega.$$

Recommended values:  $R_{prot} = 10\text{ k}\Omega$ .

## 2.7 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between output pin and a positive supply voltage ( $V_{PU}$ ) like the +5 V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

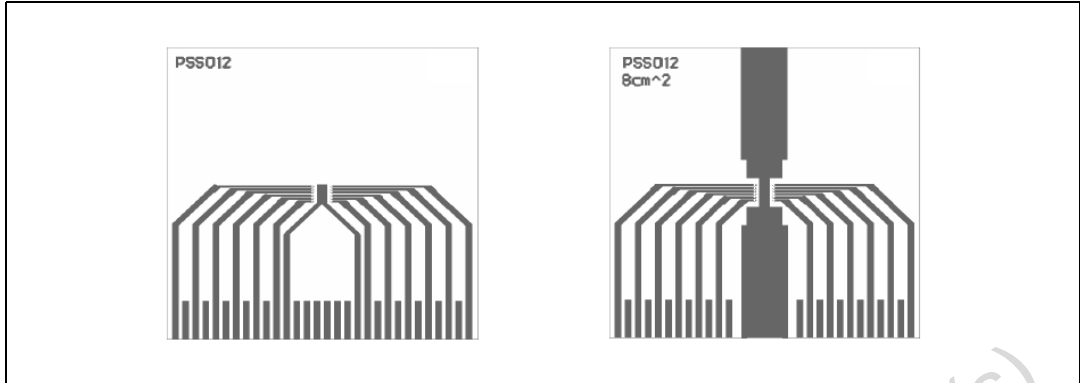
- no false open-load indication when load is connected: in this case we have to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition  $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$ .
- no misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .



### 3 Package and PCB thermal data

#### 3.1 PowerSSO-12 thermal data

Figure 9. PowerSSO-12 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 78 mm x 78 mm, PCB thickness = 2 mm, Cu thickness=35  $\mu$ m, Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

Figure 10.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

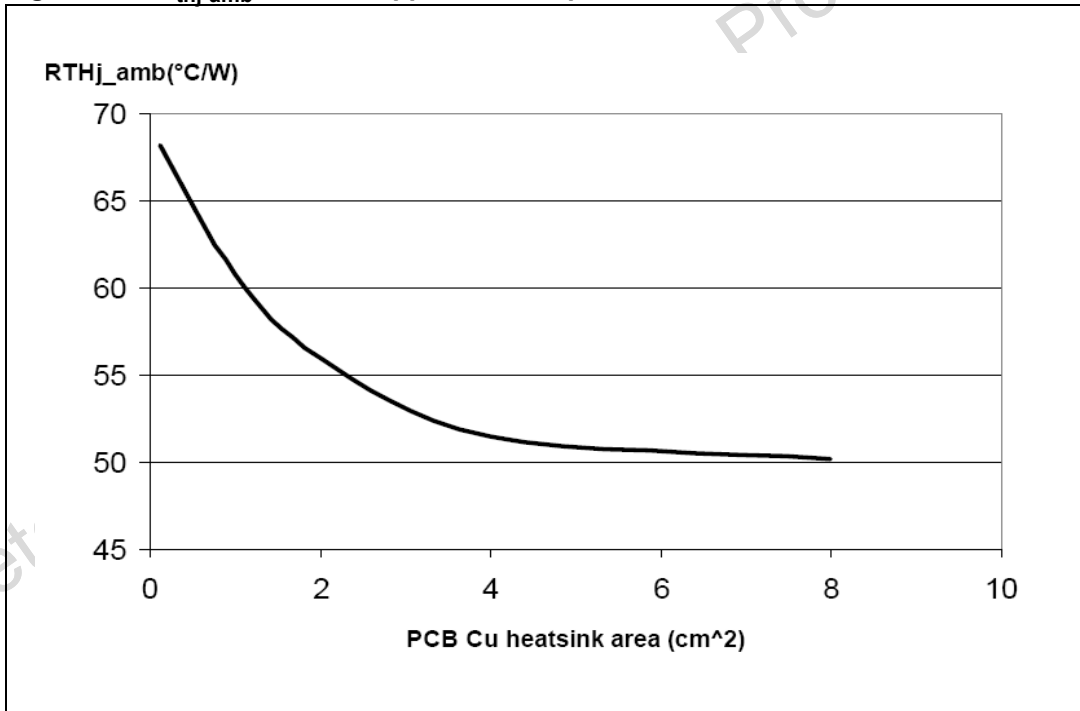
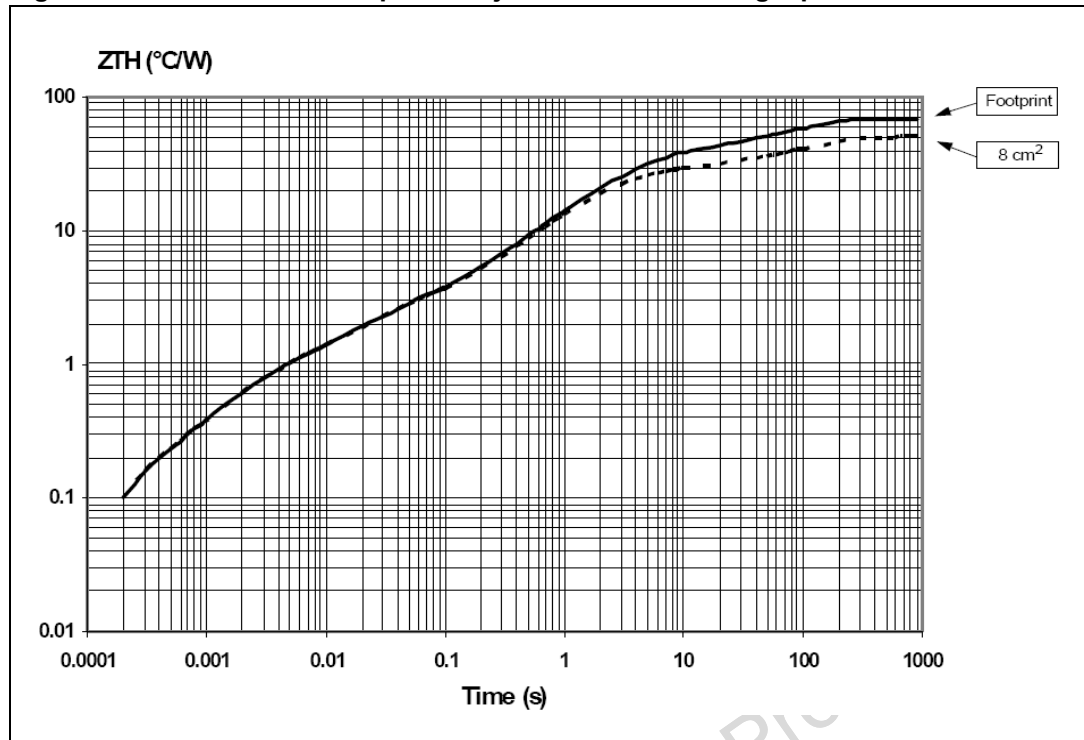




Figure 11. P<sup>2</sup>PAK thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 12. PowerSSO-12 thermal fitting model of a single channel

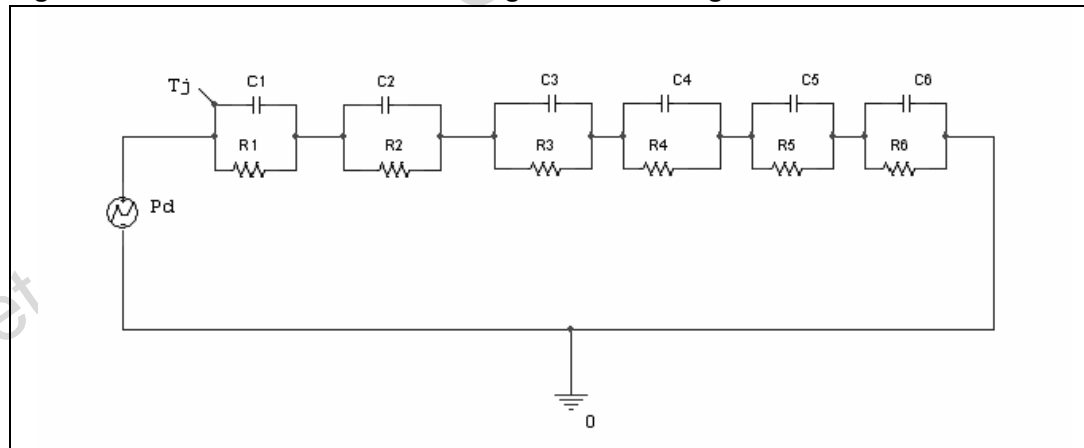


Table 16. PowerSSO-12 thermal parameter

Area/island (cm <sup>2</sup> )	Footprint	8
R1 (°C/W)	0.1	
R2 (°C/W)	0.6	

Table 16. PowerSSO-12 thermal parameter (continued)

Area/island (cm <sup>2</sup> )	Footprint	8
R3 (°C/W)	1.5	
R4 (°C/W)	8	
R5 (°C/W)	28	18
R6 (°C/W)	30	22
C1 (W·s/°C)	0.001	
C2 (W·s/°C)	0.0035	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.1	
C5 (W·s/°C)	0.15	0.017
C6 (W·s/°C)	3	5

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## 4 Package and packing information

### 4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 4.2 PowerSSO-12 mechanical data

Figure 13. PowerSSO-12 package dimensions

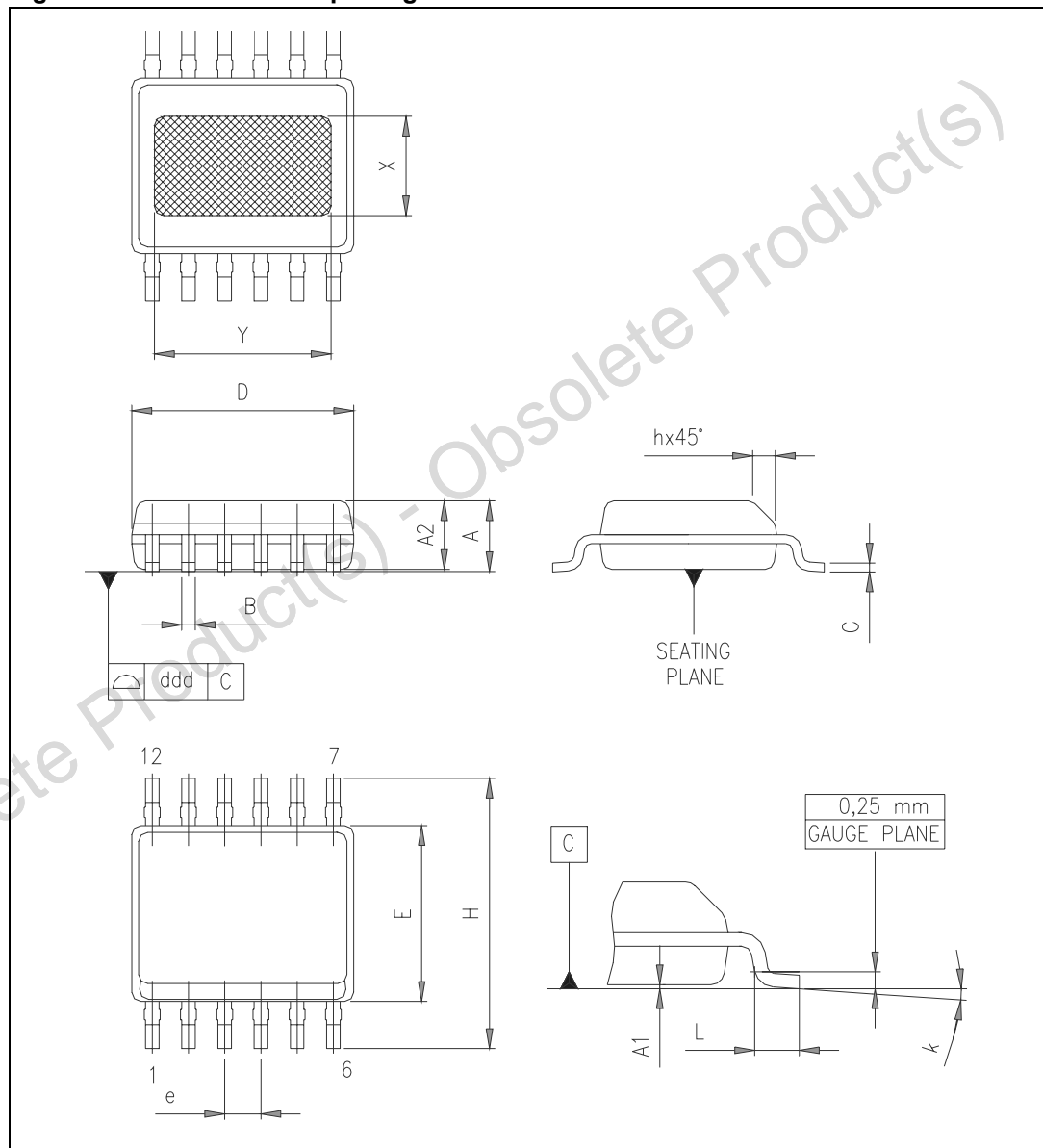


Table 17. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.62
A1	0		0.1
A2	1.10		1.65
B	0.23		0.41
C	0.19		0.25
D	4.8		5.0
E	3.8		4.0
e		0.8	
H	5.8		6.2
h	0.25		0.5
L	0.4		1.27
k	0°		8°
X	1.9		2.5
Y	3.6		4.2
ddd			0.1

## 5 Revision history

Table 18. Document revision history

Date	Revision	Changes
07-Oct-2004	1	Initial release.
24-Nov-2004	2	PowerSSO-12 thermal characteristics insertion.
12-Dec-2004	3	Thermal data correction.
23-Nov-2009	4	Updated feature list.

Obsolete Product(s) - Obsolete Product(s)

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