

N-channel 100 V, 2.6 mΩ typ., 180 A, STripFET™ F7 Power MOSFET in a TO-247 package

Datasheet - production data

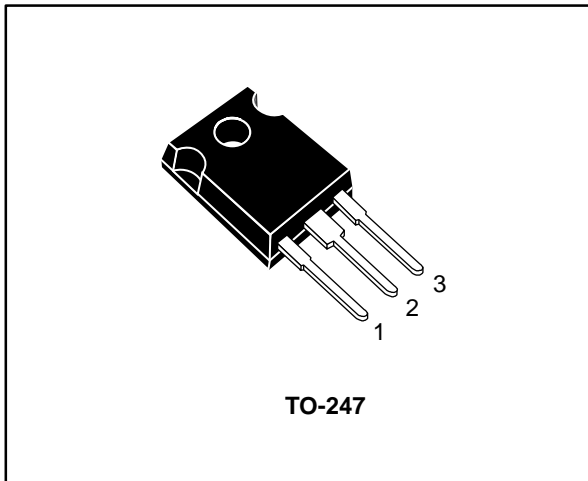
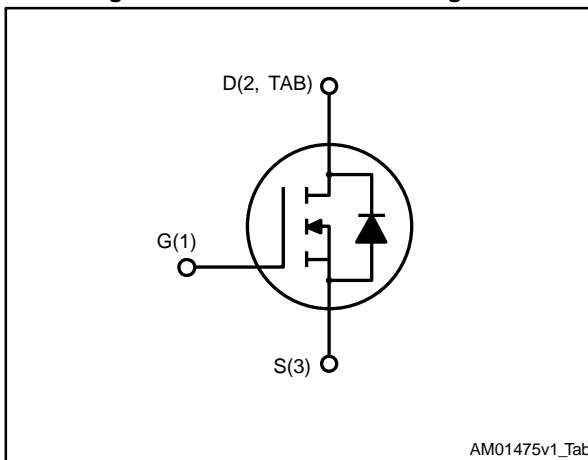


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STW240N10F7	100 V	3.0 mΩ	180 A

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STW240N10F7	240N10F7	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	180	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	160	A
$I_D^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	300	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	500	mJ
T_J	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		$^{\circ}\text{C}$

Notes:

(1) Current limited by package

(2) Pulse width limited by safe operating area

(3) Starting $T_J = 25\text{ °C}$, $I_D = 45\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	$^{\circ}\text{C/W}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	100			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 100 V			1	μA
		V _{GS} = 0, V _{DS} = 100 V; T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 90 A		2.6	3.0	mΩ

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{ISS}	Input capacitance	V _{GS} = 0, V _{DS} = 25 V, f = 1 MHz	-	11550	-	pF
C _{OSS}	Output capacitance			2950		pF
C _{RSS}	Reverse transfer capacitance			217		pF
Q _g	Total gate charge	V _{DD} = 50 V, I _D = 180 A	-	160	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V		48		nC
Q _{gd}	Gate-drain charge	(see Figure 14 : "Test circuit for gate charge behavior")		38		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 90 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13 : "Test circuit for resistive load switching times")	-	49	-	ns
t _r	Rise time			139		ns
t _{d(off)}	Turn-off delay time			110		ns
t _f	Fall time			112		ns

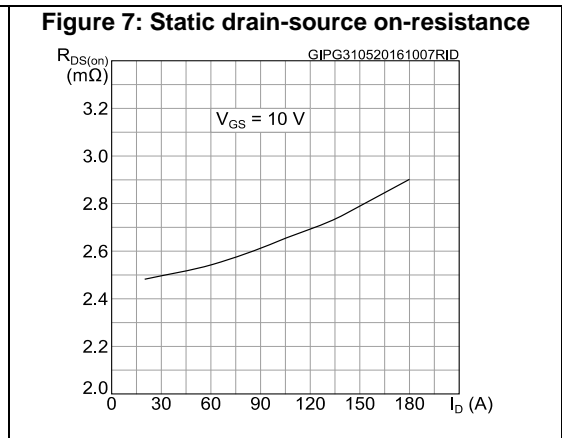
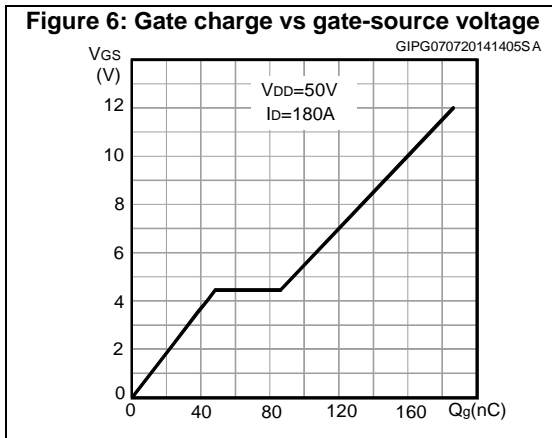
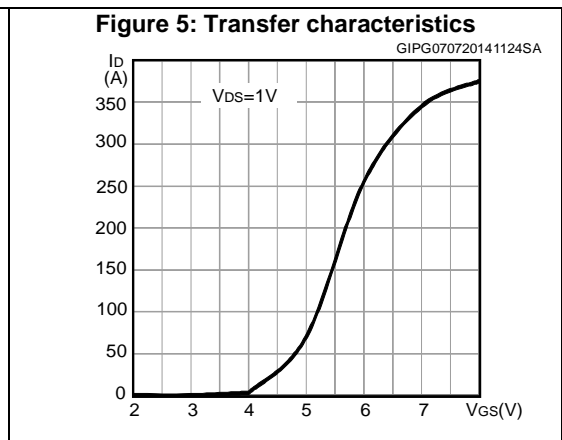
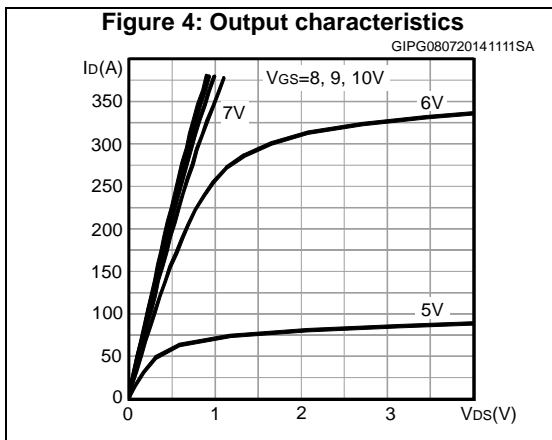
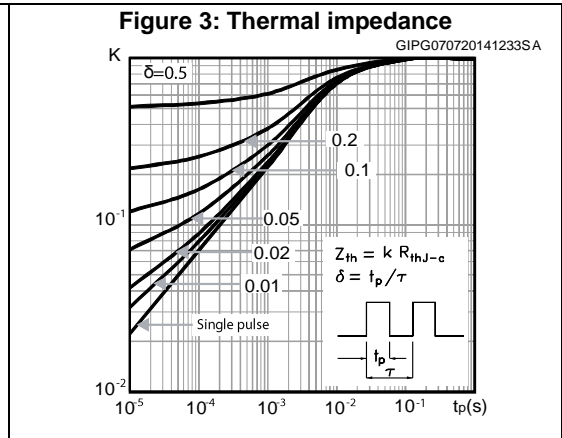
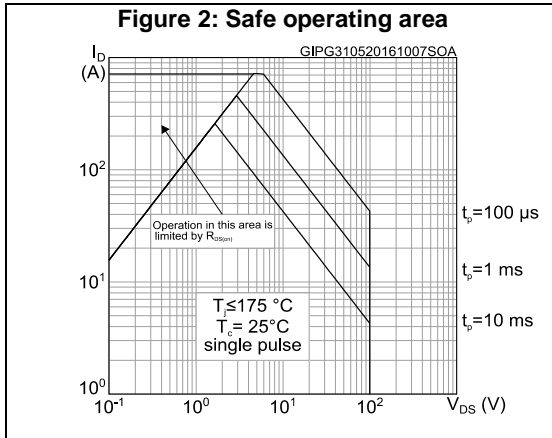
Table 7: Source-drain diode

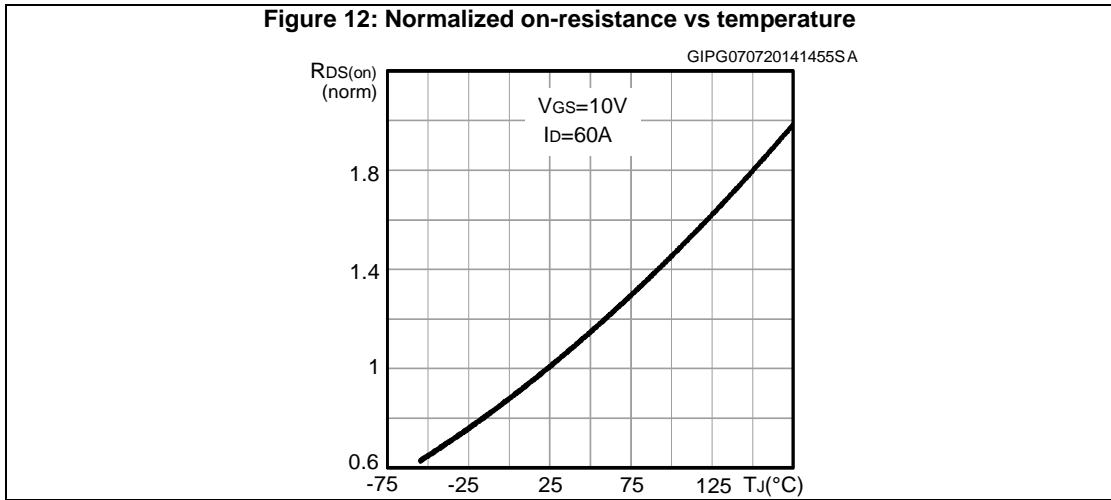
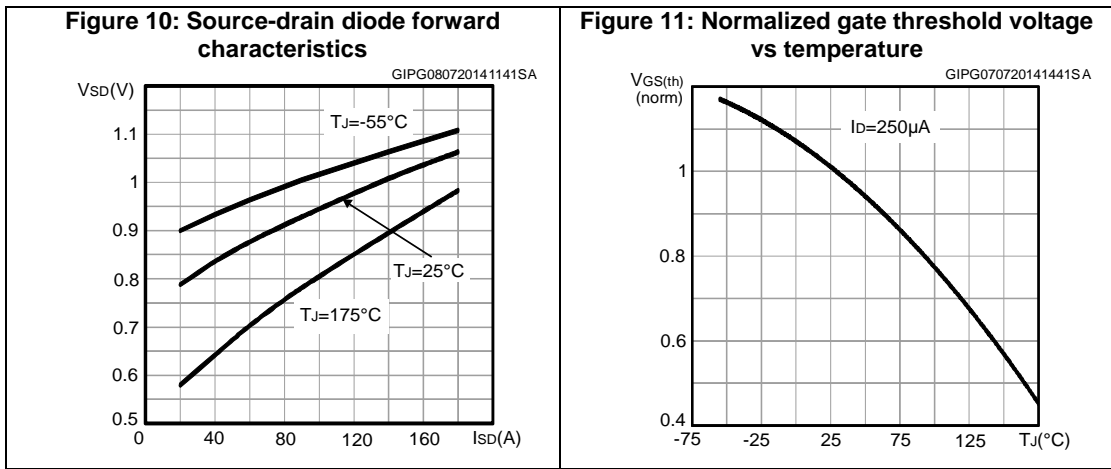
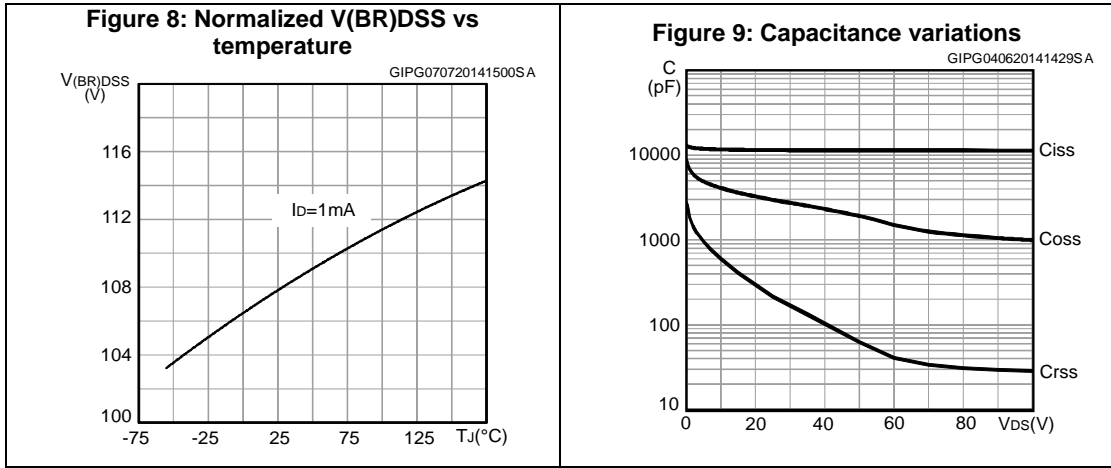
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 180 \text{ A}$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 180 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 80 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")		108		ns
Q_{rr}	Reverse recovery charge			315		nC
I_{RRM}	Reverse recovery current			5.8		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

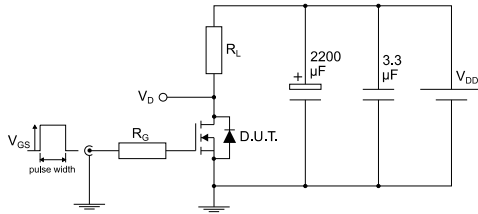
2.1 Electrical characteristics (curves)





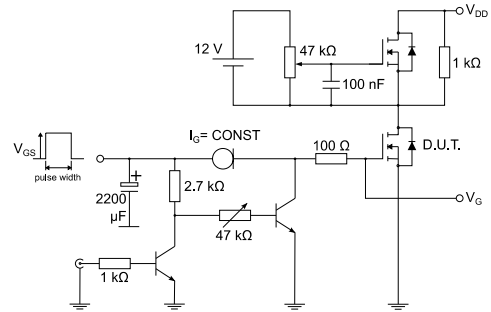
3 Test circuits

Figure 13: Test circuit for resistive load switching times



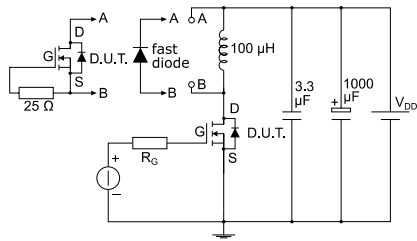
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Figure 14: Test circuit for gate charge behavior



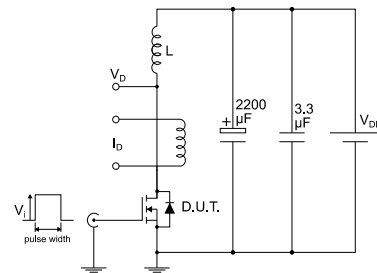
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Figure 15: Test circuit for inductive load switching and diode recovery times



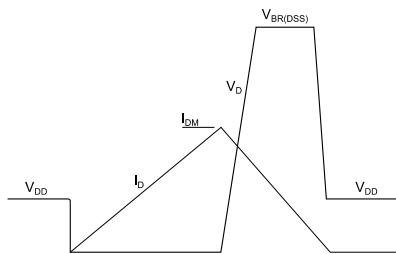
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Figure 16: Unclamped inductive load test circuit



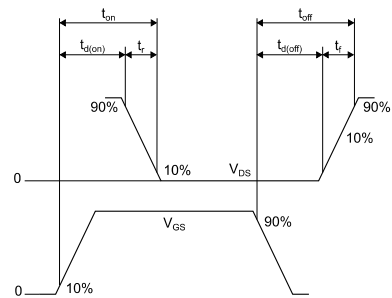
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 19: TO-247 package outline

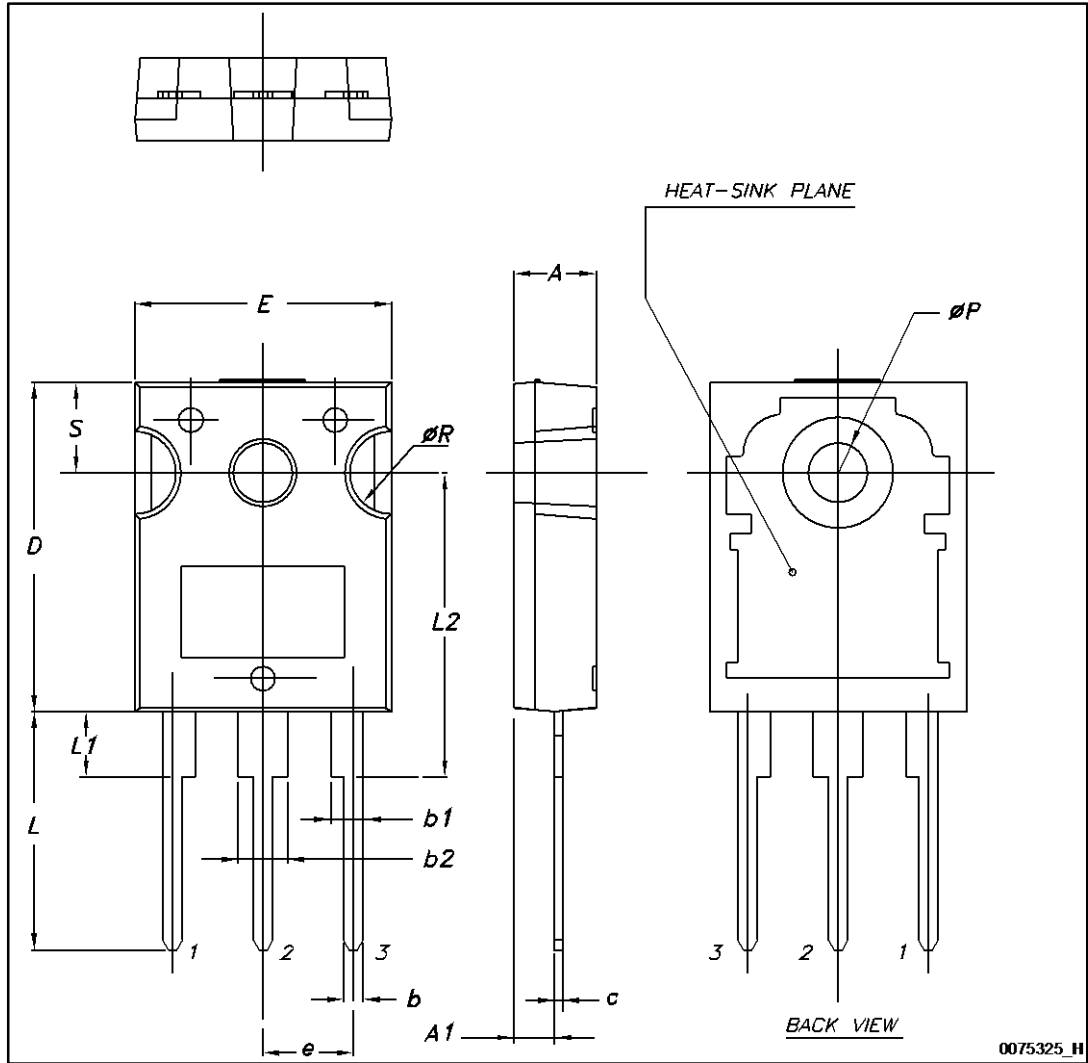


Table 8: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
06-Jun-2016	1	Initial release.
08-Jul-2016	2	Document status promoted from preliminary to production data.

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.