# IS63WV1024BLL
# IS64WV1024BLL

## 128K x 8 HIGH-SPEED CMOS STATIC RAM

**MAY 2012**

### FEATURES

- High-speed access time:
  12 ns: 3.3V ± 10%
  15 ns: 2.5V – 3.6V
- High-performance, low-power CMOS process
- CMOS Low Power Operation
  50 mW (typical) operating current
  25 µW (typical) standby current
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Packages available:
  – 32-pin TSOP (Type II)
  – 32-pin sTSOP (Type I)
  – 48-Ball miniBGA (6mm x 8mm)
  – 32-pin 300-mil SOJ
- Lead-free available

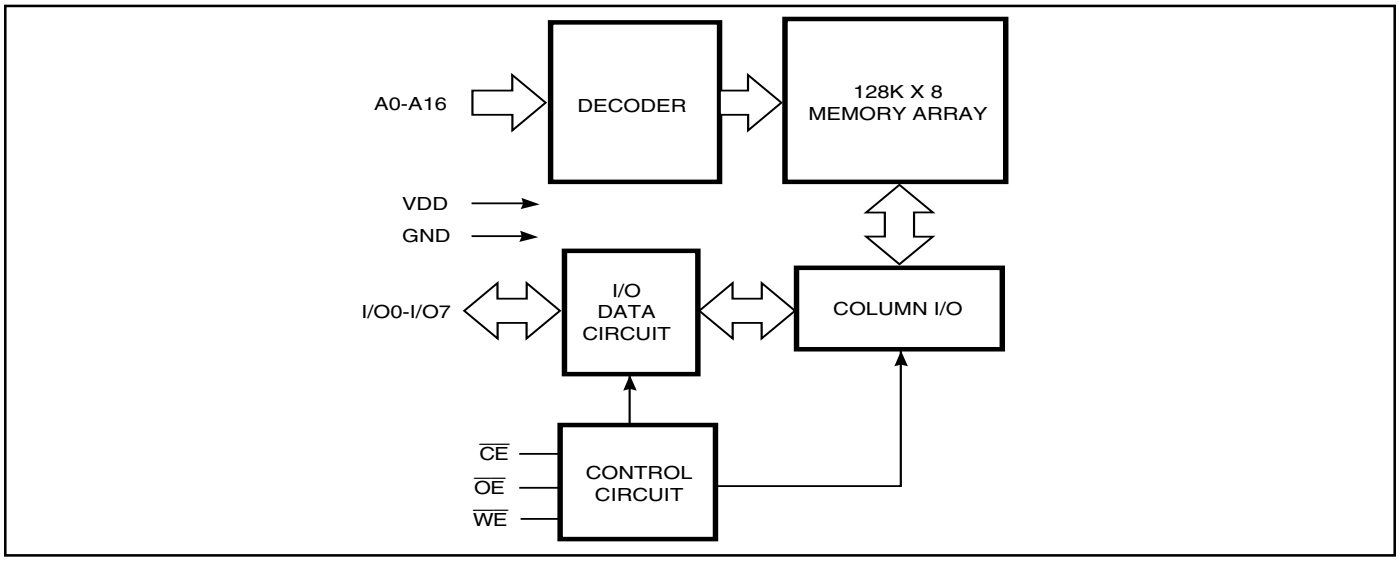
### DESCRIPTION

The *ISSI* IS63/64WV1024BLL is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM. The IS63/64WV1024BLL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

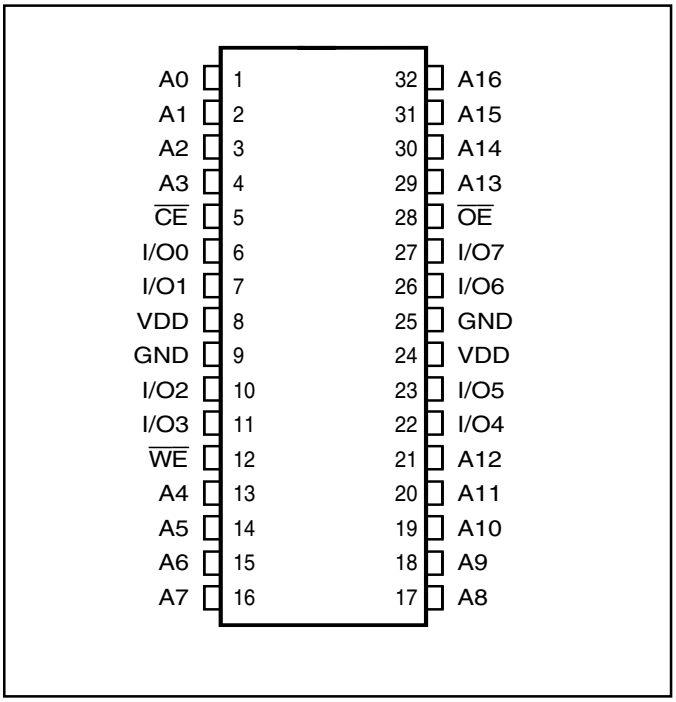
When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 25 µW (typical) with CMOS input levels.

The IS63/64WV1024BLL operates from a single $V_{DD}$ power supply. The IS63/64WV1024BLL is available in 32-pin TSOP (Type II), 32-pin sTSOP (Type I), 48-Ball miniBGA (6mm x 8mm), and 32-pin SOJ (300-mil) packages.

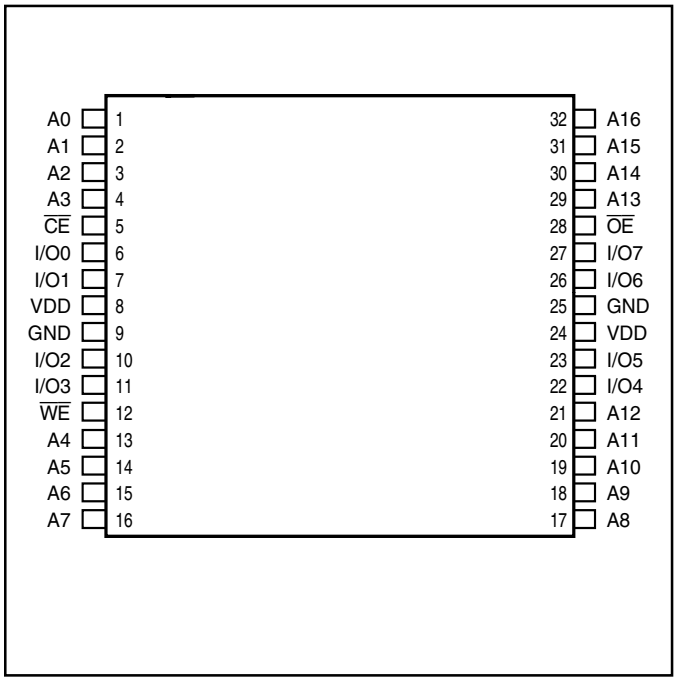
### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION
### 32-Pin SOJ



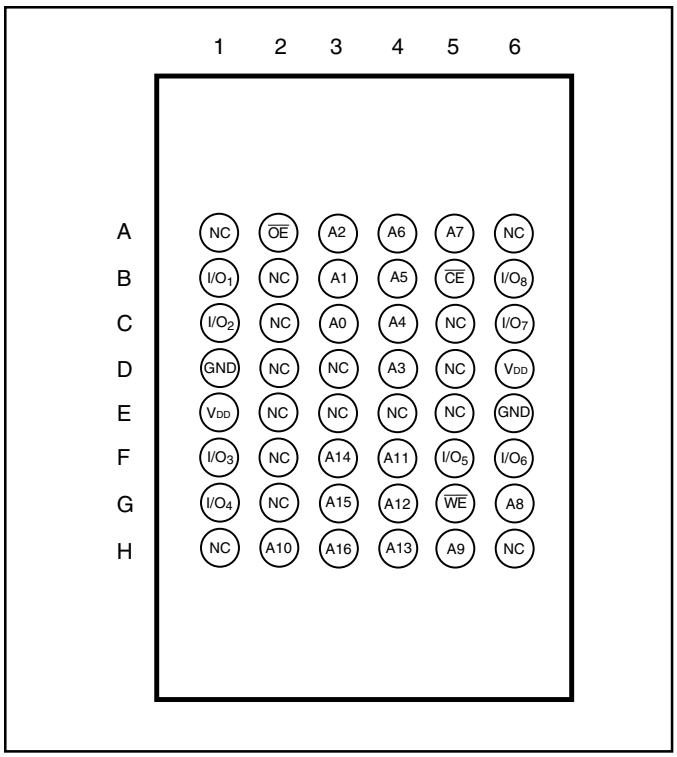

## PIN CONFIGURATION
### 32-Pin TSOP (Type II) (T)
### 32-Pin sTSOP (Type I) (H)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A16 | Address Inputs |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write Enable Input |
| I/O0-I/O7 | Bidirectional Ports |
| $V_{DD}$ | Power |
| GND | Ground |

## PIN CONFIGURATION
### 48-mini BGA (B) (6 mm x 8 mm)



## TRUTH TABLE

| Mode | $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | I/O Operation | $V_{DD}$ Current |
|---|---|---|---|---|---|
| Not Selected (Power-down) | X | H | X | High-Z | $I_{SB1}$, $I_{SB2}$ |
| Output Disabled | H | L | H | High-Z | $I_{CC1}$, $I_{CC2}$ |
| Read | H | L | L | $D_{OUT}$ | $I_{CC1}$, $I_{CC2}$ |
| Write | L | L | X | $D_{IN}$ | $I_{CC1}$, $I_{CC2}$ |

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to $V_{DD}$+0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.5 | W |
| $V_{DD}$ | $V_{DD}$ Related to GND | -0.2 to +3.9 | V |

**Note:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE ($V_{DD}$)

| Range | Ambient Temperature | $V_{DD}$ (15 ns) | $V_{DD}$ (12 ns) |
|---|---|---|---|
| Commercial | 0°C to +70°C | 2.5V-3.6V | 3.3V $\pm$ 10% |
| Industrial | –40°C to +85°C | 2.5V-3.6V | 3.3V $\pm$ 10% |
| Automotive | –40°C to +125°C | 2.5V-3.6V | 3.3V $\pm$ 10% |

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

### $V_{DD}$ = 2.5V-3.6V

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –1.0 mA | 2.3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 1.0 mA | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{DD}$ | –2 | 2 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{DD}$, Outputs Disabled | –2 | 2 | µA |

**Note:**
1. $V_{IL}$ (min.) = –0.3V DC; $V_{IL}$ (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   $V_{IH}$ (max.) = $V_{DD}$ + 0.3V DC; $V_{IH}$ (max.) = $V_{DD}$ + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

### $V_{DD}$ = 3.3V ± 10%

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –4.0 mA | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 8.0 mA | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{DD}$ | –2 | 2 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{DD}$, Outputs Disabled | –2 | 2 | µA |

**Note:**
1. $V_{IL}$ (min.) = –0.3V DC; $V_{IL}$ (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   $V_{IH}$ (max.) = $V_{DD}$ + 0.3V DC; $V_{IH}$ (max.) = $V_{DD}$ + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | Test Conditions | Options | -12 ns Min. | -12 ns Max. | -15 ns Min. | -15 ns Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ | COM. | — | 35 | — | 30 | mA |
| | | | IND. | — | 45 | — | 40 | |
| | | | AUTO | — | 60 | — | 50 | |
| | | | typ.[2] | — | 20 | — | 20 | |
| $I_{CC1}$ | Operating Supply Current | $V_{DD}$ = Max., Iout = 0mA, f = 0 | COM. | — | 5 | — | 5 | mA |
| | | | IND. | — | 5 | — | 5 | |
| | | | AUTO | — | 5 | — | 5 | |
| $I_{SB1}$ | TTL Standby Current (TTL Inputs) | $V_{DD}$ = Max., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\overline{CE} \geq V_{IH}$, f = 0 | COM. | — | 3 | — | 3 | mA |
| | | | IND. | — | 4 | — | 4 | |
| | | | AUTO | — | 4 | — | 4 | |
| $I_{SB2}$ | CMOS Standby Current (CMOS Inputs) | $V_{DD}$ = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0 | COM. | — | 20 | — | 20 | uA |
| | | | IND. | — | 50 | — | 50 | |
| | | | AUTO | — | 75 | — | 75 | |
| | | | typ.[2] | — | 6 | — | 6 | |

**Note:**
1. At f = $f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at $V_{DD}$=2.5V, $T_A$=25°C. Not 100% tested.

## CAPACITANCE[1]

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{OUT}$ | Input/Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Note:**
1. Tested initially and after any design or process changes that may affect these parameters.

## AC TEST CONDITIONS

| Parameter | Unit (2.5V-3.6V) | Unit (3.3V ± 10%) |
|---|---|---|
| Input Pulse Level | 0V to $V_{DD}$ V | 0V to $V_{DD}$ V |
| Input Rise and Fall Times | 1.5ns | 1.5ns |
| Input and Output Timing and Reference Level ($V_{Ref}$) | $V_{DD}/2$ | $V_{DD}/2$ + 0.05 |
| Output Load | See Figures 1a and 1b | See Figures 1a and 1b |

## AC TEST LOADS

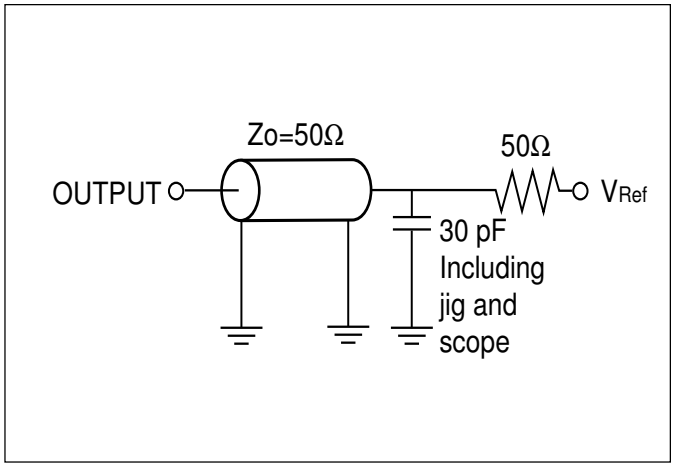



**Figure 1a.**

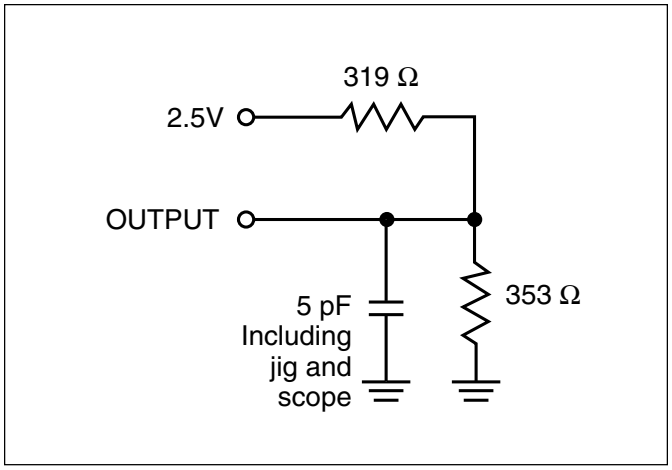



**Figure 1b.**

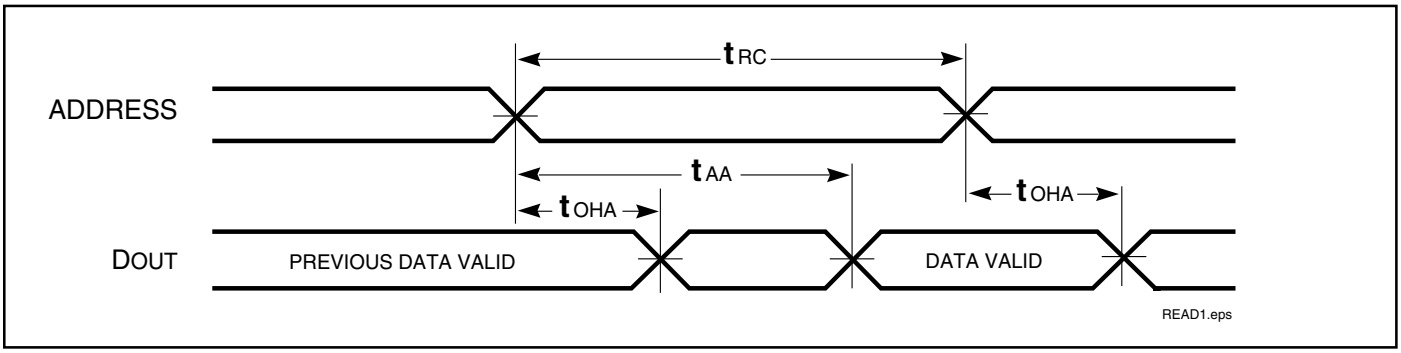
## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | -12 ns Min. | -12 ns Max. | -15 ns Min. | -15 ns Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 12 | — | 15 | — | ns |
| $t_{AA}$ | Address Access Time | — | 12 | — | 15 | ns |
| $t_{OHA}$ | Output Hold Time | 3 | — | 3 | — | ns |
| $t_{ACE}$ | $\overline{CE}$ Access Time | — | 12 | — | 15 | ns |
| $t_{DOE}$ | $\overline{OE}$ Access Time | — | 6 | — | 7 | ns |
| $t_{LZOE}$[2] | $\overline{OE}$ to Low-Z Output | 0 | — | 0 | — | ns |
| $t_{HZOE}$[2] | $\overline{OE}$ to High-Z Output | 0 | 6 | 0 | 6 | ns |
| $t_{LZCE}$[2] | $\overline{CE}$ to Low-Z Output | 3 | — | 3 | — | ns |
| $t_{HZCE}$[2] | $\overline{CE}$ to High-Z Output | 0 | 6 | 0 | 6 | ns |
| $t_{PU}$ | $\overline{CE}$ to Power Up Time | 0 | — | 0 | — | ns |
| $t_{PD}$ | $\overline{CE}$ to Power Down Time | — | 12 | — | 15 | ns |

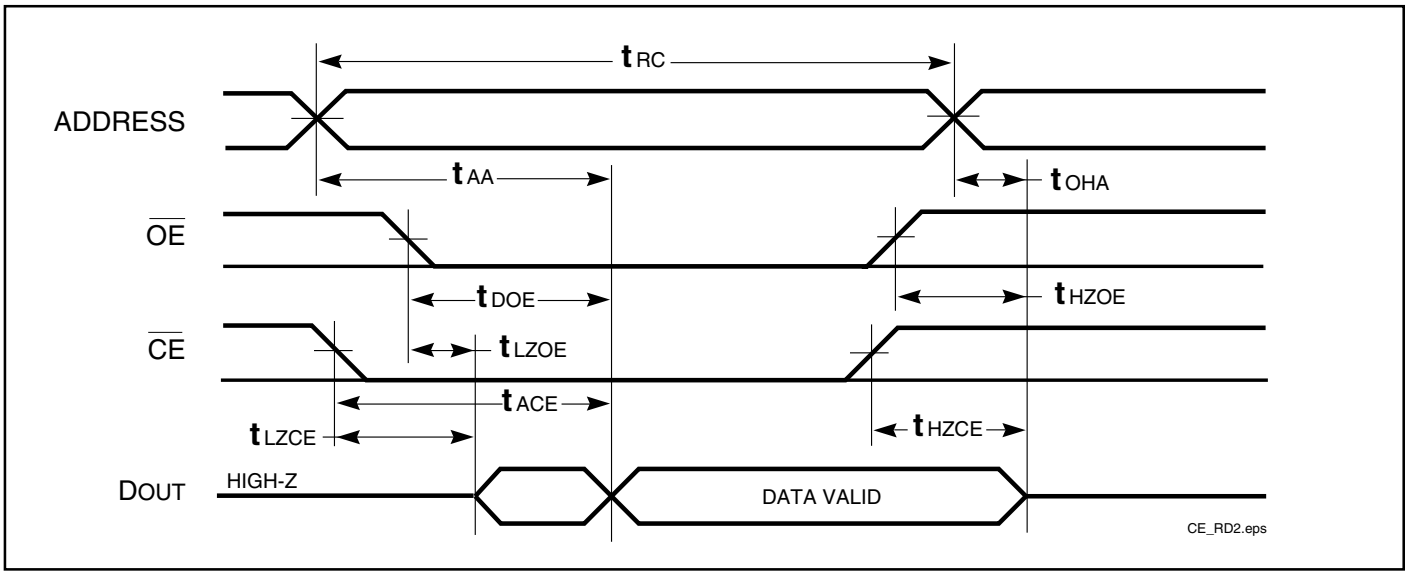
**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to $V_{DD}$-0.3V and output loading specified in Figure 1.
2. Tested with the loading specified in Figure 1. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

## AC WAVEFORMS

### READ CYCLE NO. 1[1,2]




### READ CYCLE NO. 2[1,3]




**Notes:**
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

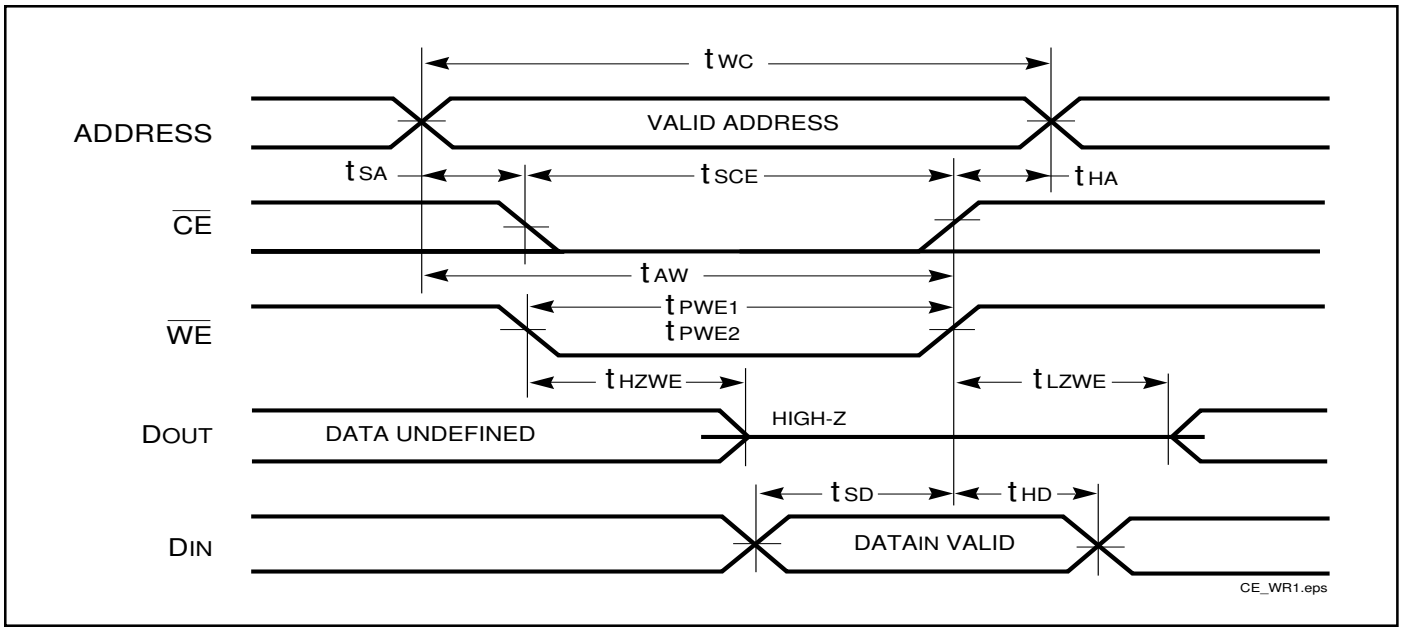
## WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

| Symbol | Parameter | -12 ns Min. | -12 ns Max. | -15 ns Min. | -15 ns Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | 12 | — | 15 | — | ns |
| $t_{SCE}$ | $\overline{CE}$ to Write End | 9 | — | 10 | — | ns |
| $t_{AW}$ | Address Setup Time to Write End | 9 | — | 10 | — | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | — | 0 | — | ns |
| $t_{SA}$ | Address Setup Time | 0 | — | 0 | — | ns |
| $t_{PWE_1}$[1] | $\overline{WE}$ Pulse Width ($\overline{OE}$ High) | 9 | — | 10 | — | ns |
| $t_{PWE_2}$[2] | $\overline{WE}$ Pulse Width ($\overline{OE}$ Low) | 11 | — | 12 | — | ns |
| $t_{SD}$ | Data Setup to Write End | 9 | — | 9 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | 0 | — | ns |
| $t_{HZWE}$[2] | $\overline{WE}$ LOW to High-Z Output | — | 6 | — | 7 | ns |
| $t_{LZWE}$[2] | $\overline{WE}$ HIGH to Low-Z Output | 3 | — | 3 | — | ns |

**Notes:**
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to $V_{DD}$-0.3V and output loading specified in Figure 1a.
2. Tested with the loading specified in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

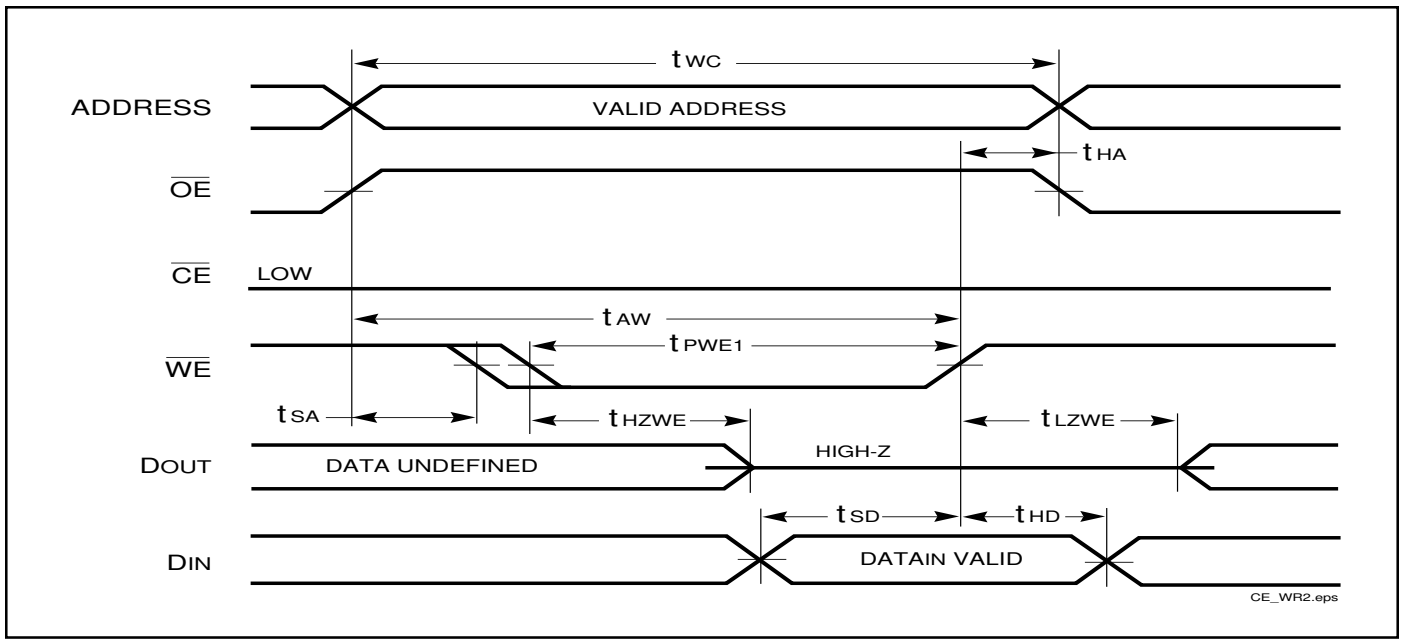
## AC WAVEFORMS

### WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

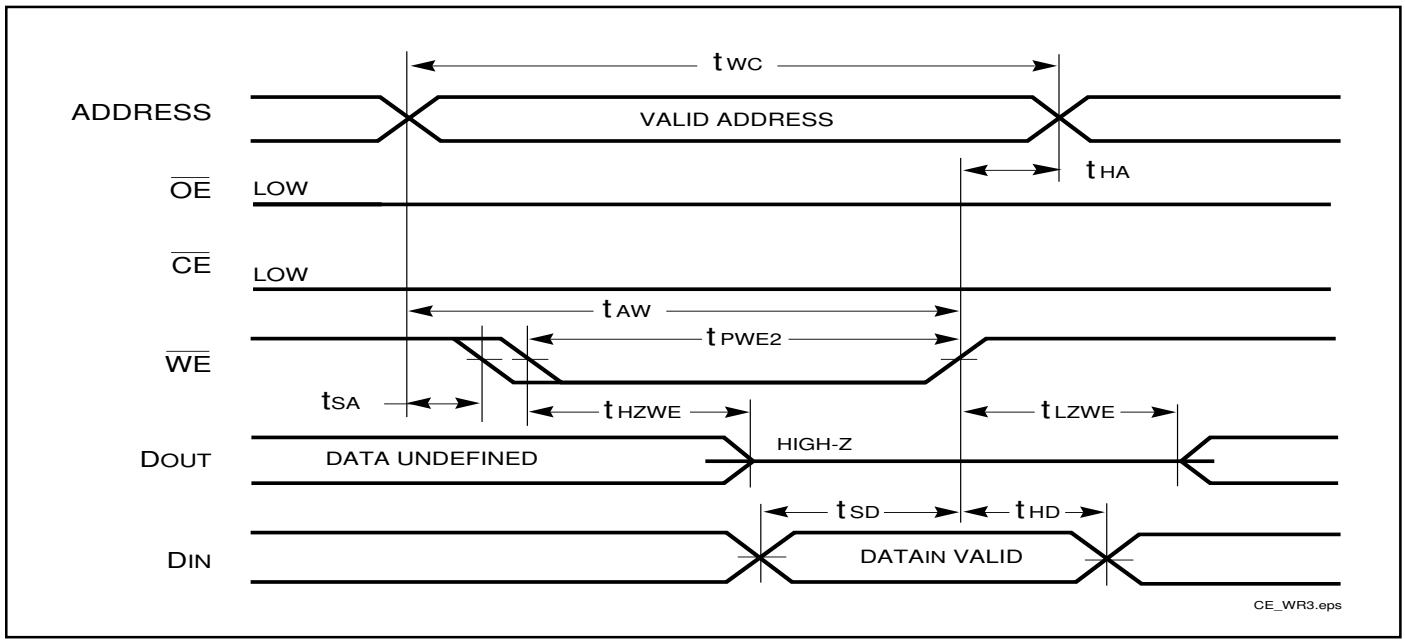


## AC WAVEFORMS

### WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)




### WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)




**Notes:**

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ > $V_{IH}$.

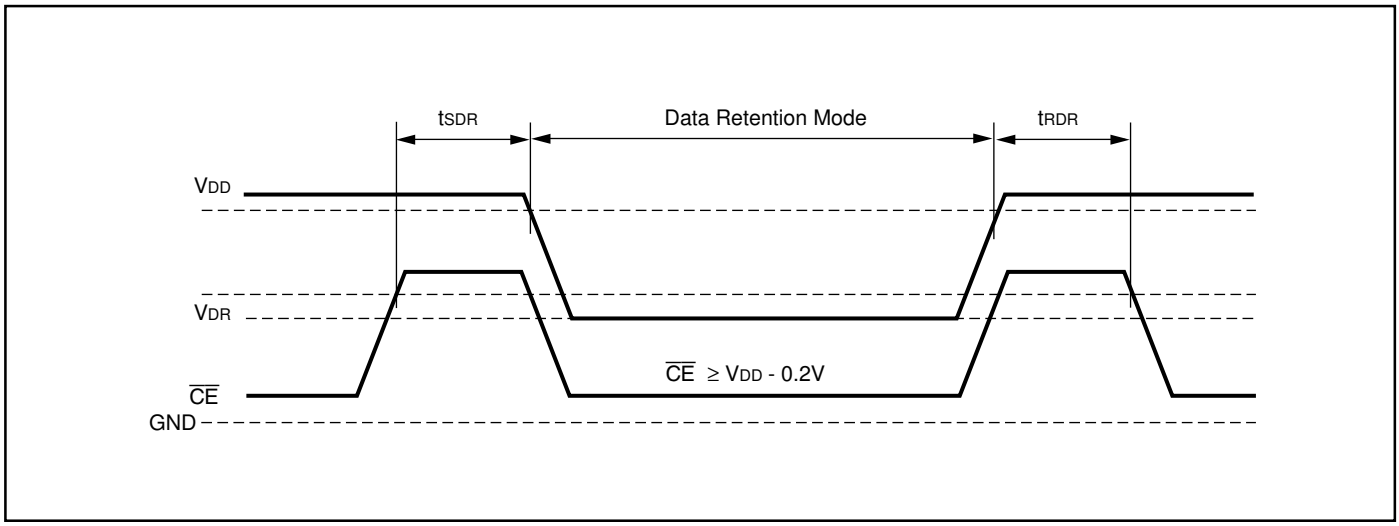
## DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Operations | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | | 1.8 | — | 3.6 | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$ = 1.8V, $\overline{CE} \geq V_{DD} - 0.2V$ | COM. | — | 6 | 20 | µA |
| | | | IND. | — | 6 | 50 | |
| | | | AUTO. | — | 6 | 75 | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | $t_{RC}$ | — | — | ns |

**Note**:

1. Typical values are measured at $V_{DD}$ = 2.5V, $T_A$ = 25°C. Not 100% tested.

## DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



## ORDERING INFORMATION

### Industrial Range: –40°C to +85°C

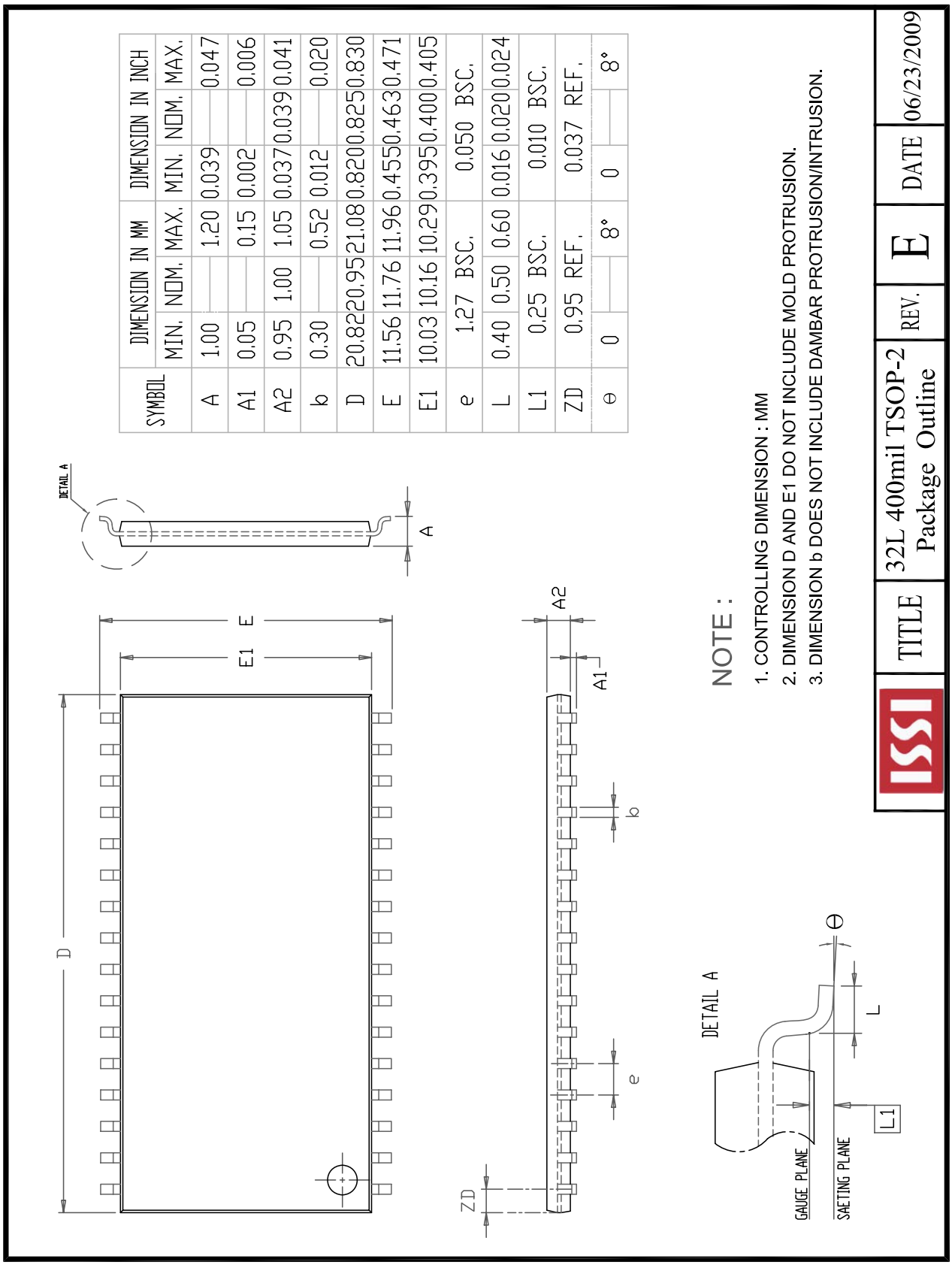
| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 12 | IS63WV1024BLL-12TI | 32-pin TSOP (Type II) |
| | IS63WV1024BLL-12TLI | 32-pin TSOP (Type II), Lead-free |
| | IS63WV1024BLL-12HI | sTSOP (Type I) (8mm x13.4mm) |
| | IS63WV1024BLL-12HLI | sTSOP (Type I) (8mm x13.4mm), Lead-free |
| | IS63WV1024BLL-12JLI | 32-pin SOJ (300-mil), Lead-free |
| | IS63WV1024BLL-12BI | mBGA(6mmx8mm) |
| | IS63WV1024BLL-12BLI | mBGA(6mmx8mm), Lead-free |

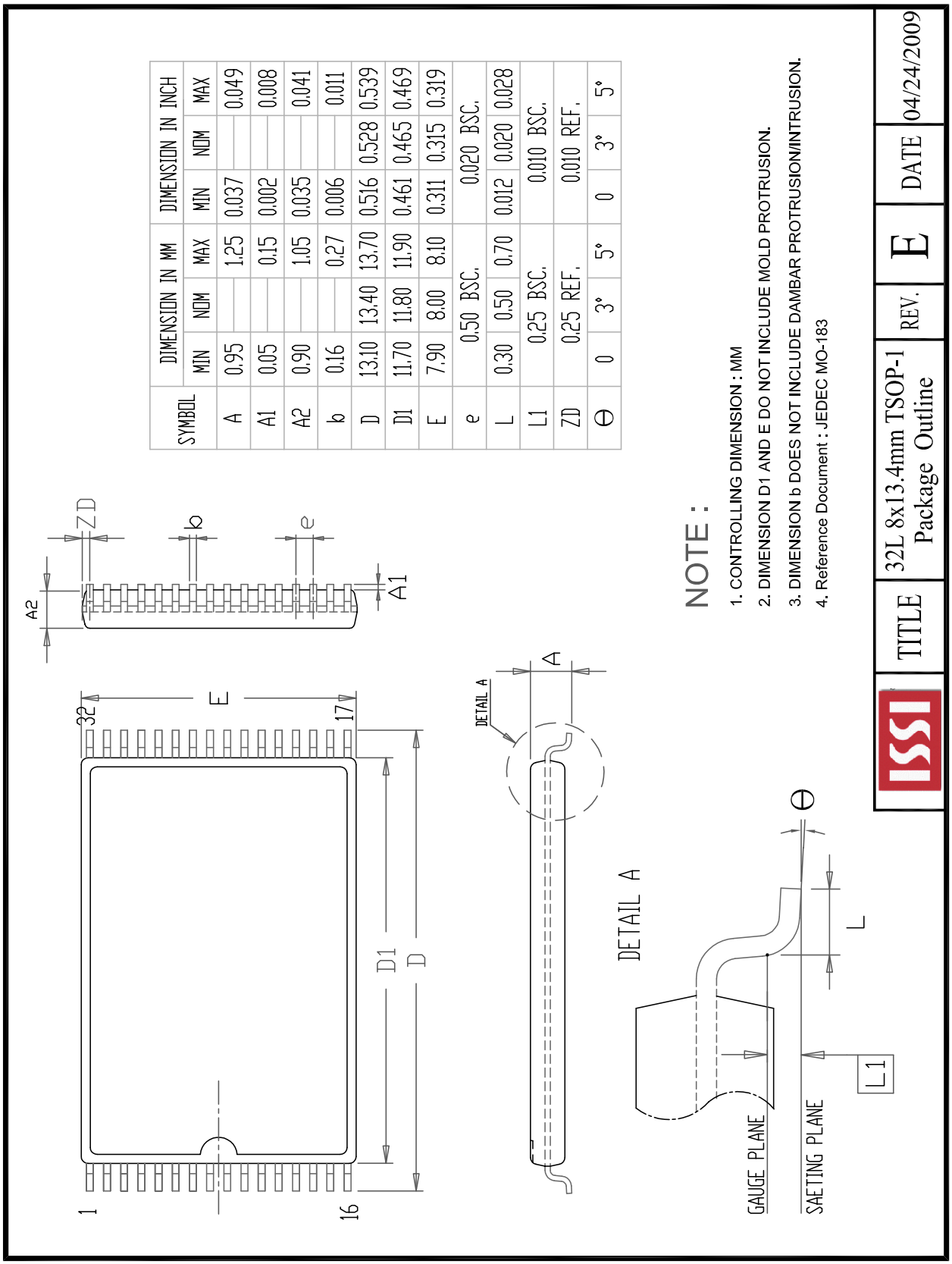
### Automotive Range (A3): –40°C to +85°C

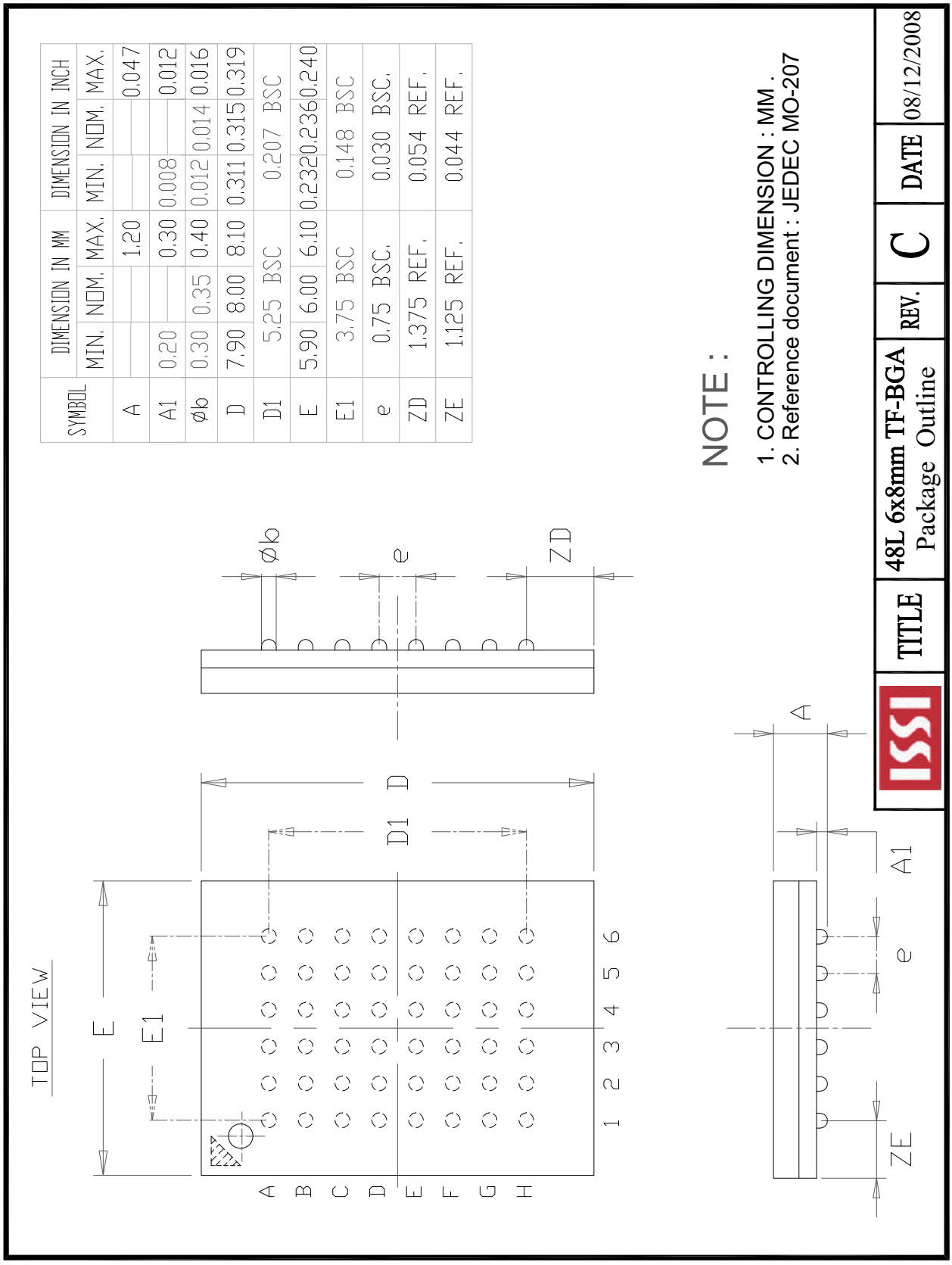
| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 15 (12*) | IS64WV1024BLL-15TA3 | 32-pin TSOP (Type II) |
| | IS64WV1024BLL-15TLA3 | 32-pin TSOP (Type II), Lead-free |
| | IS64WV1024BLL-15HA3 | sTSOP (Type I) (8mm x13.4mm) |
| | IS64WV1024BLL-15HLA3 | sTSOP (Type I) (8mm x13.4mm), Lead-free |
| | IS64WV1024BLL-15BA3 | mBGA(6mmx8mm) |
| | IS64WV1024BLL-15BLA3 | mBGA(6mmx8mm), Lead-free |

**Note:**
1. Speed = 12ns for $V_{DD}$ = 3.3V $\pm$ 10%. Speed = 15ns for $V_{DD}$ = 2.5V-3.6V.

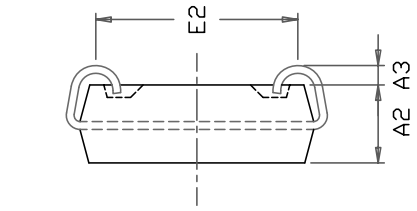
| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | — | 1.20 | 0.039 | — | 0.047 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | — | 0.52 | 0.012 | — | 0.020 |
| D | 20.82 | 20.95 | 21.08 | 0.820 | 0.825 | 0.830 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 1.27 BSC. | | | 0.050 BSC. | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.25 BSC. | | | 0.010 BSC. | | |
| ZD | 0.95 REF. | | | 0.037 REF. | | |
| θ | 0 | — | 8° | 0 | — | 8° |

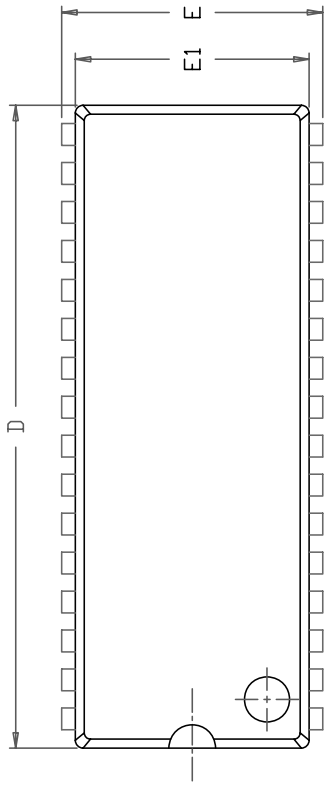


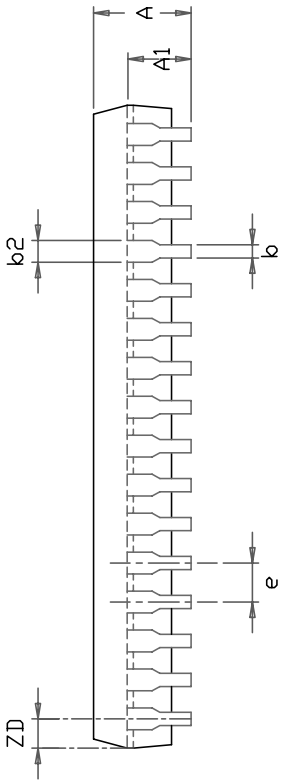

SYMBOL
DIMENSION IN MM
MIN
NOM
MAX
DIMENSION IN INCH
MIN
NOM
MAX
A 0.95 — 1.25 0.037 — 0.049
A1 0.05 — 0.15 0.002 — 0.008
A2 0.90 — 1.05 0.035 — 0.041
b 0.16 — 0.27 0.006 — 0.011
D 13.10 13.40 13.70 0.516 0.528 0.539
D1 11.70 11.80 11.90 0.461 0.465 0.469
E 7.90 8.00 8.10 0.311 0.315 0.319
e 0.50 BSC. 0.020 BSC.
L 0.30 0.50 0.70 0.012 0.020 0.028
L1 0.25 BSC. 0.010 BSC.
ZD 0.25 REF. 0.010 REF.
Θ 0 3° 5° 0 3° 5°
NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183
ISSI
TITLE
32L 8x13.4mm TSOP-1 Package Outline
REV.
E
DATE
04/24/2009
ZD
b
e
A2
A1
32
17
1
16
E
D1
D
DETAIL A
A
GAUGE PLANE
SEATING PLANE
L1
L
Θ


SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
øb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.2320.2360.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207
TOP VIEW
øb
e
ZD
D1
D
E
E1
A
A1
ZE
1 2 3 4 5 6
A B C D E F G H
TITLE
48L 6x8mm TF-BGA
Package Outline
REV.
C
DATE
08/12/2008

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 3.05 | — | 3.76 | 0.120 | — | 0.148 |
| A1 | 2.08 | — | 2.41 | 0.082 | — | 0.095 |
| A2 | 2.41 | 2.54 | 2.67 | 0.095 | 0.100 | 0.105 |
| A3 | 0.64 | — | 1.09 | 0.025 | — | 0.043 |
| b | 0.41 | — | 0.51 | 0.016 | — | 0.020 |
| b2 | 0.66 | — | 0.81 | 0.026 | — | 0.032 |
| D | 20.82 | — | 21.09 | 0.820 | — | 0.830 |
| E | 8.38 | 8.51 | 8.64 | 0.330 | 0.335 | 0.340 |
| E1 | 7.49 | 7.62 | 7.75 | 0.295 | 0.300 | 0.305 |
| E2 | 6.48 | — | 6.99 | 0.255 | — | 0.275 |
| e | 1.27 BSC. | | | 0.050 BSC. | | |
| ZD | 0.95 REF. | | | 0.037 REF. | | |




NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

| TITLE | 32L 300mil SOJ Package Outline | REV. | C | DATE | 08/14/2009 |
|---|---|---|---|---|---|

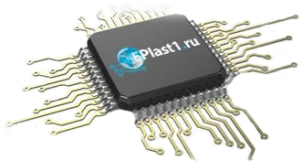
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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