International Rectifier

SMPS MOSFET

IRFIB5N65APbF

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	I_D
650V	0.93Ω	5.1A

Applications
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- High Voltage Isolation = 2.5KVRMS⑥
- Lead-Free

Benefits
- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current

TO-220 Full-Pak G D S

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	5.1	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	3.2	
I_{DM}	Pulsed Drain Current ①	21	
P_D @T_C = 25°C	Power Dissipation	60	W
	Linear Derating Factor	0.48	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	2.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Single Transistor Flyback
- Single Transistor Forward

Notes ① through ⑥are on page 8

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	650	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.67	–––	V/°C	Reference to 25°C, I_D = 1mA⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.93	Ω	V_{GS} = 10V, I_D = 3.1.A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–––	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	μA	V_{DS} = 650V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 520V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	3.9	–––	–––	S	V_{DS} = 50V, I_D = 3.1A
Q_g	Total Gate Charge	–––	–––	48	nC	I_D = 5.2A
Q_{gs}	Gate-to-Source Charge	–––	–––	12		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	19		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	–––	14	–––	ns	V_{DD} = 325V
t_r	Rise Time	–––	20	–––		I_D = 5.2A
$t_{d(off)}$	Turn-Off Delay Time	–––	34	–––		R_G = 9.1Ω
t_f	Fall Time	–––	18	–––		R_D = 62Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	–––	1417	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	177	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	7.0	–––		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	–––	1912	–––		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	–––	48	–––		V_{GS} = 0V, V_{DS} = 520V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	84	–––		V_{GS} = 0V, V_{DS} = 0V to 520V ⑤

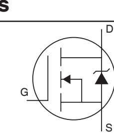
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	325	mJ
I_{AR}	Avalanche Current①	–––	5.2	A
E_{AR}	Repetitive Avalanche Energy①	–––	6	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	2.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	–––	65	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	5.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	21		
V_{SD}	Diode Forward Voltage	–––	–––	1.5	V	T_J = 25°C, I_S = 5.2A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	493	739	ns	T_J = 25°C, I_F = 5.2A
Q_{rr}	Reverse RecoveryCharge	–––	2.1	3.2	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

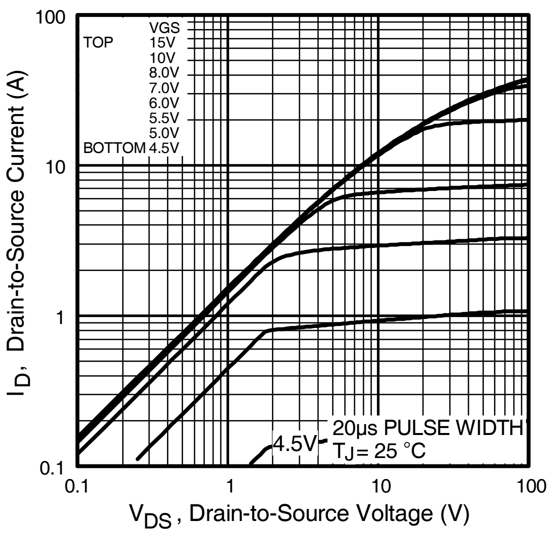


Fig 1. Typical Output Characteristics

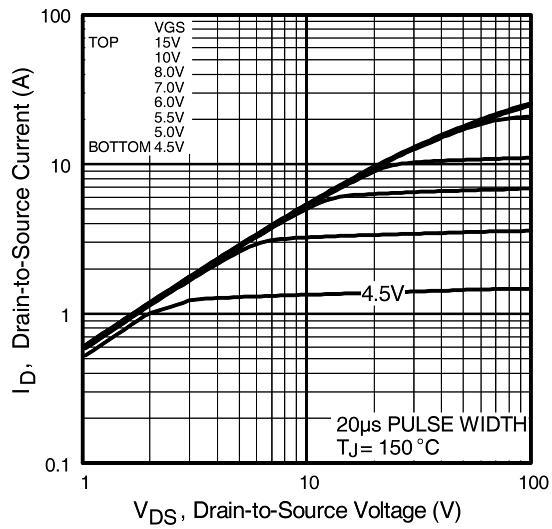


Fig 2. Typical Output Characteristics

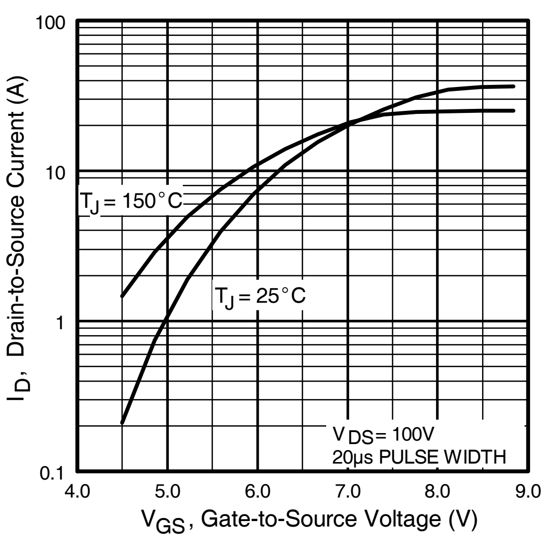


Fig 3. Typical Transfer Characteristics

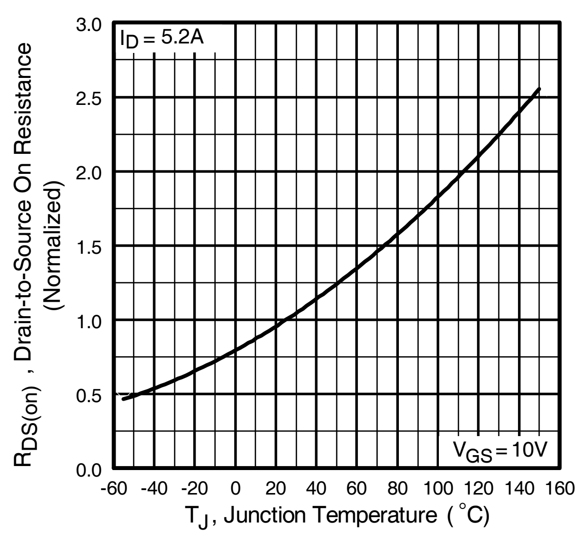


Fig 4. Normalized On-Resistance Vs. Temperature

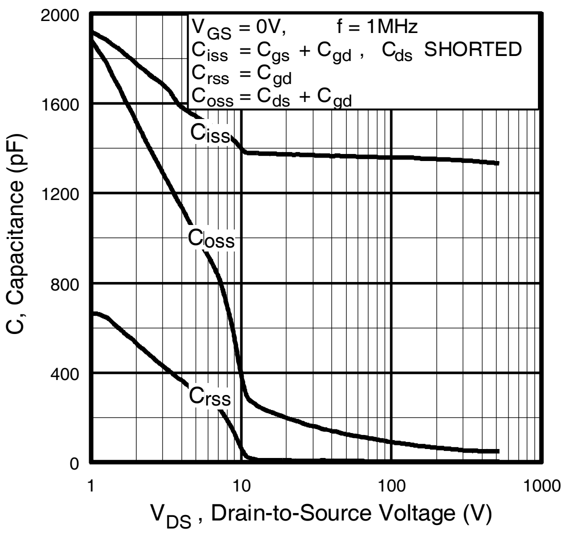


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

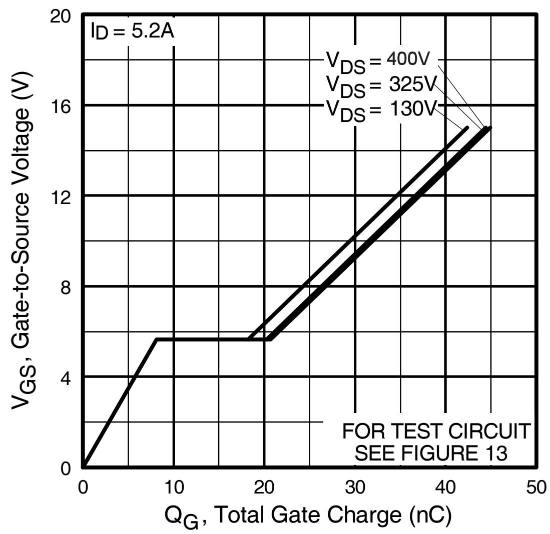


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

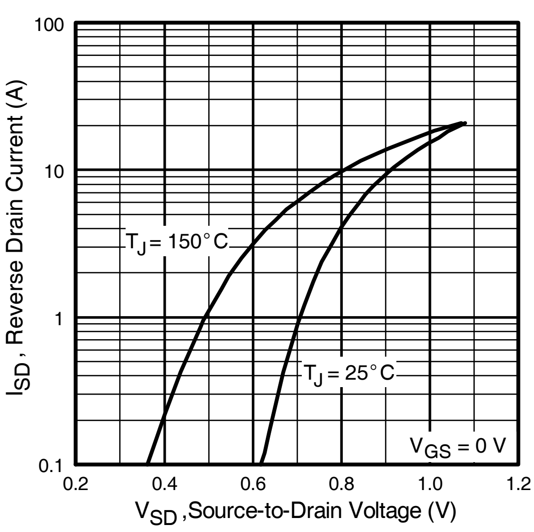


Fig 7. Typical Source-Drain Diode Forward Voltage

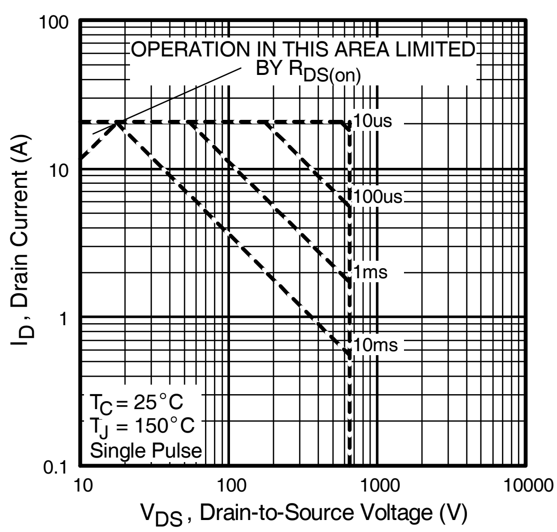


Fig 8. Maximum Safe Operating Area

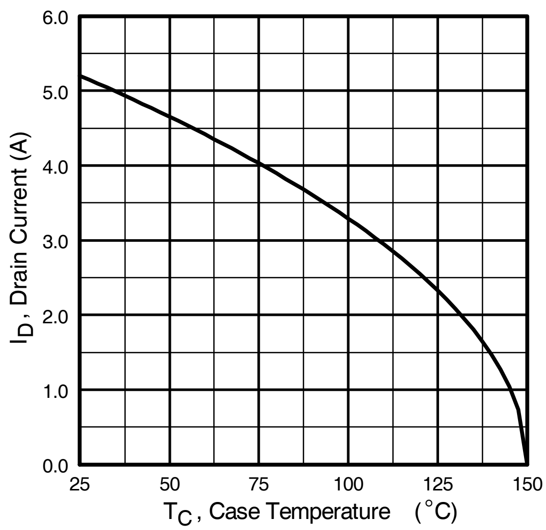


Fig 9. Maximum Drain Current Vs. Case Temperature

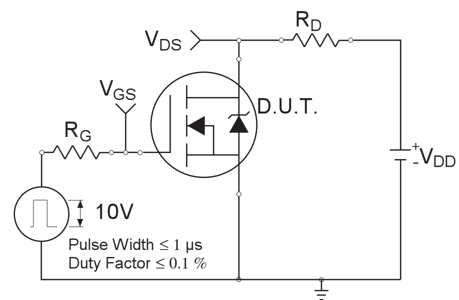


Fig 10a. Switching Time Test Circuit

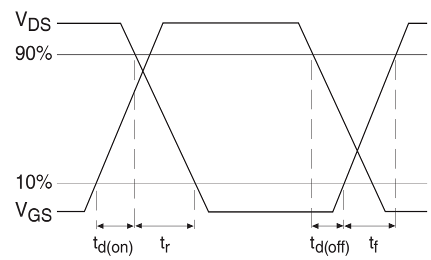


Fig 10b. Switching Time Waveforms

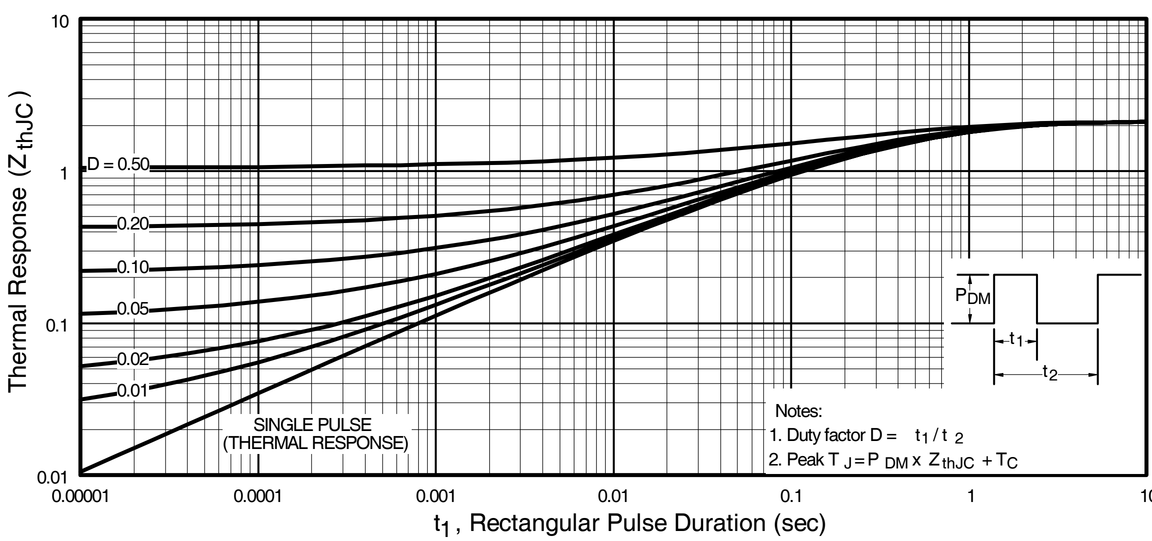


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

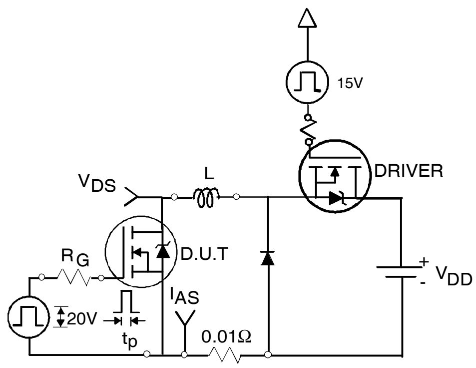


Fig 12a. Unclamped Inductive Test Circuit

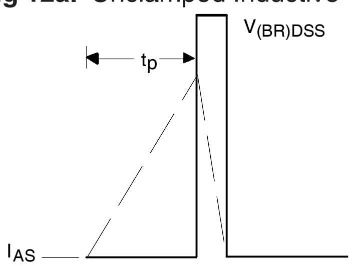


Fig 12b. Unclamped Inductive Waveforms

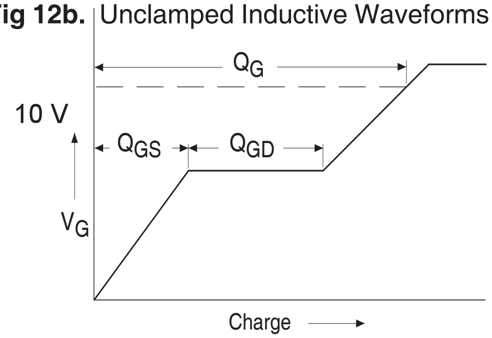


Fig 13a. Basic Gate Charge Waveform

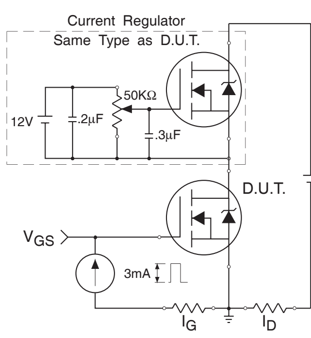


Fig 13b. Gate Charge Test Circuit

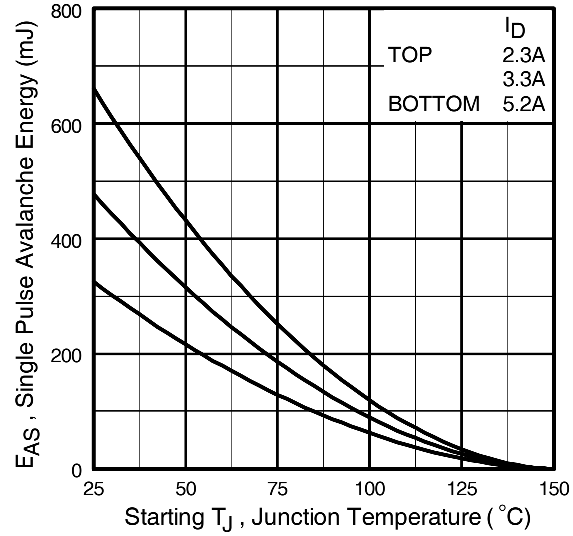


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

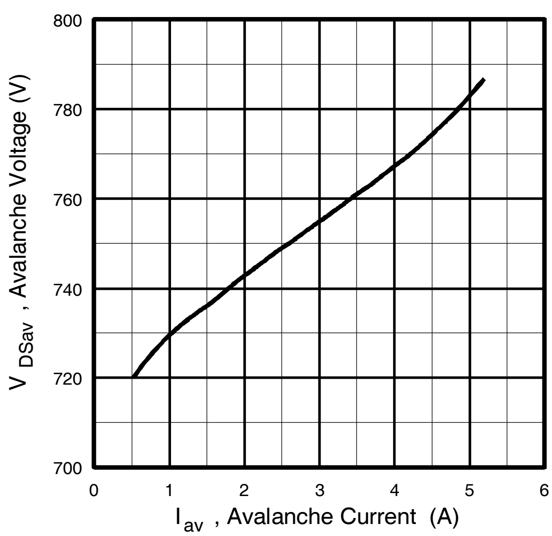
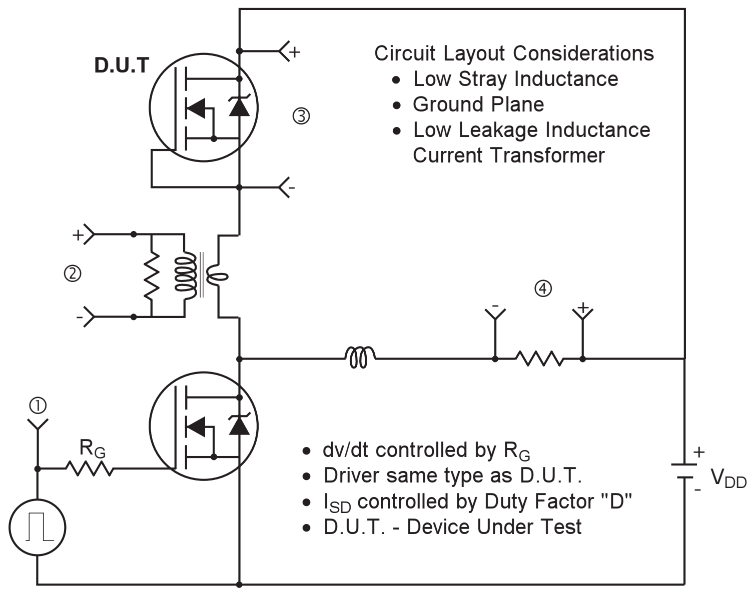
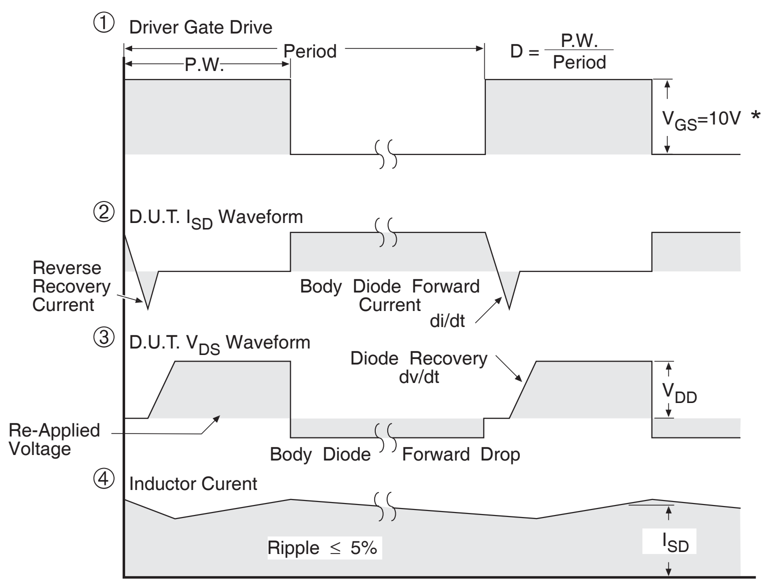


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



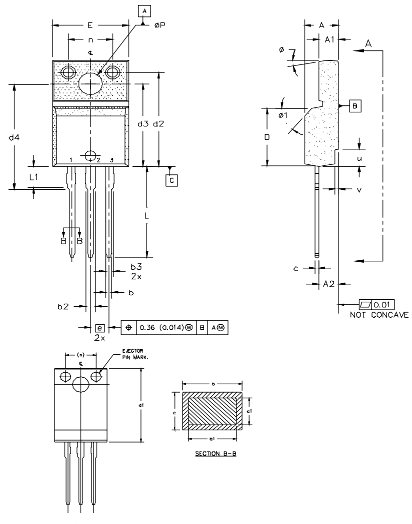


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.0 DIMENSION b1 APPLY TO BASE METAL ONLY
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN	MAX.	MIN	MAX.	
A	4.57	4.83	0.180	0.190	
A1	2.57	2.83	0.101	0.114	
A2	2.51	2.85	0.099	0.112	
b	0.622	0.89	0.024	0.035	
b1	0.622	0.838	0.024	0.033	5
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
c	0.440	0.629	0.017	0.025	
c1	0.440	0.584	0.017	0.023	
D	8.65	9.80	0.341	0.386	4
d1	15.80	16.12	0.622	0.635	
d2	13.97	14.22	0.550	0.560	
d3	12.30	12.92	0.484	0.509	
d4	8.64	9.91	0.340	0.390	
E	10.36	10.63	0.408	0.419	4
e	2.54 BSC		0.100 BSC		
L	13.20	13.73	0.520	0.541	
L1	3.10	3.50	0.122	0.138	3
n	6.05	6.15	0.238	0.242	
øP	3.05	3.45	0.120	0.136	
u	2.40	2.50	0.094	0.098	6
v	0.40	0.50	0.016	0.020	6
ø	3°	7°	3°	7°	
ø1		45°		45°	

LEAD ASSIGNMENTS

HEXFET

1 - GATE
2.- DRAIN
3.- SOURCE

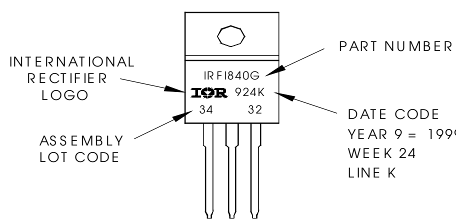
IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, L = 24mH $R_G = 25\Omega$, $I_{AS} = 5.2A$. (See Figure 12)

③ $I_{SD} \leq 5.2A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ t=60s, f=60Hz

Data and specifications subject to change without notice.

International
IOR Rectifier

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11/03

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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