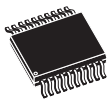
STM8L051F3

Value line, 8-bit ultralow power MCU, 8-KB Flash, 256-byte data EEPROM, RTC, timers, USART, I2C, SPI, ADC

Data brief – preliminary data

Features

- Operating conditions
  - Operating power supply: 1.8 V to 3.6 V
    Temperature range: –40 °C to 85 °C
- Low power features
  - 5 low power modes: Wait, Low power run, Low power wait, Active-halt with RTC, Halt
  - Ultralow leakage per I/0: 50 nA
  - Fast wakeup from Halt: 5 µs
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq: 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low power, ultrasafe BOR reset with 5 selectable thresholds
  - Ultra low power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1 to 16 MHz crystal oscillators
  - Internal 16 MHz factory-trimmed RC
  - Internal 38 kHz low consumption RC
  - Clock security system
- Low power RTC
  - BCD calendar with alarm interrupt
  - Digital calibration with +/- 0.5 ppm accuracy
  - LSE security system
  - Auto-wakeup from Halt w/ periodic interrupt
- Memories
  - 8 Kbytes of Flash program memory and 256 bytes of data EEPROM with ECC
  - Flexible write and read protection modes
  - 1 Kbyte of RAM



TSSOP20

- DMA
  - 4 channels supporting ADC, SPI, I2C, USART, timers
  - 1 channel for memory-to-memory
- 12-bit ADC up to 1 Msps/28 channels
  - Internal reference voltage
- Timers
  - Two 16-bit timers with 2 channels (used as IC, OC, PWM), quadrature encoder
  - One 8-bit timer with 7-bit prescaler
  - 2 watchdogs: 1 Window, 1 Independent
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - Synchronous serial interface (SPI)
  - Fast I^2C 400 kHz SMBus and PMBus
  - USART
- Up to 18 I/Os, all mappable on interrupt vectors
- Development support
  - Fast on-chip programming and non-intrusive debugging with SWIM
  - Bootloader using USART

Table 1. Device summary

Reference	Part number
STM8L051xx	STM8L051F3

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1 Introduction

This document describes the features, pinout, mechanical data and ordering information for the low density value line STM8L151F3 microcontroller with 8-Kbyte Flash memory density.

For more details on the whole STMicroelectronics ultra low power family please refer to *Section 2.2: Ultra low power continuum*.

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

Low density value line devices provide the following benefits:

- Integrated system
  - 8 Kbytes of low-density embedded Flash program memory
  - 256 bytes of data EEPROM
  - 1 Kbyte of RAM
  - Internal high-speed and low-power low speed RC
  - Embedded reset
- Ultra low power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Wide choice of development tools

These features make the value line STM8L05xxx ultra low power microcontroller family suitable for a wide range of consumer and mass market applications.

Refer to *Table 2: Low density value line STM8L05xxx low power device features and peripheral counts* and *Section 3: Functional overview* for an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the block diagram of the low density value line STM8L05xxx family.

2 Description

The low density value line STM8L05xxx devices are members of the STM8L ultra low power 8-bit family.

The STM8L ultra low power family features an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultra-fast Flash programming.

Low density value line STM8L05xxx microcontrollers feature embedded data EEPROM and low power, low-voltage, single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, a real-time clock, two 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as an SPI, an I^2C interface, and one USART.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

All STM8L ultra low power products are based on the same architecture with the same memory mapping and a coherent pinout.

2.1 Device overview

Table 2. Low density value line STM8L05xxx low power device features and peripheral counts

Features		STM8L051F3
Flash (Kbytes)		8
Data EEPROM (Bytes)		256
RAM (Kbytes)		1
Timers	Basic	1 (8-bit)
	General purpose	2 (16-bit)
Communication interfaces	SPI	1
	I2C	1
	USART	1
GPIOs		18 (1)
12-bit synchronized ADC (number of channels)		1 (10)
Others		RTC, window watchdog, independent watchdog, 16-MHz and 32-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator
CPU frequency		16 MHz
Operating voltage		1.8 to 3.6 V
Operating temperature		– 40 to +85 °C
Package		TSSOP20

1. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

2.2 Ultra low power continuum

The ultra low power value line STM8L05xxx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra low power strategy which also includes STM8L101xx and STM32L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm Ultralow leakage process.

Note: The STM8L051xx are pin-to-pin compatible with STM8L101xx devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra low power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L051xx and STM32L15xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripheral: ADC1
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L051xx and STM32L15xx devices use a common architecture:

- Same power supply range from 1.65 to 3.6 V
- Architecture optimized to reach ultra low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L051xx and STM32L15xx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

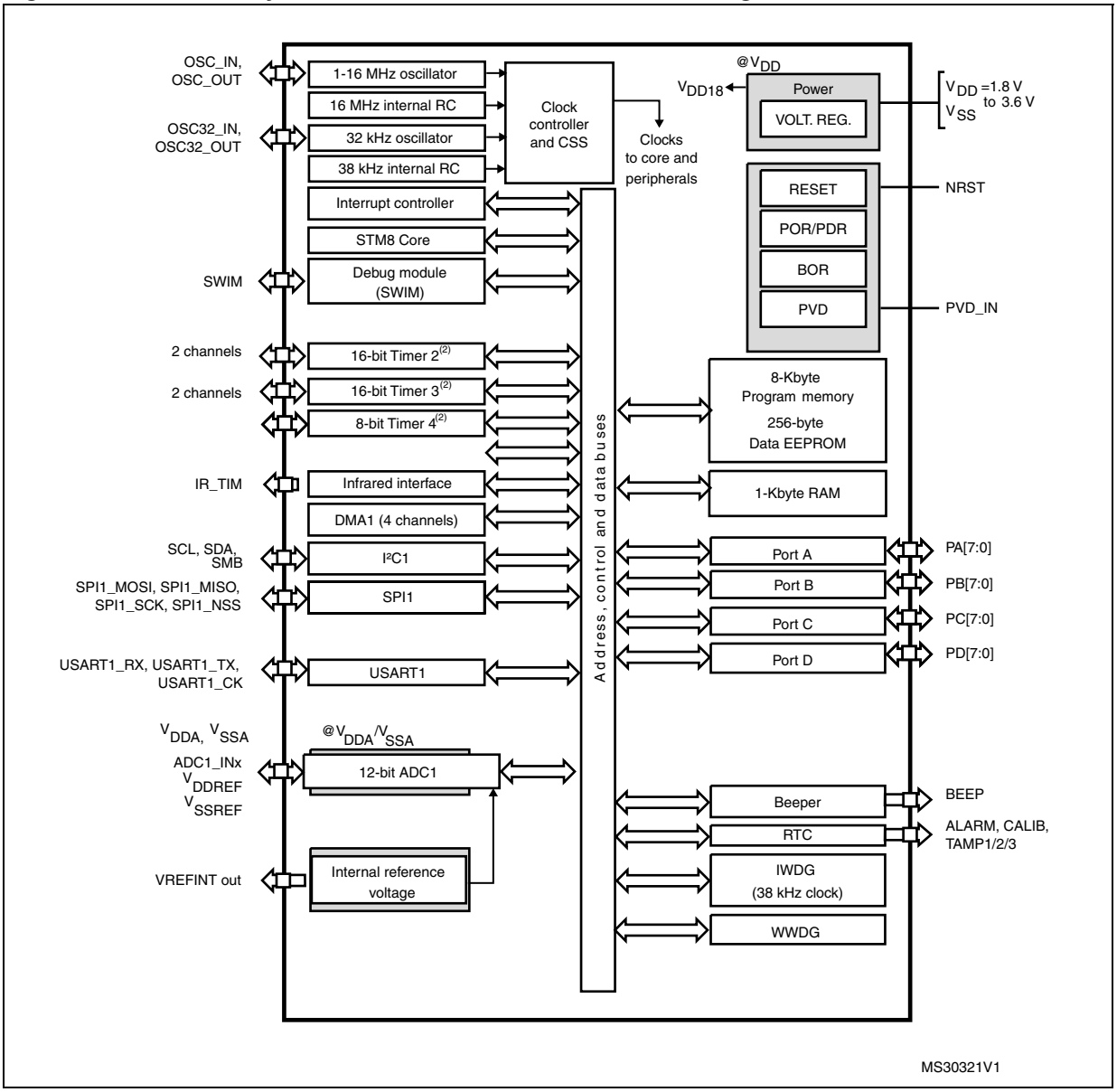
Features

ST ultra low power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

3 Functional overview

Figure 1. Low density value line STM8L05xxx device block diagram



1. **Legend**:
ADC: Analog-to-digital converter
BOR: Brownout reset
DMA: Direct memory access
I²C: Inter-integrated circuit multimaster interface
IWDG: Independent watchdog
POR/PDR: Power-on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low power modes

The low density value line STM8L05xxx devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra low power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1) and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64-Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The low density value line STM8L05xxx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 17 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.8 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1} ; V_{DD1} = 1.8 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1}.
- V_{SSA}; V_{DDA} = 1.8 to 3.6 V: external power supplies for analog peripherals. V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{SS2} ; V_{DD2} = 1.8 to 3.6 V: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{REF+}, V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. When the microcontroller operates between 1.8 and 3.6 V, BOR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The low density value line STM8L05xxx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

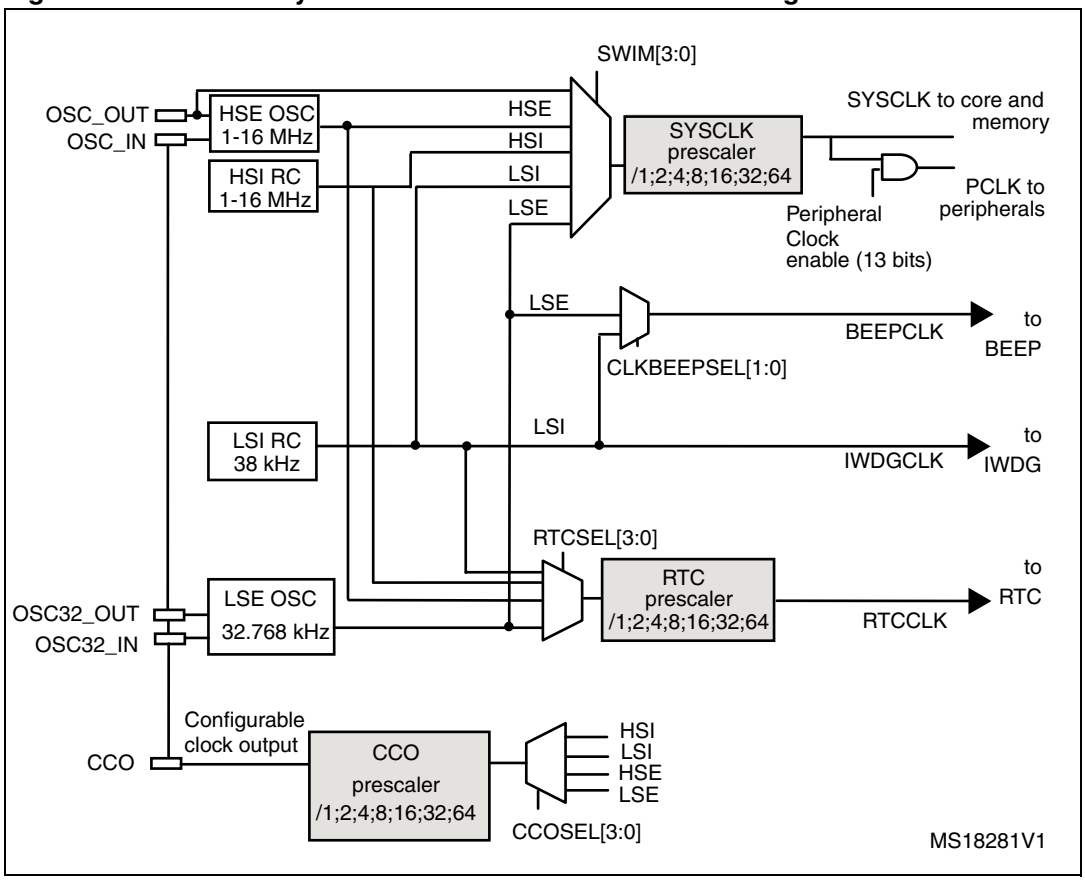
3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** four different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC clock sources:** the above four sources can be chosen to clock the RTC whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, it is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. Low density value line STM8L05xxx clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to Section HSE clock in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to Section LSE clock in the STM8L15x and STM8L16x reference manual (RM0031).

3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

3.6 Memories

The low density value line STM8L05xxx devices have the following main features:

- Up to 1 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - 8 Kbytes of low-density embedded Flash program memory
  - 256 bytes of Data EEPROM
  - Option bytes

The EEPROM embeds the error correction code (ECC) feature.

The option byte protects part of the Flash program memory from write and readout piracy.

3.7 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, I2C1, SPI1, USART1, and the three timers.

3.8 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 10 channels (including 1 fast channel) and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.9 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface controls the routing of internal analog signals to ADC1 and the internal reference voltage V_{REFINT}.

3.10 Timers

Low density value line STM8L05xxx devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	up/down	Any power of 2 from 1 to 128	Yes	2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.10.1 16-bit general purpose timers (TIM2, TIM3)

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.10.2 8-bit basic timer (TIM4)

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.11 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.11.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.11.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.12 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.13 Communication interfaces

3.13.1 SPI

The serial peripheral interfaces (SPI1) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.13.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.13.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

3.14 Infrared (IR) interface

The low density STM8L05xxx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.15 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

The low density value line STM8L05xxx ultra low power devices feature a built-in bootloader (see *UM0560: STM8 bootloader user manual*).

The bootloader is used to download application software into the device memories, including RAM, program and data memory, using standard serial interfaces. It is a complementary solution to programming via the SWIM debugging interface.

4 Pin description

Figure 3. STM8L051Fx 20-pin TSSOP20 package pinout

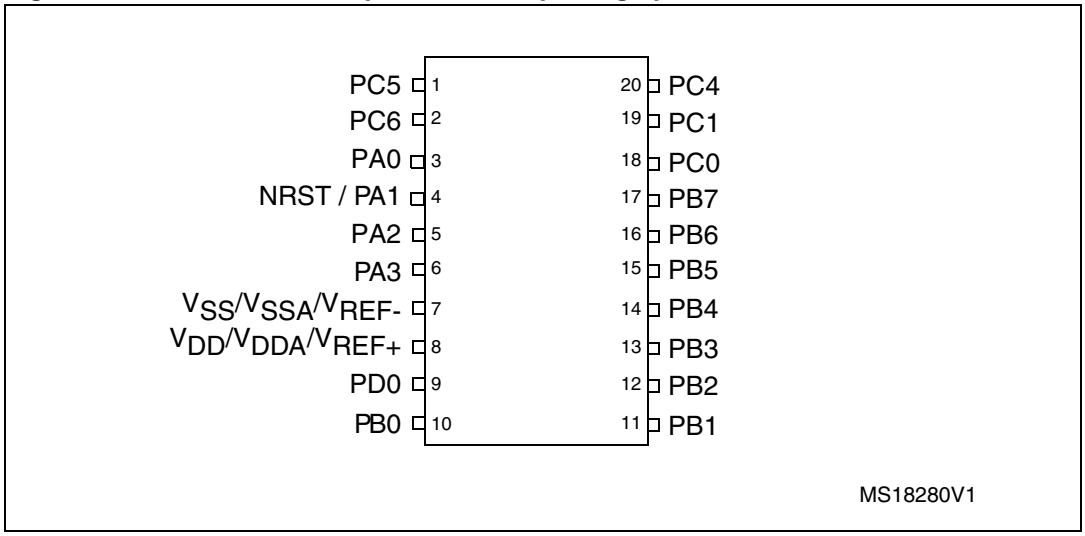


Table 4. Low density value line STM8L05xxx pin description

pin n°	Pin name	Type	Input			Output			Main function (after reset)	Default alternate function
TSSOP20			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
4	NRST/PA1(1)	I/O		**X**		HS		X	**Reset**	PA1
5	PA2/OSC_IN/*[USART_TX](2)/ [SPI_MISO]* (2)	I/O	**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART transmit] / [SPI master in- slave out]*
6	PA3/OSC_OUT/*[USART_RX](2)/[SPI_MOSI]*(2)	I/O	**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART receive]/ [SPI master out/slave in]/*
10	PB0(3)/TIM2_CH1/ADC1_IN18	I/O	**X**	X	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / ADC1_IN18
11	PB1/TIM3_CH1/ADC1_IN17	I/O	**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / ADC1_IN17
12	PB2/ TIM2_CH2/ ADC1_IN16	I/O	**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 ADC1_IN16
13	PB3/TIM2_ETR/ ADC1_IN15/RTC_ALARM	I/O	**X**	X	X	HS	X	X	**Port B3**	Timer 2 - external trigger / ADC1_IN15 / RTC_ALARM
14	PB4(3)/SPI1_NSS/ADC1_IN14	I/O	**X**	X	X	HS	X	X	**Port B4**	SPI master/slave select / ADC1_IN14
15	PB5/SPI_SCK/ /ADC1_IN13	I/O	**X**	X	X	HS	X	X	**Port B5**	[SPI clock] / ADC1_IN13
16	PB6/SPI1_MOSI/ ADC1_IN12	I/O	**X**	X	X	HS	X	X	**Port B6**	SPI master out/ slave in / ADC1_IN12

Table 4. Low density value line STM8L05xxx pin description (continued)

pin n°	Pin name	Type	Input			Output			Main function (after reset)	Default alternate function
TSSOP20			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
17	PB7/SPI1_MISO/ADC1_IN11	I/O	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ ADC1_IN11
18	PC0/I2C_SDA	I/O	**X**		X		T(4)		**Port C0**	I2C data
19	PC1/I2C_SCL	I/O	**X**		X		T(3)		**Port C1**	I2C clock
20	PC4/USART_CK]/ I2C_SMB/CCO/ADC1_IN4	I/O	**X**	X	X	HS	X	X	**Port C4**	USART synchronous clock / I2C1_SMB / Configurable clock output / ADC1_IN4
1	PC5/OSC32_IN /*[SPI1_NSS]*(2)/ *[USART_TX]*(2)/TIM2_CH1	I/O	**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI master/slave select] / [USART transmit]/Timer 2 -channel 1*
2	PC6/OSC32_OUT/*[SPI_SCK]*(2)/*[USART_RX]*(2)/TIM2_CH2	I/O	**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output */ [SPI clock] / [USART receive]/ Timer 2 -channel 2*
9	PD0/TIM3_CH2/*[ADC1_TRIG]*(2)/ ADC1_IN22	I/O	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22
8	V_{DD} / V_{DDA} / V_{REF+}	S							Digital supply voltage / ADC1 positive voltage reference	
7	V_{SS} / V_{REF-} / V_{SSA}								Ground voltage / ADC1 negative voltage reference / Analog ground voltage	
3	PA0(5)/*[USART_CK]*(2)/ SWIM/BEEP/IR_TIM (6)	I/O	X	**X**	X	HS (6)	X	X	**Port A0**	*[USART1 synchronous clock]*(2) / SWIM input and output / Beep output / Infrared Timer output

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High Sink LED driver capability available on PA0.

Note: The slope control of all GPIO pins, except true open drain pins, can be programmed. By default, the slope control is limited to 2 MHz.

4.1 System configuration options

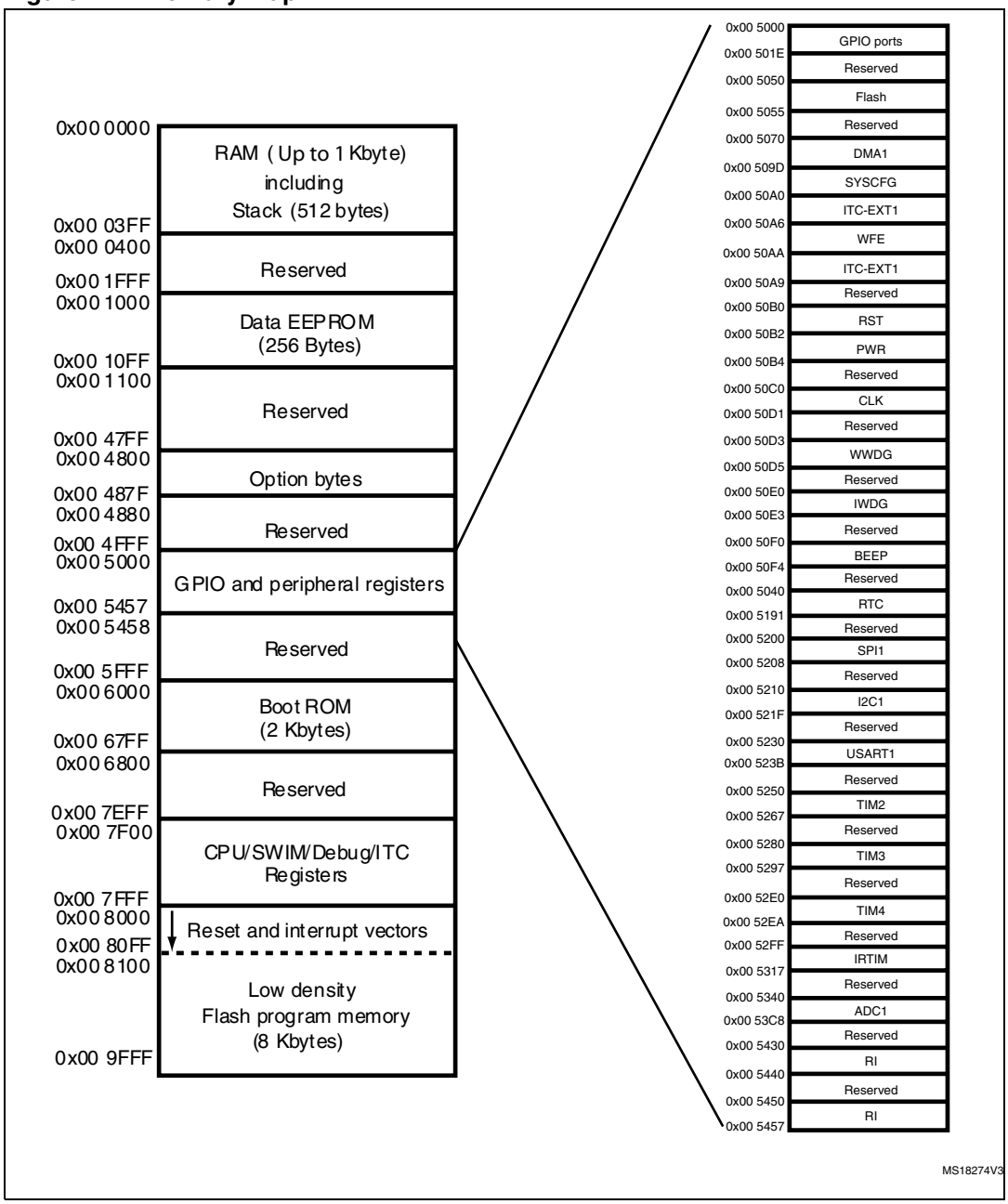
As shown in *Table 4: Low density value line STM8L05xxx pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the " Routing interface (RI) and system configuration controller" section in the STM8L15xx and STM8L16xx reference manual (RM0031).

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 4*.

Figure 4. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1 Kbyte	0x00 0000	0x00 03FF
Flash program memory	8 Kbytes	0x00 8000	0x00 9FFF

5.2 Register map

Table 6. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014 to 0x00 501D	Reserved area (0 bytes)			

Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (44 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5055 to 0x00 506F	Reserved area (27 bytes)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 507D to 0x00 507E	DMA1	Reserved area (2 bytes)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00
0x00 5084		Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5098	DMA1	DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C		Reserved area (3 bytes)		
0x00 509D	SYSCFG	SYSCFG_RMPCR3	Remapping register 3	0x00
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9		WFE_CR4	WFE control register 4	0x00
0x00 50AA	ITC - EXTI	EXTI_CR4	External interrupt control register 4	0x00
0x00 50AB		EXTI_CONF2	External interrupt port select register 2	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_CKDIVR	CLK Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	CLK Clock RTC register	0x00(1)
0x00 50C2		CLK_ICKCR	CLK Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	CLK Peripheral clock gating register 1	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C4	CLK	CLK_PCKENR2	CLK Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	CLK Configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	CLK External clock control register	0x00
0x00 50C7		CLK_SCSR	CLK System clock status register	0x01
0x00 50C8		CLK_SWR	CLK System clock switch register	0x01
0x00 50C9		CLK_SWCR	CLK Clock switch control register	0xX0
0x00 50CA		CLK_CSSR	CLK Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	CLK Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	CLK HSI calibration register	0xXX
0x00 50CD		CLK_HSITRIMR	CLK HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	CLK HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	CLK Main regulator control status register	0bxx11 1 00X
0x00 50D0		CLK_PCKENR3	CLK Peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0x01
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to0x00 513F	Reserved area (76 bytes)			
0x00 5140	RTC	RTC_TR1	RTC Time register 1	0x00
0x00 5141		RTC_TR2	RTC Time register 2	0x00
0x00 5142		RTC_TR3	RTC Time register 3	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5143	RTC	Reserved area (1 byte)		
0x00 5144		RTC_DR1	RTC Date register 1	0x01
0x00 5145		RTC_DR2	RTC Date register 2	0x21
0x00 5146		RTC_DR3	RTC Date register 3	0x00
0x00 5147		Reserved area (1 byte)		
0x00 5148		RTC_CR1	RTC Control register 1	0x00(1)
0x00 5149		RTC_CR2	RTC Control register 2	0x00(1)
0x00 514A		RTC_CR3	RTC Control register 3	0x00(1)
0x00 514B		Reserved area (1 byte)		
0x00 514C		RTC_ISR1	RTC Initialization and status register 1	0x01
0x00 514D		RTC_ISR2	RTC Initialization and Status register 2	0x00
0x00 514E 0x00 514F		Reserved area (2 bytes)		
0x00 5150		RTC_SPRERH	RTC Synchronous prescaler register high	0x00(1)
0x00 5151		RTC_SPRERL	RTC Synchronous prescaler register low	0xFF(1)
0x00 5152		RTC_APRER	RTC Asynchronous prescaler register	0x7F(1)
0x00 5153		Reserved area (1 byte)		
0x00 5154		RTC_WUTRH	RTC Wakeup timer register high	0xFF(1)
0x00 5155		RTC_WUTRL	RTC Wakeup timer register low	0xFF(1)
0x00 5156		Reserved area (1 byte)		
0x00 5157		RTC_SSRL	RTC Subsecond register low	0x00
0x00 5158		RTC_SSRH	RTC Subsecond register high	0x00
0x00 5159		RTC_WPR	RTC Write protection register	0x00
0x00 5158		RTC_SSRH	RTC Subsecond register high	0x00
0x00 5159		RTC_WPR	RTC Write protection register	0x00
0x00 515A		RTC_SHIFTRH	RTC Shift register high	0x00
0x00 515B		RTC_SHIFTRL	RTC Shift register low	0x00
0x00 515C		RTC_ALRMAR1	RTC Alarm A register 1	0x00(1)
0x00 515D		RTC_ALRMAR2	RTC Alarm A register 2	0x00(1)
0x00 515E		RTC_ALRMAR3	RTC Alarm A register 3	0x00(1)
0x00 515F		RTC_ALRMAR4	RTC Alarm A register 4	0x00(1)
0x00 5160 to 0x00 5163		Reserved area (4 bytes)		
0x00 5164		RTC_ALRMASSRH	RTC Alarm A subsecond register high	0x00(1)
0x00 5165		RTC_ALRMASSRL	RTC Alarm A subsecond register low	0x00(1)

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5166	RTC	RTC_ALRMASSMSKR	RTC Alarm A masking register	0x00(1)
0x00 5167 to 0x00 5169		Reserved area (3 bytes)		
0x00 516A		RTC_CALRH	RTC Calibration register high	0x00(1)
0x00 516B		RTC_CALRL	RTC Calibration register low	0x00(1)
0x00 516C		RTC_TCR1	RTC Tamper control register 1	0x00(1)
0x00 516D		RTC_TCR2	RTC Tamper control register 2	0x00(1)
0x00 516E to 0x00 518A		Reserved area (36 bytes)		
0x00 5190		CSSLSE_CSR	CSS on LSE control and status register	0x00(1)
0x00 519A to 0x00 51FF	Reserved area (111 bytes)			
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OAR2	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0X
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 521D	I2C1	I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 bytes)			
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	0xXX
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 Slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_DER	TIM2 DMA1 request enable register	0x00
0x00 5255		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5256		TIM2_SR1	TIM2 status register 1	0x00
0x00 5257		TIM2_SR2	TIM2 status register 2	0x00
0x00 5258		TIM2_EGR	TIM2 event generation register	0x00
0x00 5259		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 525A		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525B		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525F		TIM2_ARRH	TIM2 auto-reload register high	0xFF

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5260	TIM2	TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5261		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5262		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5263		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5264		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5265		TIM2_BKR	TIM2 break register	0x00
0x00 5266		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5267 to 0x00 527F	Reserved area (25 bytes)			
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52DF	Reserved area (72 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5317 to 0x00 533F	Reserved area (41 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 542F	Reserved area(104 bytes)			
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	RI Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	RI Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	RI I/O input register 1	0xXX
0x00 5434		RI_IOIR2	RI I/O input register 2	0xXX
0x00 5435		RI_IOIR3	RI I/O input register 3	0xXX
0x00 5436		RI_IOCMR1	RI I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	RI I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	RI I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	RI I/O switch register 1	0x00
0x00 543A		RI_IOSR2	RI I/O switch register 2	0x00
0x00 543B		RI_IOSR3	RI I/O switch register 3	0x00
0x00 543C		RI_IOGCR	RI I/O group control register	0xFF
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	RI Analog switch register 2	0x00
0x00 543F		RI_RCR	RI Resistor control register	0x00
0x00 5440 to 0x00 544F	Reserved area (16 bytes)			
0x00 5450	RI	RI_CR	RI I/O control register	0x00
0x00 5451		RI_MASKR1	RI I/O mask register 1	0x00
0x00 5452		RI_MASKR2	RI I/O mask register 2	0x00
0x00 5453		RI_MASKR3	RI I/O mask register 3	0x00
0x00 5454		RI_MASKR4	RI I/O mask register 4	0x00
0x00 5455		RI_IOIR4	RI I/O input register 4	0xXX
0x00 5456		RI_IOCMR4	RI I/O control mode register 4	0x00
0x00 5457		RI_IOSR4	RI I/O switch register 4	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

Table 8. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	CPU	Reserved area (85 bytes)		
0x00 7F60		CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC-SPR	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00

Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F97	DM	DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only

6 Interrupt vector mapping

Table 9. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	TLI(2)	External Top level Interrupt	-	-	-	-	0x00 8008
1	FLASH	FLASH end of programing/ write attempted to protected page interrupt	-	-	Yes	Yes	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8014
4	RTC	RTC alarm A/wakeup/ tamper 1/tamper 2/tamper 3	Yes	Yes	Yes	Yes	0x00 8018
5	PVD	PVD interrupt	Yes	Yes	Yes	Yes	0x00 801C
6	EXTIB	External interrupt port B	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID	External interrupt port D	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	Reserved						0x00 8048
17	CLK	CLK system clock switch/CSS interrupt	-	-	Yes	Yes	0x00 804C
18	ADC1	ACD1 end of conversion/ analog watchdog/ overrun interrupt	Yes	Yes	Yes	Yes	0x00 8050
19	TIM2	TIM2 update /overflow/trigger/break interrupt	-	-	Yes	Yes	0x00 8054

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
20	TIM2	TIM2 Capture/Compare interrupt	-	-	Yes	Yes	0x00 8058
21	TIM3	TIM3 Update /Overflow/Trigger/Break interrupt	-	-	Yes	Yes	0x00 805C
22	TIM3	TIM3 Capture/Compare interrupt	-	-	Yes	Yes	0x00 8060
23	RI	RI trigger interrupt	-	-	Yes	-	0x00 8064
24	Reserved						0x00 8068
25	TIM4	TIM4 update/overflow/ trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI1	SPI1 TX buffer empty/ RX buffer not empty/ error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART 1	USART1 transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART 1	USART1 received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I^2C1	I^2C1 interrupt(3)	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. The TLI interrupt is the logic OR between TIM2 overflow interrupt, and TIM4 overflow interrupts.
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

7 Package characteristics

7.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.2 Package mechanical data

7.2.1 20-lead thin shrink small package (TSSOP20)

Figure 5. TSSOP20 20-lead thin shrink small package outline

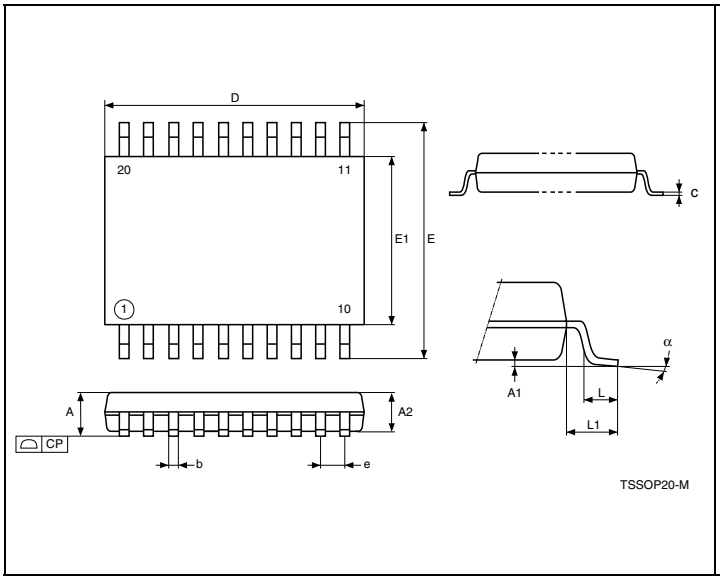
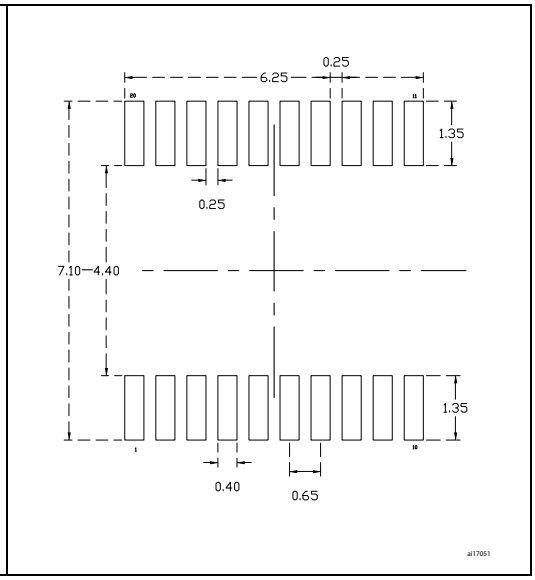


Figure 6. TSSOP20 recommended footprint



1. Drawing is not to scale
2. Dimensions are in millimeters

Table 10. TSSOP20 20-lead thin shrink small package, mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.0472
A1	0.05		0.15	0.0020		0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19		0.3	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.2520	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1	4.3	4.4	4.5	0.1693	0.1732	0.1772
e	-	0.65	-		0.0256	-
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2.2 32-pin Low profile quad flat package (LQFP32)

Figure 7. LQFP32 32-pin low profile quad flat package outline

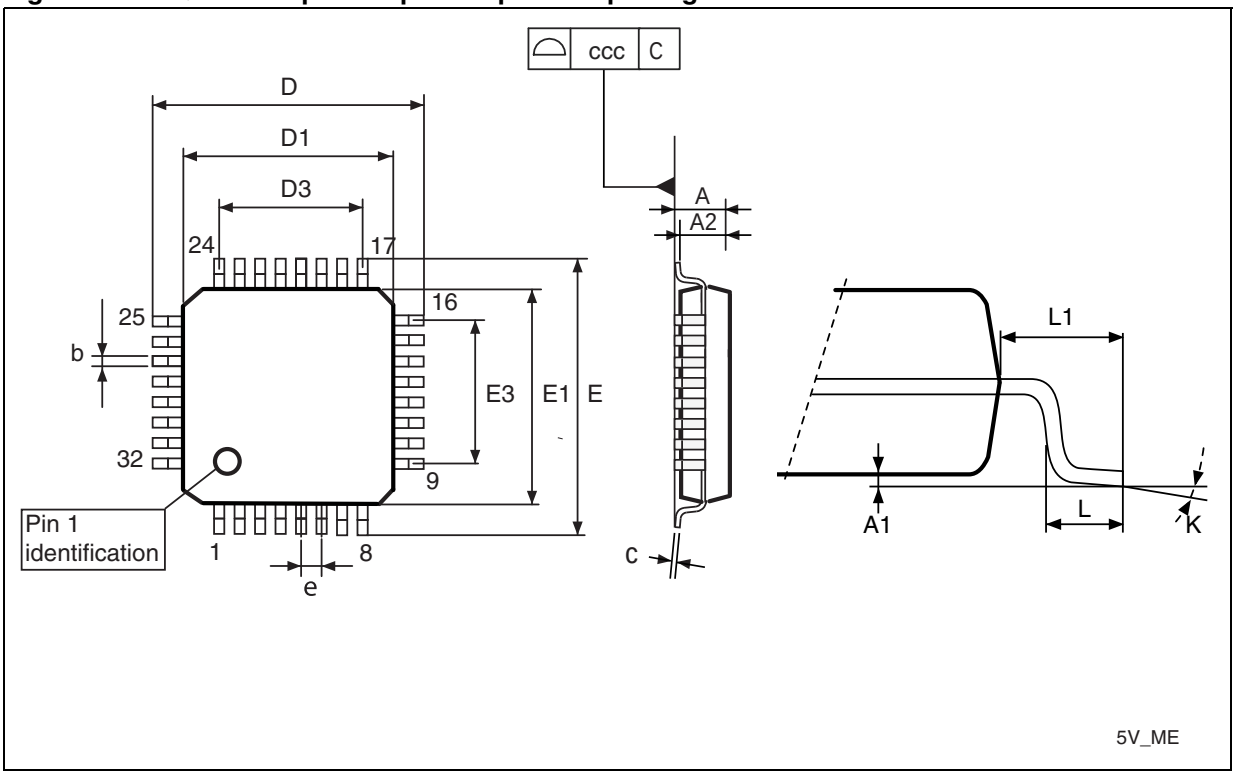
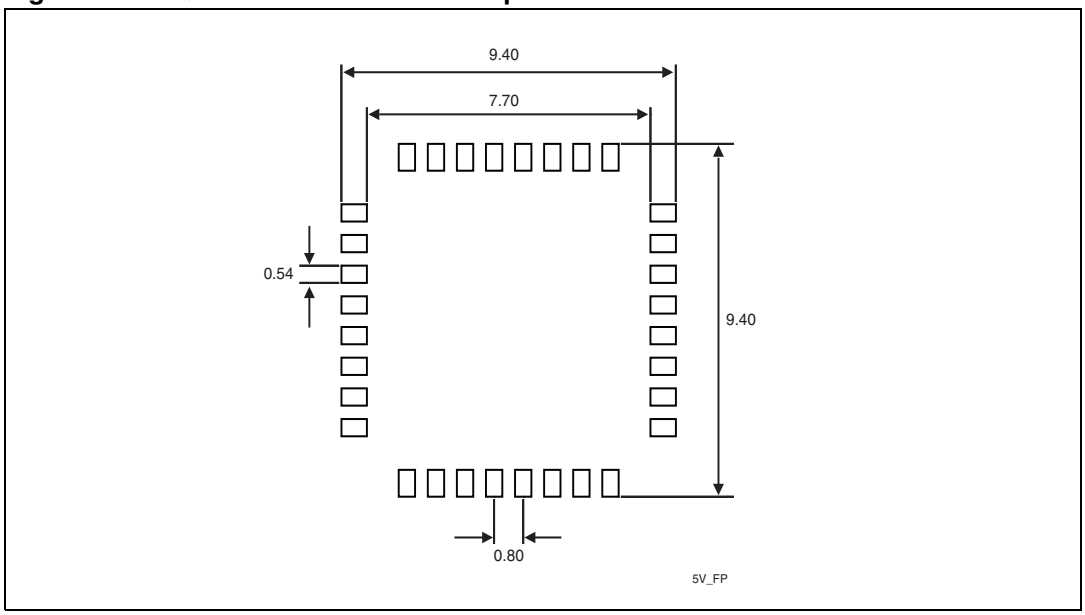


Table 11. LQFP32 32-pin low profile quad flat package, mechanical data

Dim.	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.600			0.2205	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.600			0.2205	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	

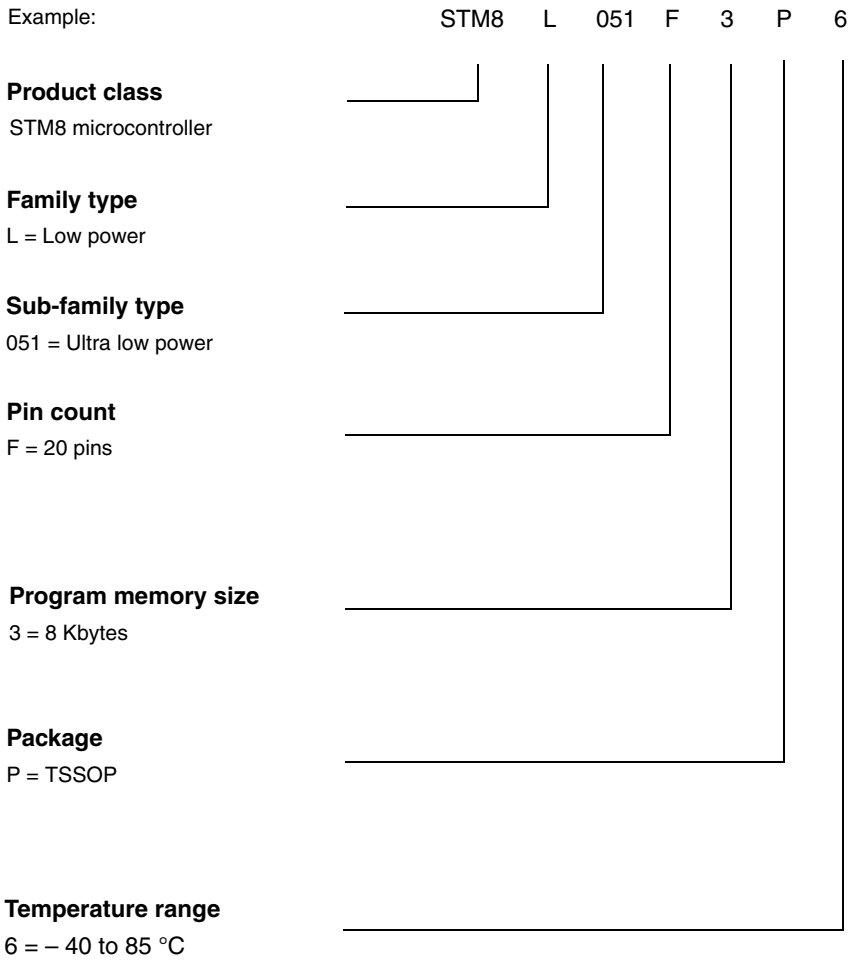
Figure 8. LQFP32 recommended footprint



1. Dimensions are in millimeters

8 Device ordering information

Figure 9. Low density value line STM8L05xxx ordering information scheme



For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST sales office nearest to you.

9 Revision history

Table 12. Document revision history

Date	Revision	Changes
23-Apr-2012	1	Initial release.

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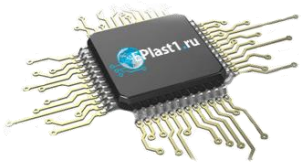

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