# HMC910LC4B

v03.1211

## BROADBAND ANALOG TIME DELAY, DC - 24 GHz

### Typical Applications

The HMC910LC4B is ideal for:

- Synchronization of clock and data
- Transponder design
- Serial Data Transmission up to 32 Gbps
- Broadband Test & Measurement
- RF ATE Applications

### Features

Very Wide Bandwidth: DC - 24 GHz

Continuous Adjustable Delay Range: 70 ps

Single-Ended or Differential Operation

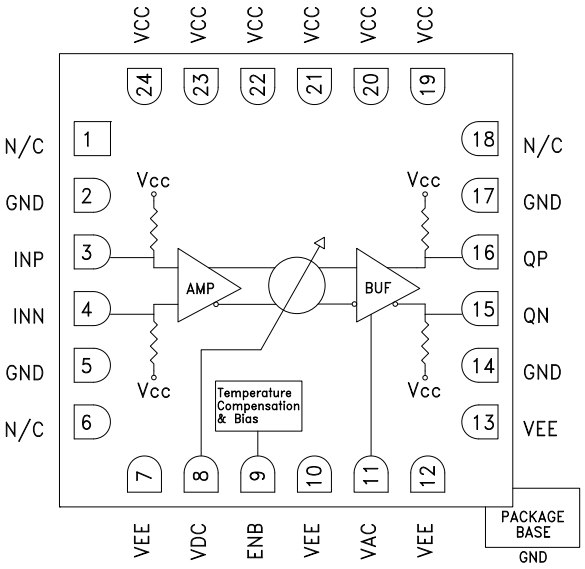
Adjustable Differential Output Voltage Swing: 170 - 760 mVp-p @ 24 GHz

Delay Control Modulation Bandwidth: 10 MHz

Single Supply: +3.3V

24 Lead Ceramic 4x4mm SMT Package: $16mm^2$

### Functional Diagram




### General Description

The HMC910LC4B is a broadband time delay with 0 to 70 ps continuously adjustable delay range. The delay control is linearly monotonic with respect to the control voltage, VDC and the control input has a modulation bandwidth of 10 MHz. The device provides a differential output voltage with constant amplitude for single-ended or differential input voltages above the input sensitivity level, while the output voltage swing may be adjusted using the VAC control pin. The HMC910LC4B features internal temperature compensation and bias circuitry to minimize delay variations with temperature. The device also features an enable pin, ENB. All RF input and outputs of the HMC910LC4B are internally terminated with 50 Ohms to Vcc, and may either be AC or DC coupled. Output pins can be connected directly to a 50 Ohm to Vcc terminated system, while DC blocking capacitors must be used if the terminated system input is 50 Ohms to a DC voltage other than Vcc.

### Electrical Specifications, $T_A$ = +25° C, Vcc = 3.3V, Vee = 0V, GND = 0V

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Power Supply Voltage | ± %9 Tolerance | 3 | 3.3 | 3.6 | V |
| Power Supply Current | VAC = 2.6V | 400 | 475 | 550 | mA |
| Time Delay Range | @ 10 GHz | 59 | 62.5 | | ps |
| | @ 20 GHz | 63 | 66.5 | | ps |
| | @ 24 GHz | 67 | 70.5 | | ps |
| Maximum Data Rate | | 32 | | | Gbps |
| Maximum Clock Frequency | | 24 | | | GHz |
| Delay Control Modulation Bandwidth | | | 10 | | MHz |
| Delay Control Voltage (VDC) | | 1.1 | | 2.3 | V |
| Output Amplitude Control Voltage (VAC) | | 1.7 | 2.6 | 2.7 | V |



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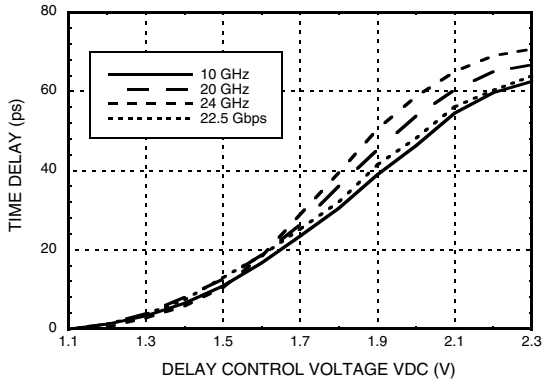
## Electrical Specifications, $T_A$ = +25° C, Vcc = 3.3V, Vee = 0V, GND = 0V *(Continued)*

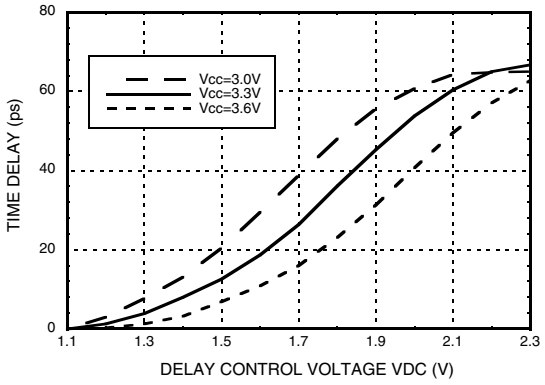
| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Input Low Voltage | VIL | Vcc-500 | Vcc-200 | Vcc-25 | mV |
| Input High Voltage | VIH | Vcc+25 | Vcc+200 | Vcc+500 | mV |
| Input Amplitude | Single-ended, peak-to-peak | 50 | | 1000 | mVp-p |
| | Differential, peak-to-peak | 100 | | 2000 | mVp-p |
| Output Amplitude | Differential, peak-to-peak @ 10 GHz | 210 | | 1020 | mVp-p |
| | Differential, peak-to-peak @ 20 GHz | 190 | | 880 | mVp-p |
| | Differential, peak-to-peak @ 24 GHz | 170 | | 760 | mVp-p |
| Input Return Loss | frequency < 25 GHz | | 12 | | dB |
| Output Return Loss | frequency < 25 GHz | | 14 | | dB |
| Deterministic Jitter, Jd [1] | | | 6 | | ps, pp |
| Additive Random Jitter, Jr | @24 GHz clock input | | | 0.3 | ps, rms |
| Rise Time, tr [1] | | | 14 | | ps |
| Fall Time, tf [1] | | | 14 | | ps |
| Propagation Delay, td | @20 GHz clock input | | 360 | | ps |
| Time Delay Temperature Sensitivity | @ 20 GHz clock input | | -0.03 | | ps/°C |

[1] $V_{data}$ = Differential 300 mVp-p, $f_{data}$ = 22.5 Gbps PRBS $2^{23}$-1 pattern

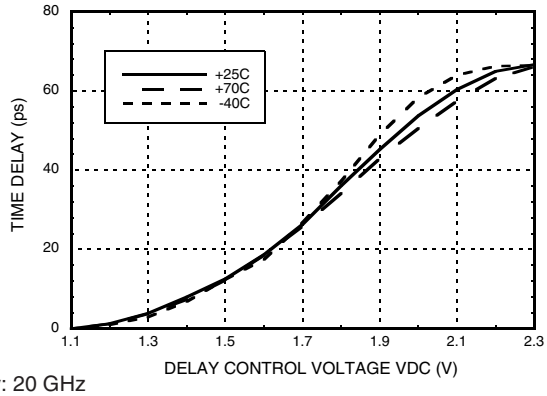
### Time Delay vs. VDC & Frequency [1]




### Time Delay vs. VDC & Supply Voltage [1][2]




### Time Delay vs. VDC & Temperature [1][2]




[1] VAC = 2.6V [2] Input Frequency: 20 GHz



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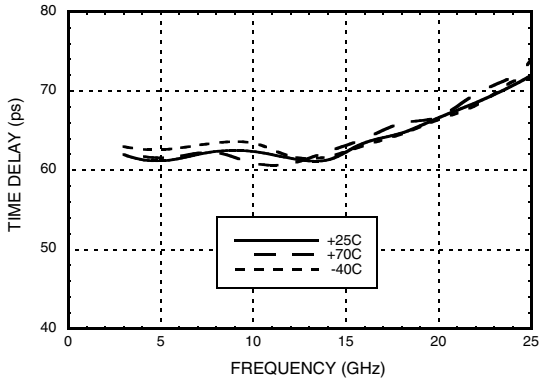
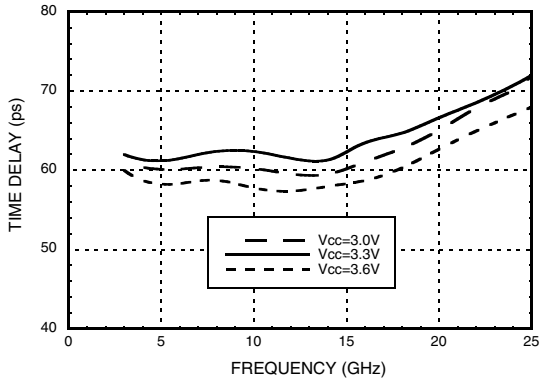
## BROADBAND ANALOG TIME DELAY, DC - 24 GHz



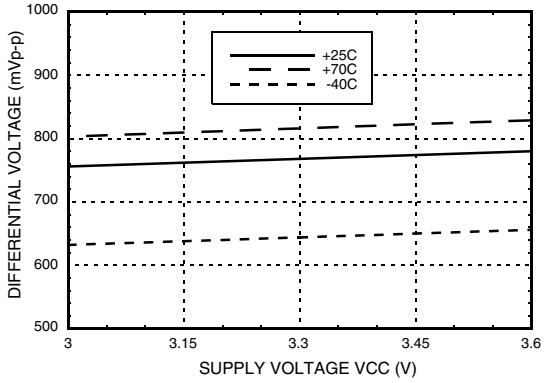
### Programmable Max. Time Delay Range vs. Frequency & Temperature [1]



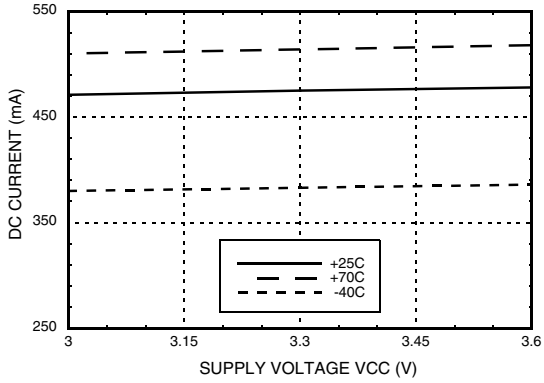

### Programmable Max. Time Delay Range vs. Frequency & Supply Voltage [1]



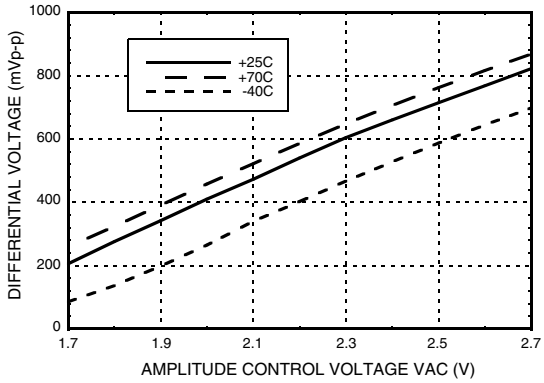

### Differential Output Swing vs. Supply Voltage [1][2][3]



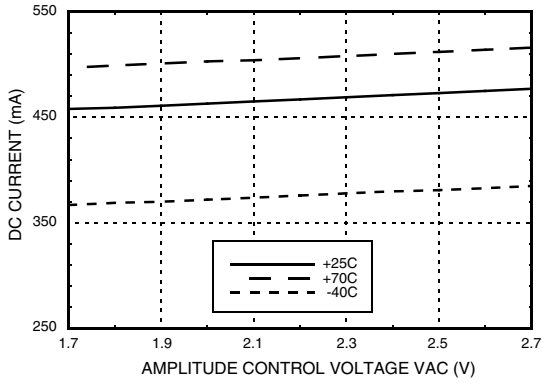

### DC Current vs. Supply Voltage [1][2][3]




### Differential Output Swing vs. VAC [2][3]




### DC Current vs. VAC [2][3]




[1] VAC = 2.6V [2] VDC = 1.1V [3] Input Frequency: 20 GHz



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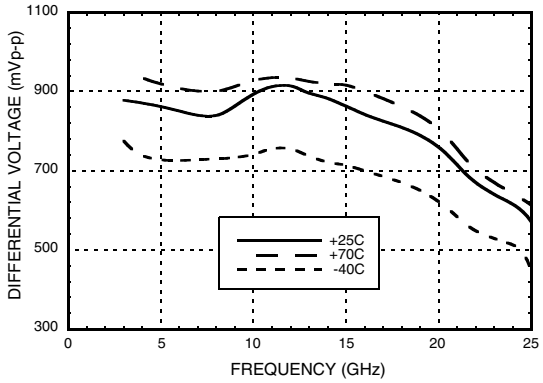
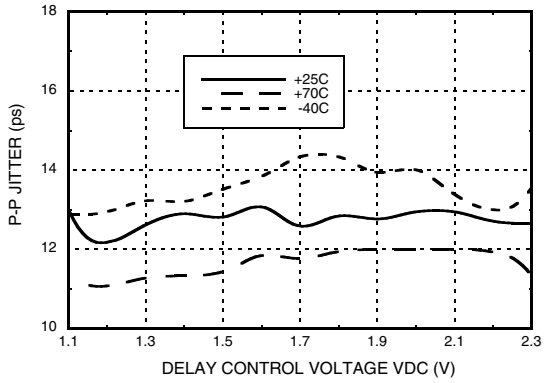
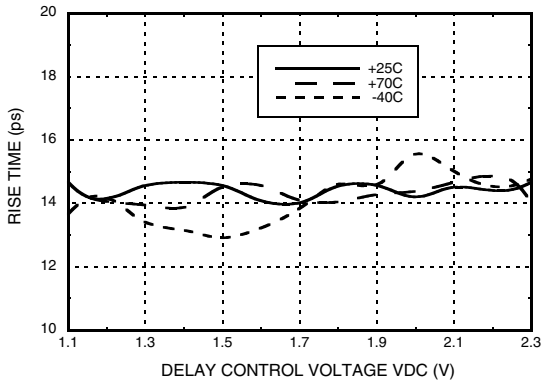
### Differential Output Swing vs. Frequency [1][2]



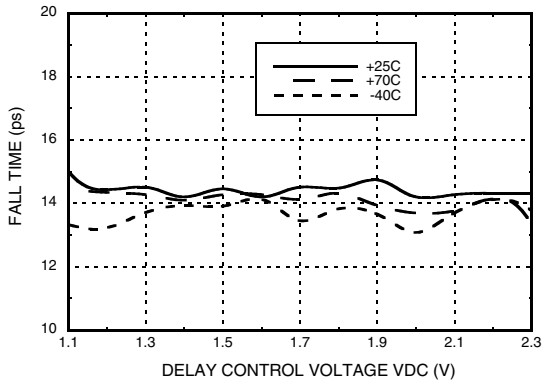

### Peak-to-Peak Jitter vs. VDC [1][3][4]



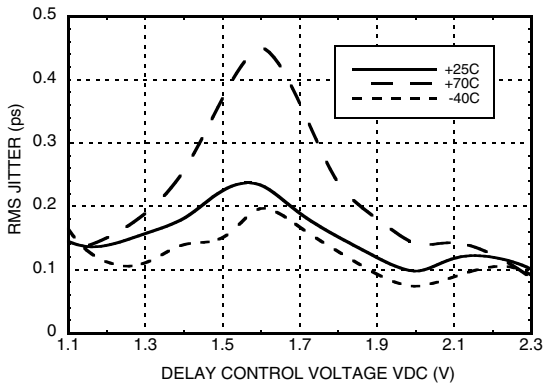

### Rise Time vs. VDC [1][3]



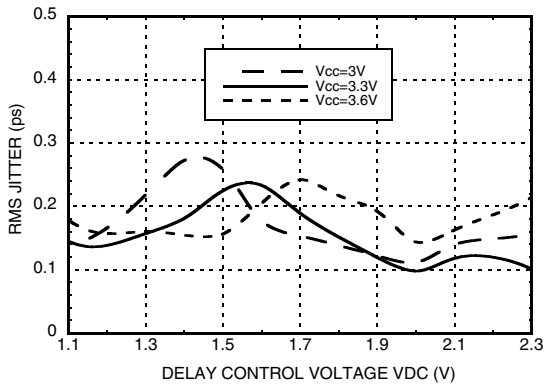

### Fall Time vs. VDC [1][3]




### RMS Jitter vs. VDC & Temperature [1][5]




### RMS Jitter vs. VDC & Supply Voltage [1][5]




[1] VAC = 2.6V [2] VDC = 1.1V [3] Input data rate: 22.5 Gbps PRBS $2^{23}$-1 [4] Source jitter was not deembeded

[5] Random jitter is calculated with the formula RJadded = √ [ (RJtested)2 – (RJsystem)2 ] at 24 GHz clock signal



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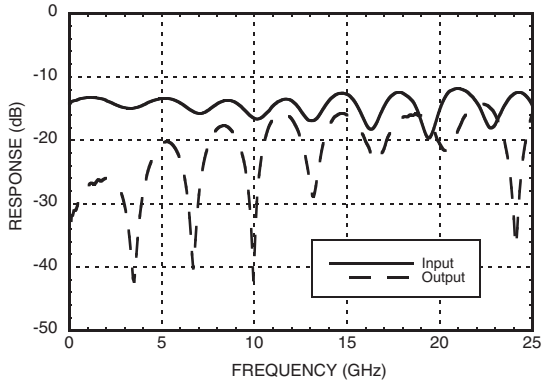
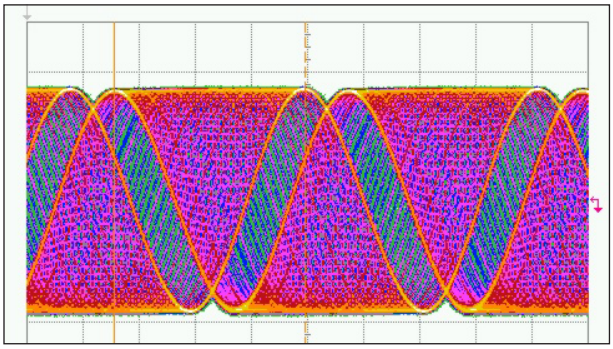
### Return Loss vs. Frequency [1][2][3]




### Output Eye Diagram Continuous Snapshot for 24 GHz Input

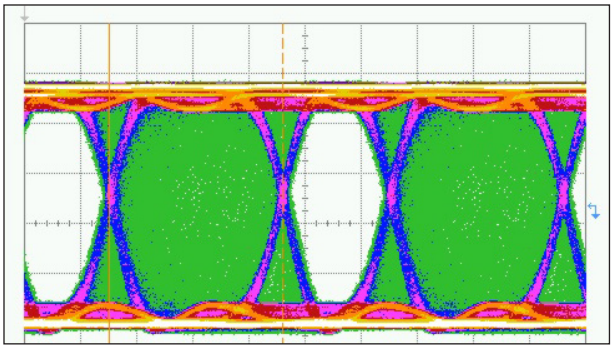


Time Scale: 10 ps/div
Amplitude Scale: 80 mV/div

Test Conditions:
VCC = 3.3V, VAC = 2.6V,
VDC = varied from 1.6V to 1.9V
(%25 of the whole delay range)
Input Data: Single ended 300 mVp-p 24 GHz clock signal

Measurement Result:
Time Delay = 34 ps

### Output Eye Diagram Continuous Snapshot for 10 Gbps Input



Time Scale: 20 ps/div
Amplitude Scale: 100 mV/div

Test Conditions:
VCC = 3.3V, VAC = 2.6V,
VDC = varied from 1.1V to 2.3V
(%100 of the whole delay range)
Input Data: Differential 300 mVp-p 10 Gbps NRZ PRBS
$2^{23}$-1 pattern

Measurement Result:
Time Delay = 61.5 ps

[1] VAC = 2.6V [2] VDC = 1.1V [3] Device measured on evaluation board with single-ended time domain gating



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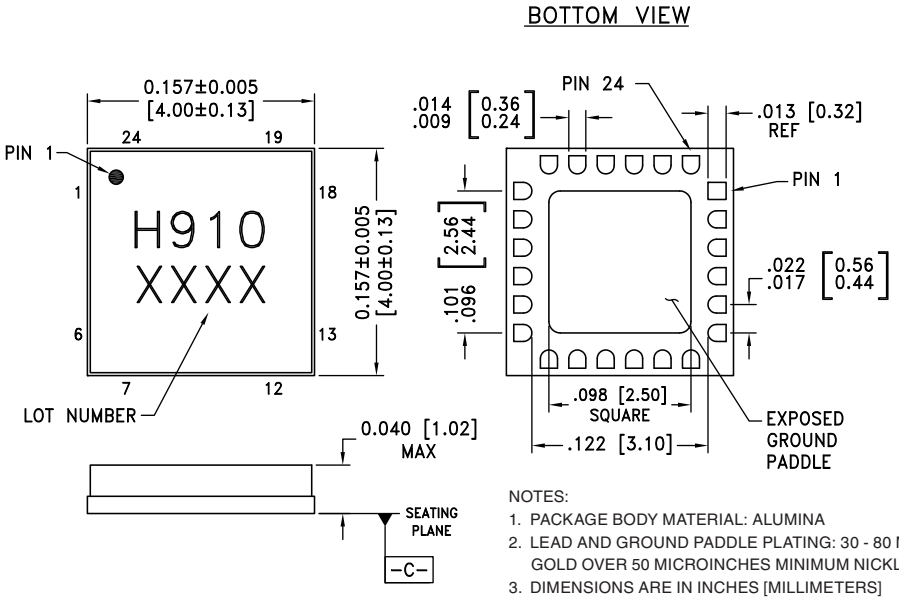
## Absolute Maximum Ratings

| | |
|---|---|
| Power Supply Voltage (Vcc) | -0.5V to +3.7V |
| Input Voltage | Vcc -1.2V to Vcc +0.5V |
| Channel Temperature (Tc) | 125 °C |
| Continuous Pdiss (T = 85 °C) (derate 54.96 mW/°C above 85 °C) | 2.2 W |
| Thermal Resistance (junction to ground paddle) | 18.20 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +70 °C |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing




NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30 - 80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKLE
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND

## Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [2] |
|---|---|---|---|---|
| HMC910LC4B | Alumina, White | Gold over Nickel | MSL3 [1] | H910<br>XXXX |

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX



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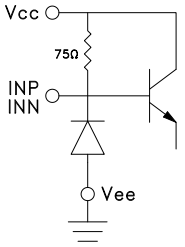
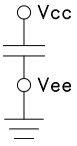
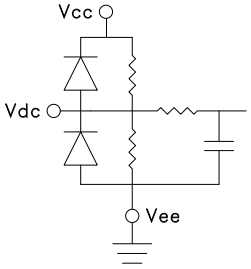
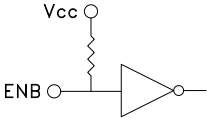
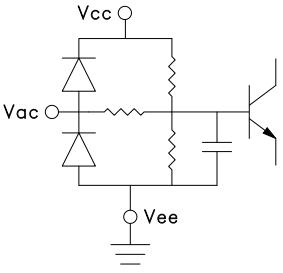
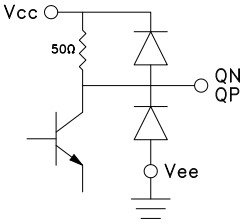
## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 6, 18 | N/C | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 2, 5, 14, 17 Package Bottom | GND | Signal grounds should be connected to 0V. Ground paddle must be connected to DC ground |  |
| 3, 4 | INP, INN | Differential Signal Inputs |  |
| 7, 10, 12, 13 | Vee | Supply grounds should be connected to 0V. |  |
| 8 | Vdc | Time delay control pin. |  |
| 9 | ENB | Enable pin for the time delay. For normal operation; leave the pin open or apply +3.3V. To disable the part apply 0V. When disabled total current consumption drops to 15mA. |  |
| 11 | Vac | Output amplitude control pin. |  |
| 15, 16 | QN, QP | Differential Signal Outputs |  |



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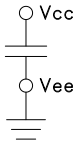
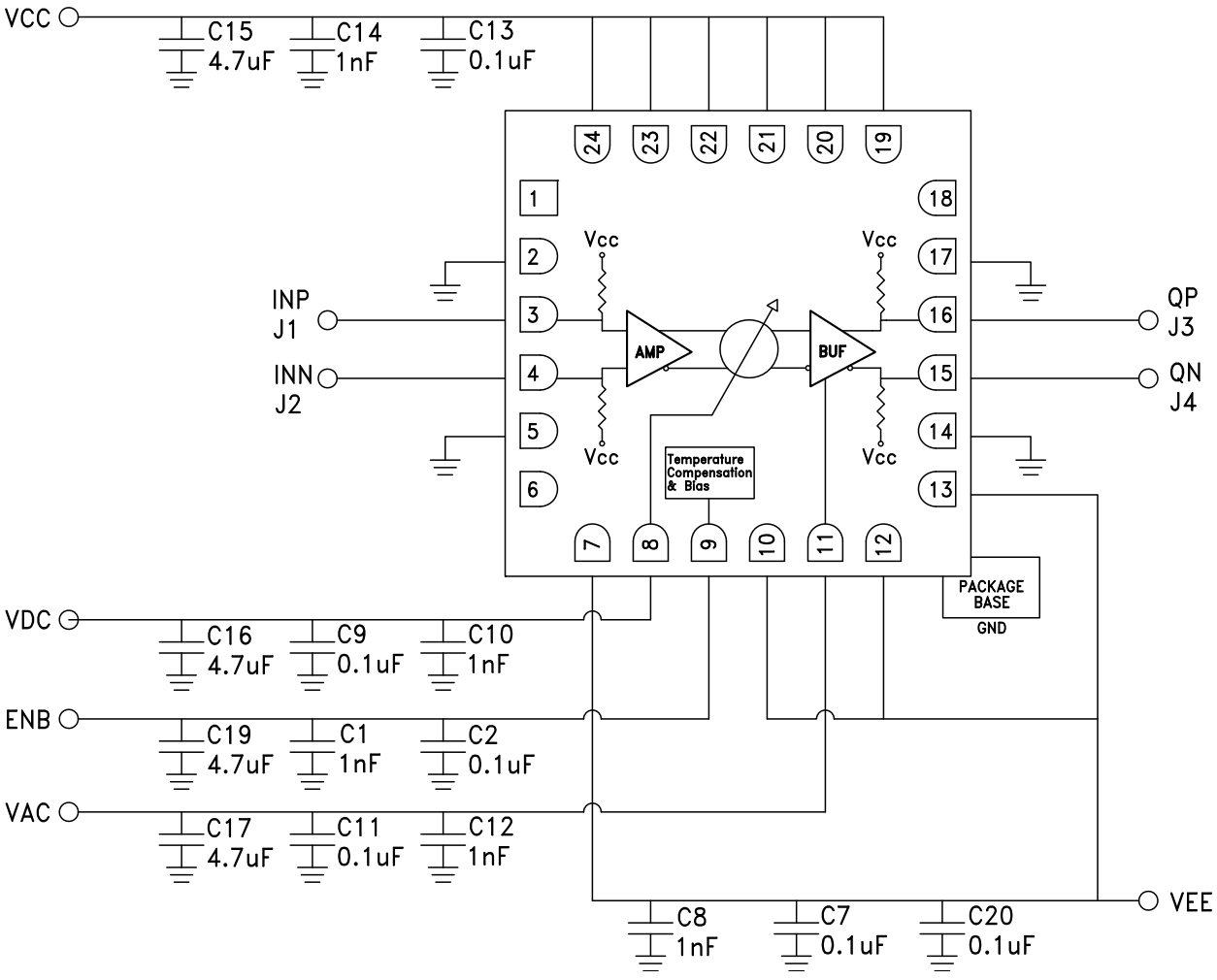
## Pin Descriptions *(Continued)*

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 19 - 24 | Vcc | Positive supply |   |

## Application Circuit



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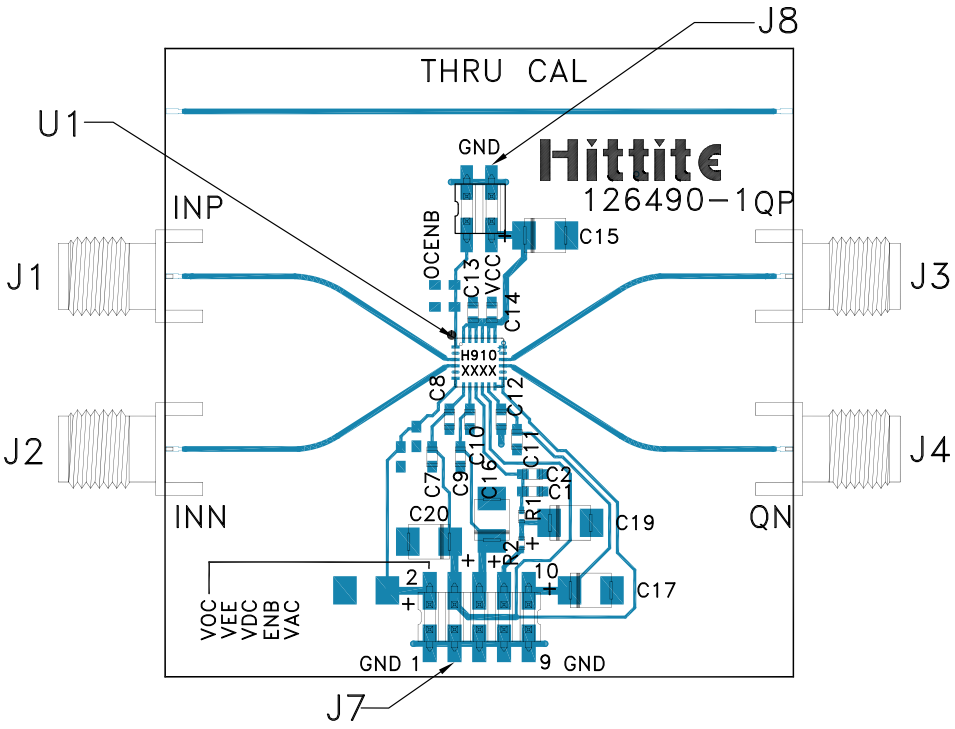
## Evaluation PCB




## List of Materials for Evaluation PCB 129874 [1]

| Item | Description |
|---|---|
| J1 - J4 | K Connector |
| J7 | 10 Pin DC Connector |
| J8 | 4 Pin DC Connector |
| C1, C8, C10, C12, C14 | 1000 pF Capacitor, 0603 Pkg. |
| C2, C7, C9, C11, C13 | 0.1 µF Capacitor, 0603 Pkg. |
| C15, C16, C17, C19, C20 | 4.7 µF Capacitor, Tantalum |
| U1 | HMC910LC4B Analog Phase Shifter |
| PCB [2] | 126490 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25 FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.



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**Notes:**





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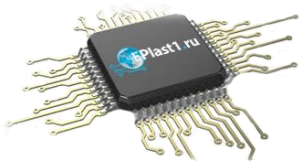
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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