

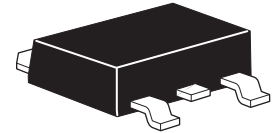
ZXMN7A11K

70V N-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}=70V : R_{DS(on)}=0.13\Omega$

$I_D=6.1A$

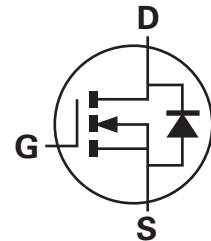


Description

This new generation of trench MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage power management applications.

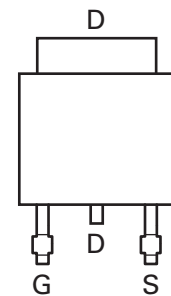
Features

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- DPAK package



Applications

- DC-DC converters
- Power management functions
- Disconnect switches
- Motor control
- Class D audio output stages



Pinout - top view

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN7A11KTC	13	16	2,500

Device marking

ZXMN
7A11

ZXMN7A11K

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DSS}	70	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current @ $V_{GS}=10V$; $T_A=25^\circ C$ (b) @ $V_{GS}=10V$; $T_A=70^\circ C$ (b) @ $V_{GS}=10V$; $T_A=25^\circ C$ (a)	I_D	6.1 4.9 4.2	A
Pulsed drain current (c)	I_{DM}	17	A
Continuous source current (body diode) (b)	I_S	8.7	A
Pulsed source current (body diode) (c)	I_{SM}	17	A
Power dissipation at $T_A = 25^\circ C$ (a) Linear derating factor	P_D	4.06 32.4	W mW/ $^\circ C$
Power dissipation at $T_A = 25^\circ C$ (b) Linear derating factor	P_D	8.5 68	W mW/ $^\circ C$
Power dissipation at $T_A = 25^\circ C$ (d) Linear derating factor	P_D	2.11 16.8	W mW/ $^\circ C$
Operating and storage temperature range	T_j, T_{stg}	-55 to +150	$^\circ C$

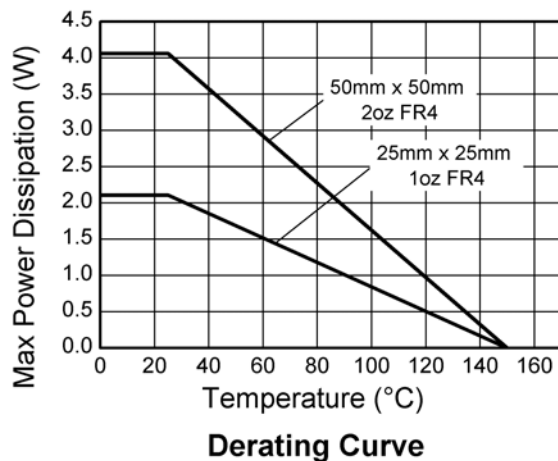
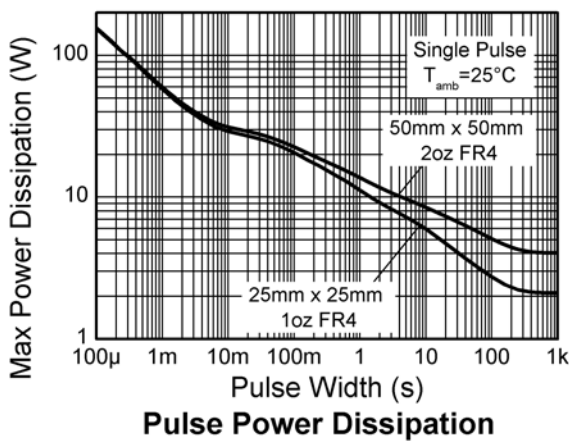
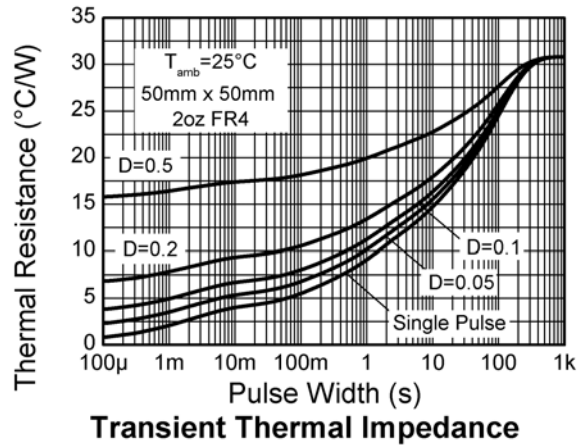
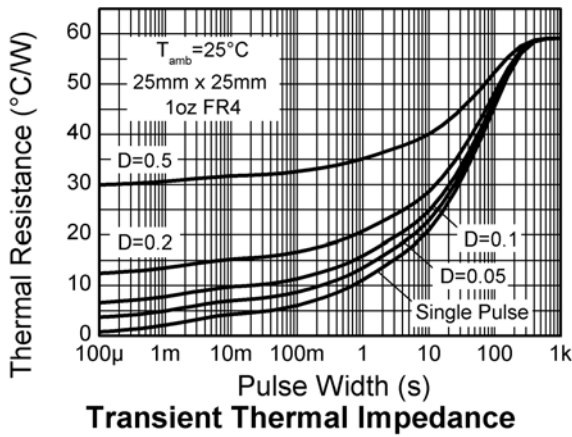
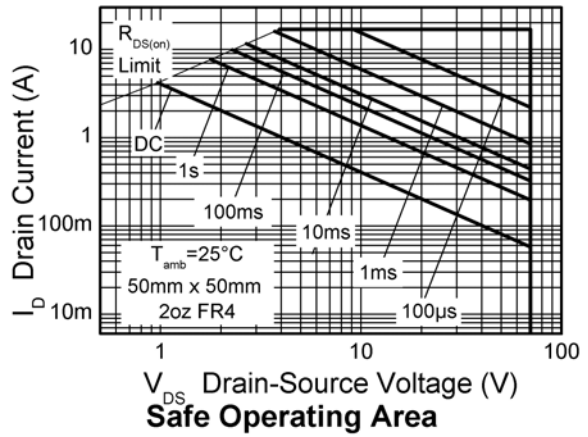
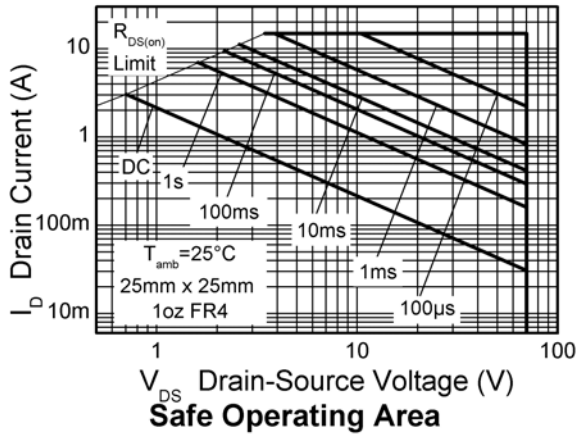
Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient	$R_{\theta JA}$	30.8	$^\circ C/W$
Junction to ambient	$R_{\theta JA}$	14.7	$^\circ C/W$
Junction to ambient	$R_{\theta JA}$	59.1	$^\circ C/W$

NOTES:

- (a) For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating 50mm x 50mm x 1.6mm FR4 PCB, $D=0.02$ pulse width=300 μs - pulse width limited by maximum junction temperature.
- (d) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

Characteristics



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Electrical characteristics (at Tamb = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	70			V	$I_D = 250\mu A, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 70V, V_{GS} = 0V$
Gate-body leakage	I_{GSS}			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Gate-source threshold voltage	$V_{GS(th)}$	1.0			V	$I_D = 250\mu A, V_{DS} = V_{GS}$
Static drain-source on-state resistance ^(*)	$R_{DS(on)}$			0.13	Ω	$V_{GS} = 10V, I_D = 4.4A$
				0.19	Ω	$V_{GS} = 4.5V, I_D = 3.8A$
Forward transconductance ^{(*)(‡)}	g_{fs}		4.66		S	$V_{DS} = 15V, I_D = 4.4A$
Dynamic^(‡)						
Input capacitance	C_{iss}		298		pF	$V_{DS} = 40V, V_{GS} = 0V$ $f = 1MHz$
Output capacitance	C_{oss}		35		pF	
Reverse transfer capacitance	C_{rss}		21		pF	
Switching^{(†) (‡)}						
Turn-on-delay time	$t_{d(on)}$		1.9		ns	$V_{DD} = 35V, I_D = 1A$ $R_G \approx 6.0\Omega, V_{GS} = 10V$
Rise time	t_r		2		ns	
Turn-off delay time	$t_{d(off)}$		11.5		ns	
Fall time	t_f		5.8		ns	
Total gate charge	Q_g		4.35		nC	$V_{DS} = 35V, V_{GS} = 5V$ $I_D = 4.4A$
Total gate charge	Q_g		7.4		nC	$V_{DS} = 35V, V_{GS} = 10V$ $I_D = 4.4A$
Gate-source charge	Q_{gs}		1.06		nC	
Gate drain charge	Q_{gd}		1.8		nC	
Source-drain diode						
Diode forward voltage ^(*)	V_{SD}		0.85	0.95	V	$T_j = 25^\circ C, I_S = 2.5A,$ $V_{GS} = 0V$
Reverse recovery time ^(‡)	t_{rr}		19.8		ns	$T_j = 25^\circ C, I_S = 2.5A,$ $di/dt = 100A/\mu s$
Reverse recovery charge ^(‡)	Q_{rr}		14		nC	

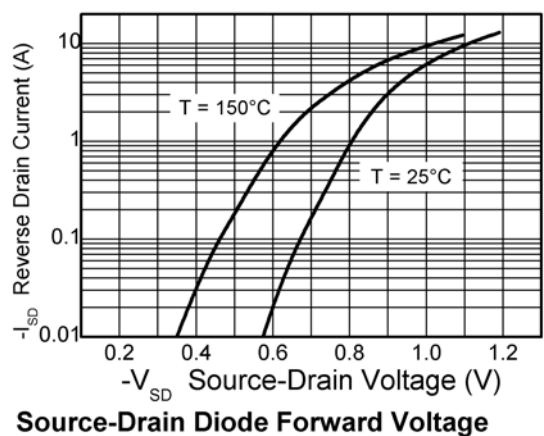
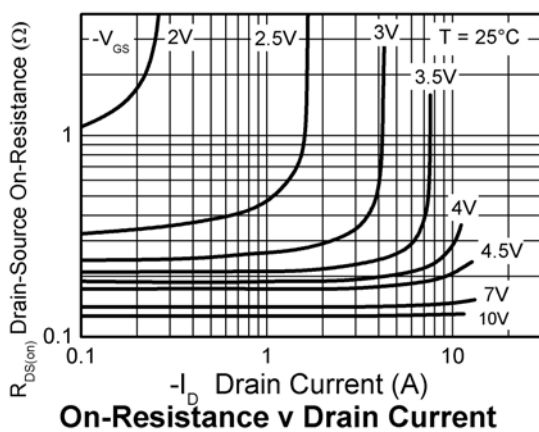
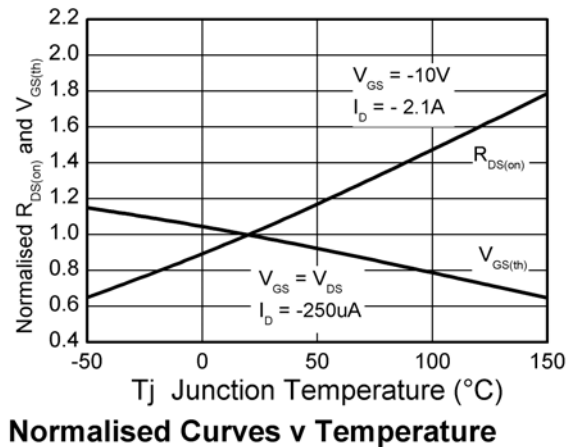
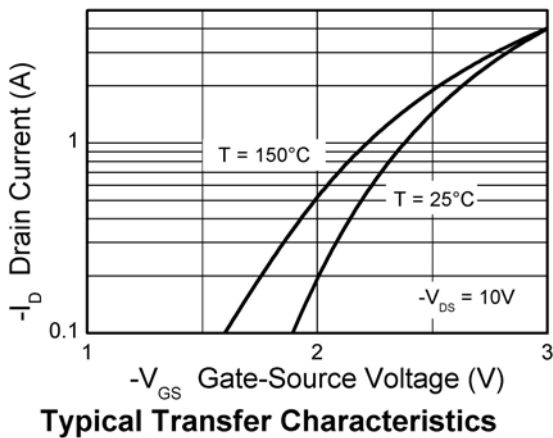
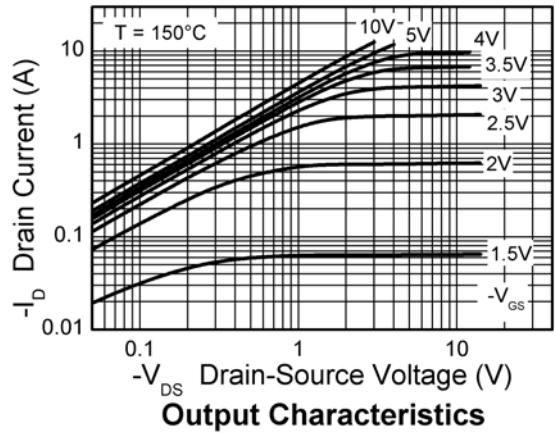
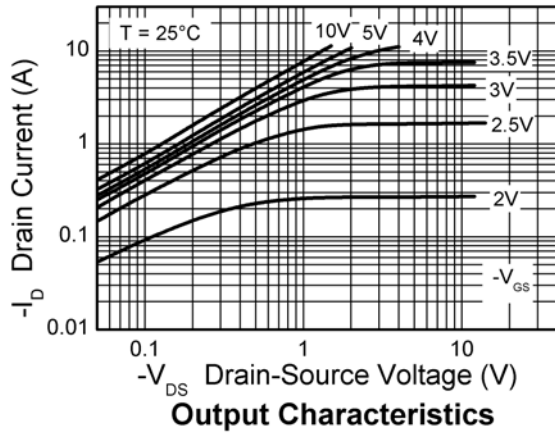
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

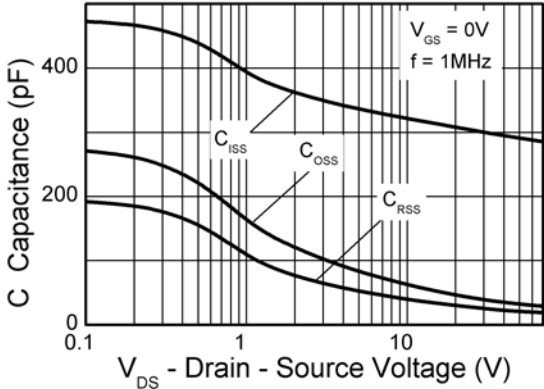
(†) Switching characteristics are independent of operating junction temperature.

(‡) For design aid only, not subject to production testing.

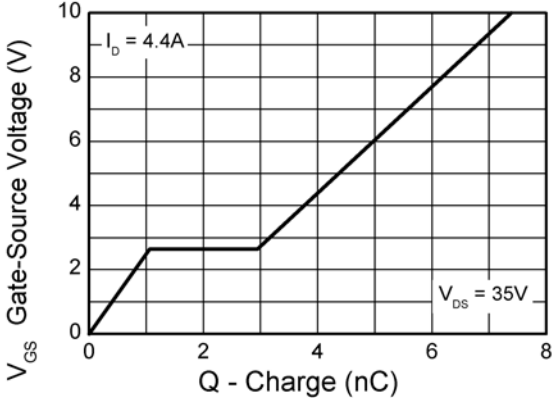
Typical characteristics



Typical characteristics



Capacitance v Drain-Source Voltage



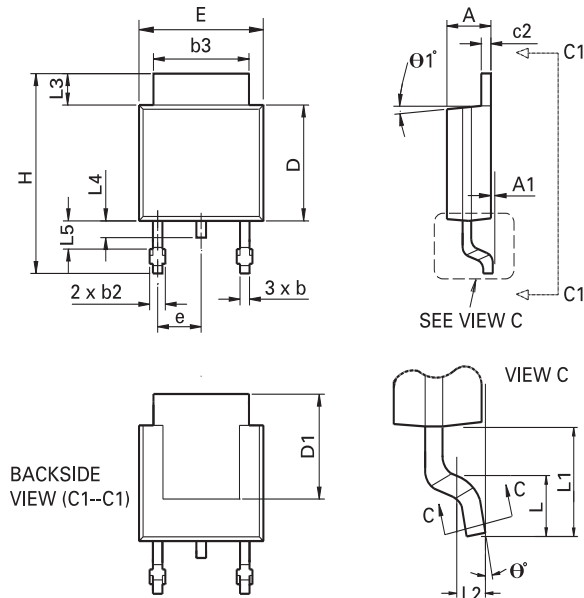
Gate-Source Voltage v Gate Charge

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Package outline - DPAK



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.086	0.094	2.18	2.39	e	0.090 BSC		2.29 BSC	
A1	-	0.005	-	0.127	H	0.370	0.410	9.40	10.41
b	0.020	0.035	0.508	0.89	L	0.055	0.070	1.40	1.78
b2	0.030	0.045	0.762	1.14	L1	0.108 REF		2.74 REF	
b3	0.205	0.215	5.21	5.46	L2	0.020 BSC		0.508 BSC	
c	0.018	0.024	0.457	0.61	L3	0.035	0.065	0.89	1.65
c2	0.018	0.023	0.457	0.584	L4	0.025	0.040	0.635	1.016
D	0.213	0.245	5.41	6.22	L5	0.045	0.060	1.14	1.52
D1	0.205	-	5.21	-	theta 1°	0°	10°	0°	10°
E	0.250	0.265	6.35	6.73	theta 0°	0°	15°	0°	15°
E1	0.170	-	4.32	-	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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- Техническая поддержка проекта;
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