71M6403
Electronic Trip Unit

SEPTEMBER 2006

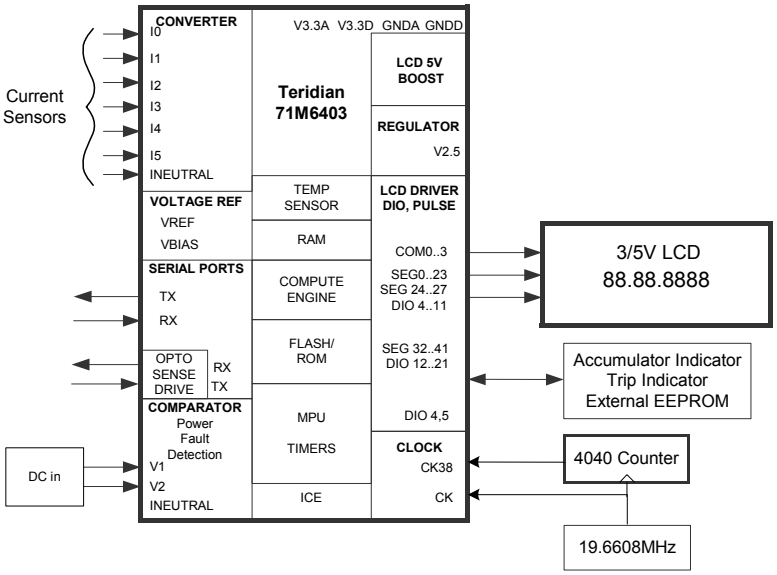
GENERAL DESCRIPTION

The Teridian 71M6403 is an electronic trip unit (ETU) system-on-chip device for air circuit breakers (ACB), molded case circuit breakers (MCCB) and other types of intelligent switchgear. Utilizing Teridian's patented Single Converter Technology™, the 71M6403 incorporates a 22-bit delta-sigma ADC, 7 current sensor inputs, digital temperature compensation, precision voltage reference, 32-bit programmable computation engine, timers, Real Time Clock (RTC), two UARTs and a single cycle execution 8-bit MCU.

Armed with an internal digital di/dt integrator, this programmable device supports either current transformer (CT) or Rogowski-Coils for any or all input channels and provides instantaneous and delayed over current, earth-leakage, ground-fault and arc fault protection functions. Furthermore, the device may be configured to support any number of conventional or custom protection algorithms that fit specific load configurations in the field.

The 71M6403 also includes a 5V LCD charge pump as well as 3V LCD support with up to 168 pixels display and up to 22 DIO pins. Easy conversion to ROM offers unprecedented cost structure for high volume MCCB applications.

A complete suite of in-circuit emulator (ICE) and development tools, a powerful real-time signal monitoring tool, programming libraries and reference designs enable rapid development of advanced switchgear.



FEATURES

- 22-bit Sigma-delta converter
- Six main sensor inputs
- One auxiliary input
- Supports CT or Rogowski Coils
- Internal di/dt integrators
- < 5 msec. startup time
- Better than 10ppm/°C accuracy
- Instantaneous and delay trip
- Peak & RMS current measurement
- Calculated or measured GND current
- Power measurement functions option
- Internal temperature sensor
- Digital temperature compensation
- Independent 32-bit compute engine
- Two UART ports
- Two timers
- Hardware watchdog
- Internal power fault detector
- Real Time Clock (RTC)
- Battery backup (RTC, RAM)
- 8-bit MPU (80515) - 1 clock cycle per instruction (5 Mhz max.)
- LCD driver (≤168 pixels)
- 5V LCD charge pump
- Up to 22 general purpose I/O pins
- High speed serial interface (SSI)
- I^2C EEPROM interface
- 64KB Flash, 7KB RAM
- Flash memory security
- 30mW @ 3.3V
- 100-lead LQFP package

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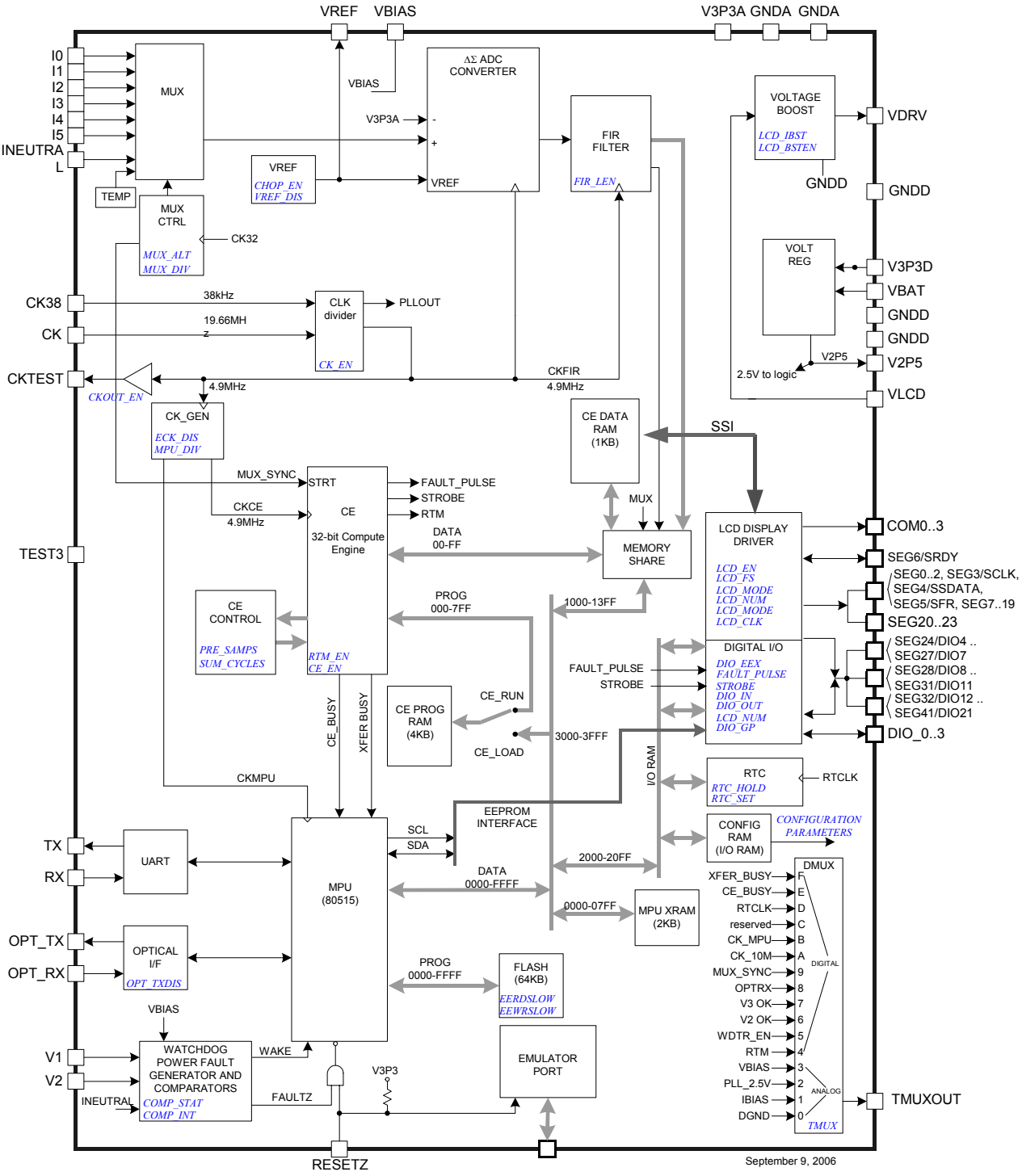


Figure 1: IC Functional Block Diagram

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HARDWARE DESCRIPTION

Hardware Overview

The TERIDIAN 71M6403 single chip Electronic Trip Unit integrates all primary functional blocks required to implement a solid-state circuit breaker. Included on chip are an analog front end (AFE), an 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515), an independent 32-bit digital computation engine (CE), a voltage reference, LCD drivers, RAM, FLASH memory, and a variety of I/O pins. Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts, and Rogowski (*di/dt)* Coils.

Measurements can be displayed on either a 3V or a 5V LCD. Flexible mapping of LCD display segments will facilitate integration with any LCD format. The design trade-off between the number of LCD segments and DIO pins can be flexibly configured using memory-mapped I/O to accommodate various requirements.

The 71M6403 includes several I/O peripheral functions that improve the functionality of the device and reduce the component count for most circuit breaker applications. The I/O peripherals include two UARTs, digital I/O, comparator inputs, LCD display drivers, I^2C interface and an optical/IR interface.

One of the two internal UARTs (UART1) is adapted to support an Infrared LED with higher internal drive output and sense input. It can also be configured to function as a standard UART with normal digital IOs.

A block diagram of the chip is shown in Figure 1. A detailed description of various hardware blocks follows.

External Components

The 71M6403 is optimized for fast startup. To achieve this, an external 19.6608 MHz oscillator is required to drive CK, the primary clock input. The frequency for the CK38 input is generated from the 19.6608 MHz oscillator using an inexpensive 'HC4040 counter chip. The divide-by-512 output of the 'HC4040 generates a 38.4 kHz signal.

Analog Front End (AFE)

The AFE of the TERIDIAN 71M6403 Electronic Trip Unit IC is comprised of an input multiplexer, a delta-sigma A/D converter with internal voltage reference, followed by an FIR filter. A block diagram of the AFE is shown in Figure 3.

Multiplexer

The input multiplexer supports eight input signals that are applied to the pins I0 through I5, INEUTRAL plus the output of the internal temperature sensor. The multiplexer can be operated in two modes:

- During a normal multiplexer cycle, the signals from the six pins I0 through I5 are selected.
- During the alternate multiplexer cycle, the temperature signal (TEMP) , INEUTRAL, and I1, I3, I4, I5 (EQU = 101) signal sources are selected. Use of the alternate multiplexer cycle is not recommended for fast response circuit breaker applications. Upon enabling the alternate multiplexer cycle, the I0 and I2 current samples are interrupted delaying over current trip detection response time.

Regular multiplexer sequence Mux State:						**Alternate multiplexer sequence Mux State:**					
0	1	2	3	4	5	0	1	2	3	4	5
I0	I1	I2	I3	I4	I5	TEMP	I1	INEUTRAL	I3	I4	I5

Table 1: Inputs Selected in Regular and Alternate Multiplexer Cycles (EQU = 101)

Note: Use of the alternate multiplexer cycle is not recommend.

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In a typical application, the I0 through I5 inputs are connected to current transformers or Rogowski coils that sense the current on each phase of the line voltage.

The Multiplexer Control Circuit handles the setting of the multiplexer. The function of the Multiplexer Control Circuit is governed by the I/O RAM registers *MUX_ALT* (0x2005[2]) and *MUX_DIV* (0x2002[7:6]). *MUX_DIV* controls the number of samples per cycle. It can request 2, 3, 4, or 6 multiplexer states per cycle.

Multiplexer Control Circuit also controls the FIR filter initiation and the chopping of the ADC reference voltage, VREF. The Multiplexer Control Circuit is clocked by PLLOUT, the 32768Hz clock from the PLL block derived from CK, and launches each pass through the CE program.

ADC

A single 21/22-bit delta-sigma A/D converter digitizes the power inputs to the AFE. The ADC inputs I0 - I5 are referenced to V3P3A with an input voltage range of ± 250 mv. The resolution of the ADC is programmable using the I/O RAM register *FIR_LEN* register (0x2005[4]). ADC resolution may be selected to be 21 bits (*FIR_LEN*=0), or 22 bits (*FIR_LEN*=1). Conversion time is two cycles of PLLOUT with *FIR_LEN* = 0 and three cycles with *FIR_LEN* = 1.

Accuracy, timing and functional specifications in this data sheet are based on *FIR_LEN* = 0 (two PLLOUT cycles).

Initiation of each ADC conversion is controlled by the Multiplexer Control Circuit as described previously.

FIR Filter

The finite impulse response (FIR) filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data of the FIR filter (raw data) is stored into the CE Data RAM (DRAM) location determined by the multiplexer selection. The location of the raw data in the CE DRAM is specified in the CE Program and Environment Section.

Voltage Reference

The 71M6403 includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques. The reference of the 71M6403 is trimmed in production to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

The voltage reference is chopper stabilized, i.e. the polarity can be switched by the MPU using the I/O RAM register *CHOP_ENA* (0x2002[5:4]). The two bits in the *CHOP_ENA* register enable the MPU to operate the chopper circuit in regular or inverted operation, or in “toggling” mode. When the chopper circuit is toggled in between multiplexer cycles, DC offsets on the measured signals will automatically be averaged out.

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The general topology of a chopped amplifier is given in Figure 2.

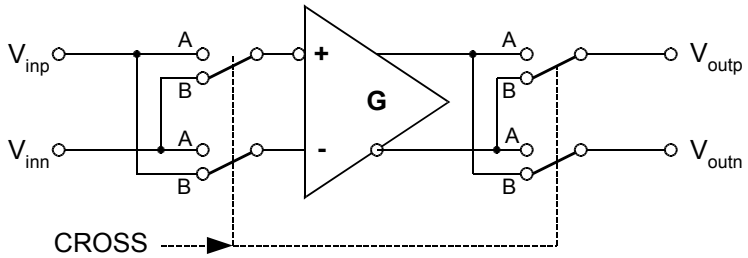


Figure 2: General Topology of a Chopped Amplifier

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS in the "A" position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the "B" position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or

Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g. after each multiplexer cycle, the offset will alternately appear on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

The Functional Description Section contains a chapter with a detailed description on controlling the *CHOP_ENA* register.

Temperature Sensor

The 71M6403 includes an on-chip temperature sensor implemented as a bandgap reference. It is used to determine the die temperature. The MPU may request an alternate multiplexer cycle containing the temperature sensor output by asserting *MUX_ALT*.

Reading the internal temperature sensor requires enabling the alternate multiplexer cycle. The alternate multiplexer cycle then displaces a normal I0-I5 current sensors acquisition cycle. Therefore, detection of an over current event may be delayed.

INEUTRAL

INEUTRAL is an analog monitor input that can be used for additional analog measurements, such as neutral current. It is sampled when the multiplexer performs an alternate multiplexer cycle. The zero reference for the INEUTRAL input is VBIAS.

INEUTRAL is also routed into the comparator block where it is compared to VBIAS. External interrupt 2 should be disabled when the INEUTRAL input is used for analog measurements.

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Functional Description

The AFE functions as a data acquisition system, controlled by the MPU. The main signals (I0, I3, I1, I4, I2, I5) are sampled and the ADC counts obtained are stored in CE RAM where they can be accessed by the CE and, if necessary, by the MPU.

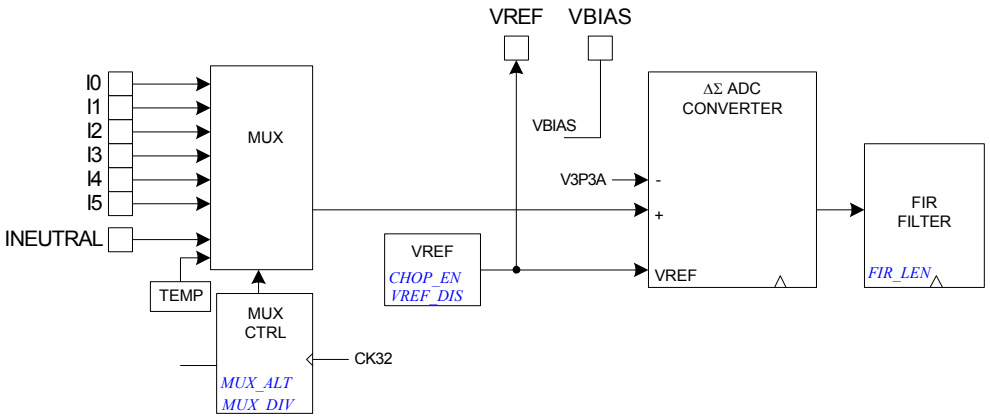


Figure 3: AFE Block Diagram

Computation Engine (CE)

The CE, a dedicated 32-bit RISC processor, performs the precision computations necessary to accurately measure currents. The CE calculations and processes include:

- Scaling of the processed samples based on chip temperature (temperature compensation) and calibration coefficients.

The CE program RAM (CE PRAM) is loaded at boot time by the MPU and then executed by the CE. Each CE instruction word is 2 bytes long. The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends (see System Timing Summary in the Functional Description Section).

The CE data RAM (CE DRAM) is shared by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR, RTM, and MPU, respectively, such that memory accesses to CE_RAM do not collide. Holding registers are used to convert 8-bit wide MPU data to/from 32-bit wide CE DRAM data, and wait states are inserted as needed, depending on the frequency of CKMPU.

Table 2 shows the CE DRAM addresses allocated to analog inputs from the AFE.

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Address	Name	Zero Reference	Description
0x00	I0	V3P3	Current input 0
0x01	I1	V3P3	Current input 1
0x02	I2	V3P3	Current input 2
0x03	I3	V3P3	Current input 3
0x04	I4	V3P3	Current input 4
0x05	I5	V3P3	Current input 5
0x06	TEMP	---	Temperature
0x07	INEUTRAL	VBIAS	INEUTRAL monitor

Table 2: CE DRAM Locations for ADC Results

CE Functional Overview

The ADC processes one sample per channel per multiplexer cycle. Figure 4 shows the timing of the six samples taken during one multiplexer cycle.

The ADC sampling process and resultant accumulation interval calculations are described in the CE Program section.

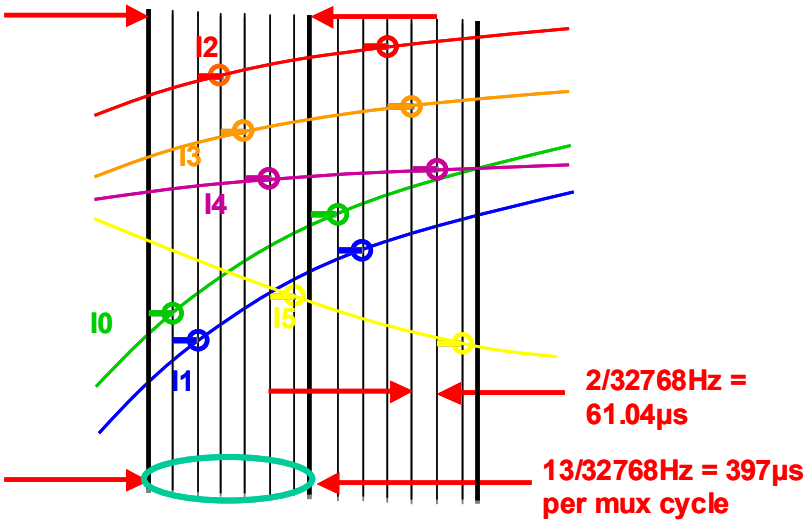


Figure 4: Samples in Multiplexer Cycle

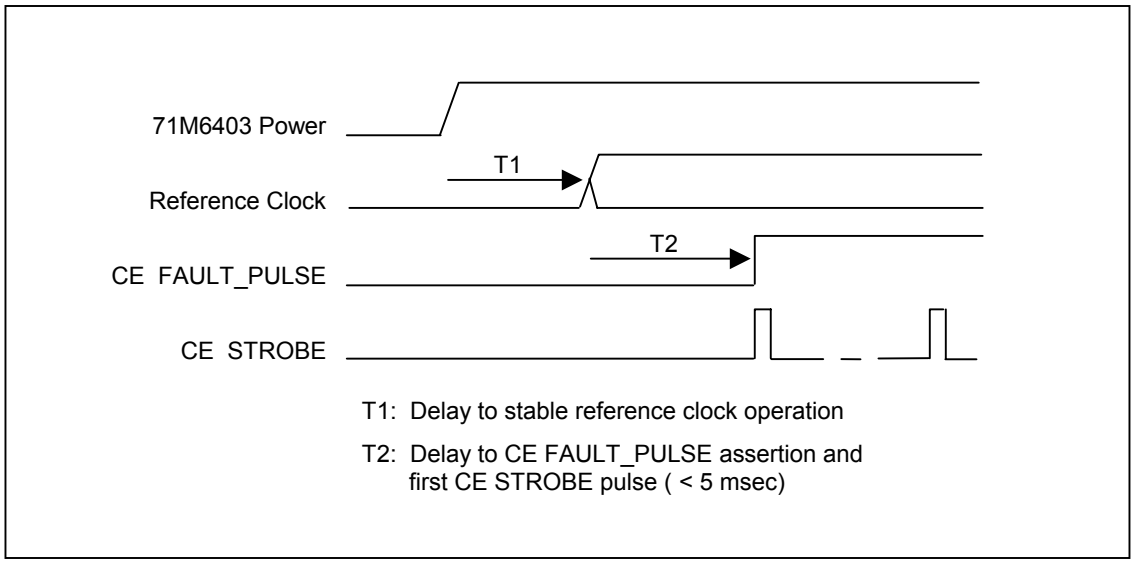
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Real-Time Monitor

The CE contains a Real Time Monitor (RTM), which can be programmed to monitor four selectable CE RAM locations at full sample rate. The four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass (see the Test Ports Section for details)

Power Up Short Circuit Detection Time

The 71M6403 detects a short circuit condition within less than 5 msec. (T2) after application of its power and a stable reference clock. This delay includes the firmware startup time for both the CE and the MPU, and for the CE to complete its initial measurements. The following diagram shows the timing delay of a CE trip indication relative to application of power and the reference clock.



Power Up Detection Time

The T1 delay is a system parameter dependent on the system clock architecture. T1 could be the start up time for an external oscillator powered from the same power source as the 71M6403, or T1 could be the delay from a system wide reference clock. If the reference clock is already stable prior to application of power to the 71M6403 (using a system wide reference clock), the T1 delay is eliminated. The resultant start up delay reduces to T2 assuming a “clean” application of power to the 71M6403.

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80515 MPU Core

80515 Overview

The 71M6403 includes an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 5MHz clock results in a processing throughput of 5 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (in average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency.

Actual processor clocking speed can be adjusted to the total processing demand of the application (current and trip calculations, memory management, LCD driver management and I/O management) using the I/O RAM register *MPU_DIV[2:0]*.

Typical measurement and circuit breaker functions based on the internal 32-bit compute engine (CE) results are available for the MPU as part of TERIDIAN's standard library. A standard ANSI "C" 80515-application programming interface library is available to help reduce design cycle time.

Memory Organization

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces.

Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (Flash), external data memory (physically consisting of XRAM, CE Data RAM, CE Program RAM and I/O RAM), and internal data memory (Internal RAM). Figure 5 shows the memory map (see also Table 54).

Internal and External Data Memory: Both internal and external data memory are physically located in the 71M6403 IC. External data memory is only meant to imply external to the 80515 MPU core.

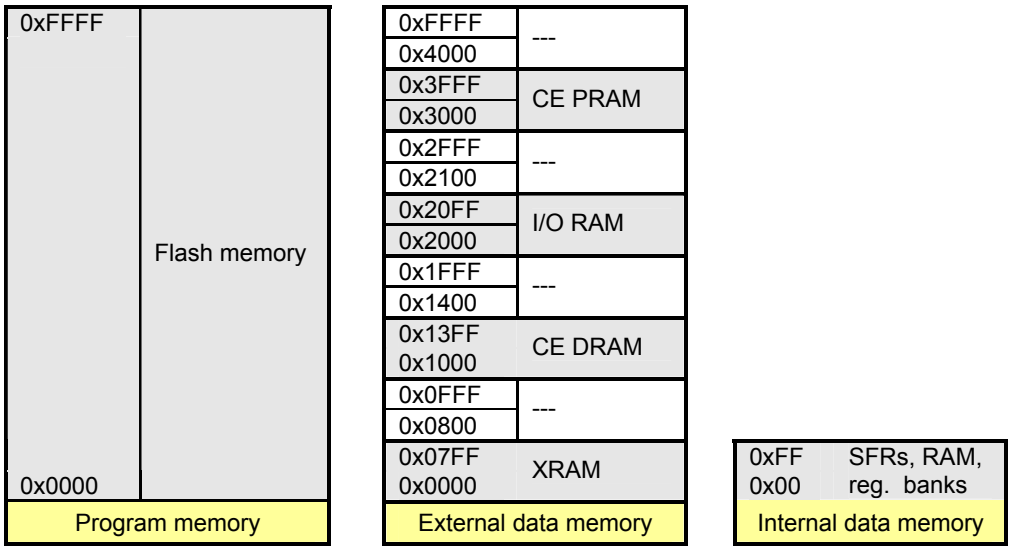


Figure 5: Memory Map

Program Memory: The 80515 can address up to 64KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation.

After reset, the MPU starts program execution from location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003.

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External Data Memory: While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 5 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction (SFR USR2 provides the upper 8 bytes for the MOVX A,@Ri instruction).

Clock Stretching: MOVX instructions can access fast or slow external RAM and external peripherals. The three low ordered bits of the CKCON register define the stretch memory cycles. Setting all the *CKCON* stretch bits to one allows access to very slow external RAM or external peripherals.

Table 3 shows how the signals of the External Memory Interface change when stretch values are set from 0 to 7. The widths of the signals are counted in MPU clock cycles. The post-reset state (001) of the CKCON register, which is in bold in the table, performs the MOVX instructions with a stretch value equal to 1.

CKCON register			Stretch Value	Read signals width		Write signal width	
CKCON.2	CKCON.1	CKCON.0		memaddr	memrd	memaddr	memwr
0	0	0	0	1	1	2	1
0	**0**	**1**	**1**	**2**	**2**	**3**	**1**
0	1	0	2	3	3	4	2
0	1	1	3	4	4	5	3
1	0	0	4	5	5	6	4
1	0	1	5	6	6	7	5
1	1	0	6	7	7	8	6
1	1	1	7	8	8	9	7

Table 3: Stretch Memory Cycle Width

Direct vs Paged Addressing: There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. The eight high-ordered bits of address are specified with the USR2 SFR. This method allows the user paged access (256 pages of 256 bytes each) to the full 64KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address. This form is faster and more efficient when accessing very large data arrays (up to 64 Kbytes), since no additional instructions are needed to set up the eight high ordered bits of address.

It is possible to mix the two MOVX types. This provides the user with four separate data pointers, two with direct access and two with paged access to the entire 64KB of external memory range.

Dual Data Pointer: The Dual Data Pointer accelerates the block moves of data. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located at the LSB of the DPS register (DPS.0). DPTR is selected when DPS.0 = 0 and DPTR1 is selected when DPS.0 = 1.

The user switches between pointers by toggling the LSB of the DPS register. All DPTR-related instructions use the currently selected DPTR for any activity.

The second data pointer may not be supported by certain compilers.

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Internal Data Memory: The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always 1 byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addressees 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 4 shows the internal data memory map.

<table>
<tr><th>Address</th><th>Direct addressing</th><th>Indirect addressing</th></tr>
<tr><td>0xFF</td><td rowspan="2">Special Function Registers (SFRs)</td><td rowspan="2">RAM</td></tr>
<tr><td>0x80</td></tr>
<tr><td>0x7F</td><td colspan="2" rowspan="2">Byte-addressable area</td></tr>
<tr><td>0x30</td></tr>
<tr><td>0x2F</td><td colspan="2" rowspan="2">Bit-addressable area</td></tr>
<tr><td>0x20</td></tr>
<tr><td>0x1F</td><td colspan="2" rowspan="2">Register banks R0…R7</td></tr>
<tr><td>0x00</td></tr>
</table>

Table 4: Internal Data Memory Map

Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 5.

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	***INTBITS***								**FF**
F0	*B*								**F7**
E8	***WDI***								**EF**
E0	*A*								**E7**
D8	*WDCON*								**DF**
D0	*PSW*								**D7**
C8									**CF**
C0	*IRCON*								**C7**
B8	*IEN1*	*IP1*	*S0RELH*	*S1RELH*				*USR2*	**BF**
B0			***FLSHCTL***					***PGADR***	**B7**
A8	*IEN0*	*IP0*	*S0RELL*						**AF**
A0	***P2***	***DIR2***	***DIR0***						**A7**
98	*S0CON*	*S0BUF*	*IEN2*	*S1CON*	*S1BUF*	*S1RELL*	***EEDATA***	***EECTRL***	**9F**
90	***P1***	***DIR1***	*DPS*		***ERASE***				**97**
88	*TCON*	*TMOD*	*TL0*	*TL1*	*TH0*	*TH1*	*CKCON*		**8F**
80	***P0***	*SP*	*DPL*	*DPH*	*DPL1*	*DPH1*	*WDTREL*	*PCON*	**87**

Table 5: Special Function Registers Locations

Only a few addresses are occupied, the others are not implemented. SFRs specific to the 71M6403 are shown in **bold** print. Any read access to unimplemented addresses will return undefined data, while any write access will have no effect.

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Special Function Registers (Generic 80515 SFRs)

Table 6 shows the location of the SFRs and the value they assume at reset or power-up.

Name	Location	Reset value	Description
P0	0x80	0xFF	Port 0
SP	0x81	0x07	Stack Pointer
DPL	0x82	0x00	Data Pointer Low 0
DPH	0x83	0x00	Data Pointer High 0
DPL1	0x84	0x00	Data Pointer Low 1
DPH1	0x85	0x00	Data Pointer High 1
WDTREL	0x86	0x00	Watchdog Timer Reload register
PCON	0x87	0x00	UART Speed Control
TCON	0x88	0x00	Timer/Counter Control
TMOD	0x89	0x00	Timer Mode Control
TL0	0x8A	0x00	Timer 0, low byte
TL1	0x8B	0x00	Timer 1, high byte
TH0	0x8C	0x00	Timer 0, low byte
TH1	0x8D	0x00	Timer 1, high byte
CKCON	0x8E	0x01	Clock Control (Stretch=1)
P1	0x90	0xFF	Port 1
DPS	0x92	0x00	Data Pointer select Register
S0CON	0x98	0x00	Serial Port 0, Control Register
S0BUF	0x99	0x00	Serial Port 0, Data Buffer
IEN2	0x9A	0x00	Interrupt Enable Register 2
S1CON	0x9B	0x00	Serial Port 1, Control Register
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte
P2	0xA0	0x00	Port 2
IEN0	0xA8	0x00	Interrupt Enable Register 0
IP0	0xA9	0x00	Interrupt Priority Register 0
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte
P3	0xB0	0xFF	Port 3
IEN1	0xB8	0x00	Interrupt Enable Register 1
IP1	0xB9	0x00	Interrupt Priority Register 1
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte
USR2	0xBF	0x00	User 2 Port, high address byte for MOVX@Ri
IRCON	0xC0	0x00	Interrupt Request Control Register
PSW	0xD0	0x00	Program Status Word
WDCON	0xD8	0x00	Baud Rate Control Register (only WDCON.7 bit used)
A	0xE0	0x00	Accumulator
B	0xF0	0x00	B Register

Table 6: Special Function Registers Reset Values

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Accumulator (ACC, A): ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to the accumulator as "A", not ACC.

B Register: The B register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Program Status Word (PSW):

MSB LSB

CV	AC	F0	RS1	RS	OV	-	P

Table 7: PSW Register Flags

Bit	Symbol	Function
PSW.7	CV	Carry flag
PSW.6	AC	Auxiliary Carry flag for BCD operations
PSW.5	F0	General purpose Flag 0 available for user. **Not to be confused with the F0 flag in the CE STATUS register.**
PSW.4	RS1	Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
PSW.3	RS0	
PSW.2	OV	Overflow flag
PSW.1	-	User defined flag
PSW.0	P	Parity flag, affected by hardware to indicate odd / even number of "one" bits in the Accumulator, i.e. even parity.

RS1/RS0	Bank selected	Location
00	Bank 0	(0x00 – 0x07)
01	Bank 1	(0x08 – 0x0F)
10	Bank 2	(0x10 – 0x17)
11	Bank 3	(0x18 – 0x1F)

Table 8: PSW bit functions

Stack Pointer (SP): The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer: The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter: The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory.

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Port Registers: The I/O ports are controlled by Special Function Registers *P0*, *P1*, and *P2*. The contents of the SFR can be observed on corresponding pins on the chip. Writing a '1' to any of the ports (see Table 9) causes the corresponding pin to be at high level (V3P3), and writing a '0' causes the corresponding pin to be held at low level (GND). The data direction registers *DIR0*, *DIR1*, and *DIR2* define individual pins as input or output pins (see the DIO section in On-Chip Resources for details.

Register	SFR Address	R/W	Description
P0	0x80	R/W	Register for port 0 read and write operations (pins DIO0…DIO7)
DIR0	0xA2	R/W	Data direction register for port 0. Setting a bit to 1 means that the corresponding pin is an output.
P1	0x90	R/W	Register for port 1 read and write operations (pins DIO8…DIO15)
DIR1	0x91	R/W	Data direction register for port 1.
P2	0xA0	R/W	Register for port 2 read and write operations (pins DIO16…DIO21)
DIR2	0xA1	R/W	Data direction register for port 2.

Table 9: Port Registers

All four ports on the chip are bi-directional. Each of them consists of a Latch (SFR 'P0' to 'P3'), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports if they are not used for alternate purposes.

Special Function Registers Specific to the 71M6403

Table 10 shows the location and description of the 71M6403-specific SFRs.

Register	Alternative Name	SFR Address	R/W	Description
ERASE	*FLSH_ERASE*	0x94	W	This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for *FLSH_ERASE* in order to initiate the appropriate Erase cycle (default = 0x00). 0x55 – Initiate Flash Page Erase cycle. Must be preceded by a write to *FLSH_PGADR* @ SFR 0xB7. 0xAA – Initiate Flash Mass Erase cycle. Must be preceded by a write to *FLSH_MEEN* @ SFR 0xB2 and the debug port must be enabled. Any other pattern written to FLSH_ERASE will have no effect.
PGADDR	*FLSH_PGADR*	0xB7	R/W	Flash Page Erase Address register containing the flash memory page address (page 0 thru 127) that will be erased during the Page Erase cycle (default = 0x00). Must be re-written for each new Page Erase cycle.
EEDATA		0x9E	R/W	I^2C EEPROM interface data register
EECTRL		0x9F	R/W	I^2C EEPROM interface control register. If the MPU wishes to write a byte of data to EEPROM, it places the data in *EEDATA* and then writes the 'Transmit' code to *EECTRL*. The write to *EECTRL* initiates the transmit sequence. See the section I2C Interface (EEPROM) for a description of the command and status bits available for *EECTRL*.

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FLSHCRL		0xB2	R/W W R/W R	Bit 0 (*FLSH_PWE*): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte is written to flash. Writes to this bit are inhibited when interrupts are enabled. Bit 1 (*FLSH_MEEN*): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle. Bit 6 (*SECURE*): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored. Bit 7 (*PREBOOT*): Indicates that the preboot sequence is active.
WDI		0xE8	R/W R/W	**Only byte operations on the whole WDI register should be used when writing**. The byte must have all bits set except the bits that are to be cleared. The multi-purpose register *WDI* contains the following bits: Bit 0 (*IE_XFER*): XFER Interrupt Flag: This flag monitors the XFER_BUSY interrupt. It is set by hardware and must be cleared by the interrupt handler Bit 1 (*IE_ZP8*): 0.8sec Interrupt Flag: This flag monitors the ZP8 0.8sec interrupt. It is set by hardware and must be cleared by the interrupt handler
INTBITS	INT0…INT6	0xF8	R	Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use. Refer to the External Interrupts description.

Table 10: Special Function Registers

Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the 64xx Software User's Guide (SUG).

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UART

The 71M6403 includes a UART (UART0) that can be programmed for general purpose communications. A second UART (UART1) is connected to the optical port, as described in the optical port description.

The UART is a dedicated 2-wire serial interface, which can communicate with an external host processor at up to 38,400 bits/s (with MPU clock = 1.2288MHz). The operation of each pin is as follows:

RX: Serial input data are applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first. The voltage applied at RX must not exceed 3.6V.

TX: This pin is used to output the serial data. The bytes are output LSB first.

The 71M6403 has several UART-related registers, which can be read and written. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38400 bps. Table 11 shows how the baud rates are calculated. Table 12 shows the selectable UART operation modes.

	Using Timer 1	Using Internal Baud Rate Generator
Serial Interface 0	$2^{smod} * f_{CKMPU} / (384 * (256-TH1))$	$2^{smod} * f_{CKMPU} / (64 * (2^{10}-S0REL))$
Serial Interface 1	N/A	$f_{CKMPU} / (32 * (2^{10}-S1REL))$

Note: S0REL and S1REL are 10-bit values derived by combining bits from the respective timer reload registers. SMOD is the SMOD bit in the SFR *PCON*. TH1 is the high byte of timer 1.

Table 11: Baud Rate Generation

	UART 0	UART 1
Mode 0	N/A	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator)
Mode 1	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1)	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator)
Mode 2	Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of f_{CKMPU}	N/A
Mode 3	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1)	N/A

Table 12: UART Modes

Note: Parity of serial data is available through the P flag of the accumulator. Seven-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. Seven-bit serial modes without parity can be simulated by setting bit 7 to a constant 1. 8-bit serial modes with parity can be simulated by setting and reading the 9^{th} bit, using the control bits S0CON3 and S1CON3 in the S0COn and S1CON SFRs.

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Serial Interface 0 Control Register (S0CON).

The function of the UART0 depends on the setting of the Serial Port Control Register S0CON.

MSB LSB

SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0

Table 13: The S0CON Register

Serial Interface 1 Control Register (S1CON).

The function of the serial port depends on the setting of the Serial Port Control Register S1CON.

MSB LSB

SM	-	SM21	REN1	TB81	RB81	TI1	RI1

Table 14: The S1CON register

Bit	Symbol	Function
S0CON.7	SM0	These two bits set the UART0 mode:
S0CON.6	SM1	
S0CON.5	SM20	Enables the inter-processor communication feature.
S0CON.4	REN0	If set, enables serial reception. Cleared by software to disable reception.
S0CON.3	TB80	The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)
S0CON.2	RB80	In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM20 is 0, RB80 is the stop bit. In Mode 0 this bit is not used. Must be cleared by software.
S0CON.1	TI0	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
S0CON.0	RI0	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

Mode	Description	SM0	SM1
0	N/A	0	0
1	8-bit UART	0	1
2	9-bit UART	1	0
3	9-bit UART	1	1

Table 15: The S0CON Bit Functions

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Bit	Symbol	Function
S1CON.7	SM	Sets the baud rate for UART1 SM: 0 — Mode A — 9-bit UART — variable SM: 1 — Mode B — 8-bit UART — variable
S1CON.5	SM21	Enables the inter-processor communication feature.
S1CON.4	REN1	If set, enables serial reception. Cleared by software to disable reception.
S1CON.3	TB81	The 9th transmitted data bit in Mode A. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)
S1CON.2	RB81	In Modes 2 and 3, it is the 9th data bit received. In Mode B, if sm21 is 0, rb81 is the stop bit. In Mode 0 this bit is not used. Must be cleared by software.
S1CON.1	TI1	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
S1CON.0	RI1	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

Table 16: The S1CON Bit Functions

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Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from certain DIO pins, see the DIO Ports chapter). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

Timer/Counter Mode Control register (TMOD):

MSB LSB

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				Timer 0			

Table 17: The TMOD Register

Bits TR1 and TR0 start their associated timers when set.

Bit	Symbol	Function
TMOD.7 TMOD.3	Gate	If set, enables external gate control (pin int0 or int1 for Counter 0 or 1, respectively). When int0 or int1 is high, and TRX bit is set (see TCON register), a counter is incremented every falling edge on t0 or t1 input pin
TMOD.6 TMOD.2	C/T	Selects Timer or Counter operation. When set to 1, a Counter operation is performed. When cleared to 0, the corresponding register will function as a Timer.
TMOD.5 TMOD.1	M1	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description.
TMOD.4 TMOD.0	M0	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description.

Table 18: TMOD Register Bit Description

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M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer with 5 lower bits in the TL0 or TL1 register and the remaining 8 bits in the TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are held at zero.
0	1	Mode 1	16-bit Counter/Timer.
1	0	Mode2	8-bit auto-reload Counter/Timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TL(x) overflows, a value from TH(x) is copied to TL(x).
1	1	Mode3	If Timer 1 M1 and M0 bits are set to '1', Timer 1 stops. If Timer 0 M1 and M0 bits are set to '1', Timer 0 acts as two independent 8-bit Timer/Counters.

Table 19: Timers/Counters Mode Description

Note: TL0 is affected by TR0 and gate control bits, and sets TF0 flag on overflow.
TH0 is affected by TR1 bit, and sets TF1 flag on overflow.

Timer/Counter Control Register (TCON)

MSB LSB

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 20: The TCON Register

Bit	Symbol	Function
TCON.7	TF1	The Timer 1 overflow flag is set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON.6	TR1	Timer 1 Run control bit. If cleared, Timer 1 stops.
TCON.5	TF0	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON.4	TR0	Timer 0 Run control bit. If cleared, Timer 0 stops.
TCON.3	IE1	Interrupt 1 edge flag is set by hardware when the falling edge on external pin int1 is observed. Cleared when an interrupt is processed.
TCON.2	IT1	Interrupt 1 type control bit. Selects either the falling edge or low level on input pin to cause an interrupt.
TCON.1	IE0	Interrupt 0 edge flag is set by hardware when the falling edge on external pin int0 is observed. Cleared when an interrupt is processed.
TCON.0	IT0	Interrupt 0 type control bit. Selects either the falling edge or low level on input pin to cause interrupt.

Table 21: The TCON Register Bit Functions

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Table 22 specifies the combinations of operation modes allowed for timer 0 and timer 1:

	Timer 1		
	Mode 0	**Mode 1**	**Mode 2**
Timer 0 - mode 0	YES	YES	YES
Timer 0 - mode 1	YES	YES	YES
Timer 0 - mode 2	Not allowed	Not allowed	YES

Table 22: Timer Modes

Timer/Counter Mode Control register (PCON):

MSB LSB

SMOD	--	--	--	--	--	--	--

Table 23: The PCON Register

The SMOD bit in the PCON register doubles the baud rate when set.

Bit	Symbol	Function
PCON.7	SMOD	

Table 24: PCON Register Bit Description

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WD Timer (Software Watchdog Timer)

The software watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After a reset, the watchdog timer is disabled and all registers are set to zero. The watchdog consists of a 16-bit counter (WDT), a reload register (WDTREL), prescalers (by 2 and by 16), and control logic. Once the watchdog is started, it cannot be stopped unless the internal reset signal becomes active.

Note: It is recommended to use the hardware watchdog timer instead of the software watchdog timer.

WD Timer Start Procedure: The WDT is started by setting the SWDT flag. When the WDT register enters the state 0x7CFF, an asynchronous WDTS signal will become active. The signal WDTS sets bit 6 in the IP0 register and requests a reset state. WDTS is cleared either by the reset signal or by changing the state of the WDT timer.

Refreshing the WD Timer: The watchdog timer must be refreshed regularly to prevent the reset request signal from becoming active. This requirement imposes an obligation on the programmer to issue two instructions. The first instruction sets WDT and the second instruction sets SWDT. The maximum delay allowed between setting WDT and SWDT is 12 clock cycles. If this period has expired and SWDT has not been set, WDT is automatically reset, otherwise the watchdog timer is reloaded with the content of the WDTREL register and WDT is automatically reset.

Special Function Registers for the WD Timer

Interrupt Enable 0 Register (IEN0):

MSB LSB

EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0

Table 25: The IEN0 Register

Bit	Symbol	Function
IEN0.6	WDT	Watchdog timer refresh flag. Set to initiate a refresh of the watchdog timer. Must be set directly before SWDT is set to prevent an unintentional refresh of the watchdog timer. WDT is reset by hardware 12 clock cycles after it has been set.

Table 26: The IEN0 Bit Functions

Note: The remaining bits in the IEN0 register are not used for watchdog control

Interrupt Enable 1 Register (IEN1):

MSB LSB

EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	

Table 27: The IEN1 Register

Bit	Symbol	Function
IEN1.6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset by the hardware 12 clock cycles after it has been set.

Table 28: The IEN1 Bit Functions

Note: The remaining bits in the IEN1 register are not used for watchdog control

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Interrupt Priority 0 Register (IP0):

MSB							LSB
--	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Table 29: The IP0 Register

Bit	Symbol	Function
IP0.6	WDTS	Watchdog timer status flag. Set when the watchdog timer was started. Can be read by software.

Table 30: The IP0 bit Functions

Note: The remaining bits in the IP0 register are not used for watchdog control

Watchdog Timer Reload Register (WDTREL):

MSB							LSB
7	6	5	4	3	2	1	0

Table 31: The WDTREL Register

Bit	Symbol	Function
WDTREL.7	7	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler
WDTREL.6 to WDTREL.0	6-0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

Table 32: The WDTREL Bit Functions

The WDTREL register can be loaded and read at any time.

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Interrupts

The 80515 provides 11 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (TCON, IRCON, and SCON). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs IEN0, IEN1, and IEN2.

External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 71M6403, such as the CE, DIO, EEPROM interface, comparators.

Interrupt Overview: When an interrupt occurs, the MPU will vector to the predetermined address as shown in Table 50. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction, "RETI". When an RETI is performed, the processor will return to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt will be acknowledged by hardware forcing an LCALL to the appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of the MPU when the interrupt occurs. If the MPU is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on the current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles to perform the LCALL.

Special Function Registers for Interrupts:

Interrupt Enable 0 register (IE0)

MSB LSB

EAL	WDT		ES0	ET1	EX1	ET0	EX0

Table 33: The IEN0 Register

Bit	Symbol	Function
IEN0.7	EAL	EAL=0 – disable all interrupts
IEN0.6	WDT	Not used for interrupt control
IEN0.5	-	
IEN0.4	ES0	ES0=0 – disable serial channel 0 interrupt
IEN0.3	ET1	ET1=0 – disable timer 1 overflow interrupt
IEN0.2	EX1	EX1=0 – disable external interrupt 1
IEN0.1	ET0	ET0=0 – disable timer 0 overflow interrupt
IEN0.0	EX0	EX0=0 – disable external interrupt 0

Table 34: The IEN0 Bit Functions

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Interrupt Enable 1 Register (IEN1)

MSB							LSB
	SWDT	EX6	EX5	EX4	EX3	EX2	

Table 35: The IEN1 Register

Bit	Symbol	Function
IEN1.7	-	
IEN1.6	SWDT	Not used for interrupt control
IEN1.5	EX6	EX6=0 – disable external interrupt 6
IEN1.4	EX5	EX5=0 – disable external interrupt 5
IEN1.3	EX4	EX4=0 – disable external interrupt 4
IEN1.2	EX3	EX3=0 – disable external interrupt 3
IEN1.1	EX2	EX2=0 – disable external interrupt 2
IEN1.0	-	

Table 36: The IEN1 Bit Functions

Interrupt Enable 2 register (IE2)

MSB							LSB
-	-	-	-	-	-	-	ES1

Table 37: The IEN2 Register

Bit	Symbol	Function
IEN2.0	ES1	ES1=0 – disable serial channel 1 interrupt

Table 38: The IEN2 Bit Functions

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Timer/Counter Control register (TCON)

MSB LSB

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 39: The TCON Register

Bit	Symbol	Function
TCON.7	TF1	Timer 1 overflow flag
TCON.6	TR1	Not used for interrupt control
TCON.5	TF0	Timer 0 overflow flag
TCON.4	TR0	Not used for interrupt control
TCON.3	IE1	External interrupt 1 flag
TCON.2	IT1	External interrupt 1 type control bit
TCON.1	IE0	External interrupt 0 flag
TCON.0	IT0	External interrupt 0 type control bit

Table 40: The TCON Bit Functions

Interrupt Request register (IRCON)

MSB LSB

		EX6	IEX5	IEX4	IEX3	IEX2	

Table 41: The IRCON Register

Bit	Symbol	Function
IRCON.7	-	
IRCON.6	-	
IRCON.5	IEX6	External interrupt 6 edge flag
IRCON.4	IEX5	External interrupt 5 edge flag
IRCON.3	IEX4	External interrupt 4 edge flag
IRCON.2	IEX3	External interrupt 3 edge flag
IRCON.1	IEX2	External interrupt 2 edge flag
IRCON.0	-	

Table 42: The IRCON Bit Functions

Note: Only TF0 and TF1 (timer 0 and timer 1 overflow flag) will be automatically cleared by hardware when the service routine is called (Signals T0ACK and T1ACK – port ISR – active high when the service routine is called).

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External Interrupts

The external interrupts are connected as shown in Table 43. The polarity of interrupts 2 and 3 is programmable in the MPU. Interrupts 2 and 3 should be programmed for falling sensitivity. The generic 8051 MPU literature states that interrupts 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 43.

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5). ZP8 has its own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 44). The ZP8 interrupt must be cleared by the MPU software. The ZP8 interrupt occurs every 853.4 msec.

External Interrupt	Connection	Polarity	Flag Reset
0	Digital I/O High Priority	see *DIO_Rx*	automatic
1	Digital I/O Low Priority	see *DIO_Rx*	automatic
2	Comparator 2 or 3	falling	automatic
3	Reserved		
4	Comparator 2 or 3	rising	automatic
5	EEPROM busy	falling	automatic
6	ZP8	falling	manual

Table 43: External MPU Interrupts

Interrupt 6 is edge-sensitive. The flag for the ZP8 interrupt is located in the *WDI* SFR (address 0xE8).

Enable Bit	Description
EX0	Enable external interrupt 0
EX1	Enable external interrupt 1
EX2	Enable external interrupt 2
EX3	Enable external interrupt 3
EX4	Enable external interrupt 4
EX5	Enable external interrupt 5
EX6	Enable external interrupt 6
EX_ZP8	Enable ZP8 interrupt

Flag Bit	Description
IE0	External interrupt 0 flag
IE1	External interrupt 1 flag
IEX2	External interrupt 2 flag
IEX3	External interrupt 3 flag
IEX4	External interrupt 4 flag
IEX5	External interrupt 5 flag
IEX6	External interrupt 6 flag
IE_ZP8	ZP8 interrupt flag

Table 44: Control Bits for External Interrupts

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Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 45:

Group			
0	External interrupt 0	Serial channel 1 interrupt	
1	Timer 0 interrupt	-	External interrupt 2
2	External interrupt 1	-	External interrupt 3
3	Timer 1 interrupt	-	External interrupt 4
4	Serial channel 0 interrupt	-	External interrupt 5
5	-	-	External interrupt 6

Table 45: Priority Level Groups

Each group of interrupt sources can be programmed individually to have one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level are received simultaneously, an internal polling sequence as per Table 49 determines which request is serviced first.

IEN enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5). ZP8 has its own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 44). Note, the ZP8 interrupt must be cleared by the MPU software.

Interrupt Priority 0 Register (IP0)

MSB LSB

--	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Table 46: The IP0 Register:

Note: WDTS is not used for interrupt control

Interrupt Priority 1 Register (IP1)

MSB LSB

-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0

Table 47: The IP1 Register:

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 48: Priority Levels

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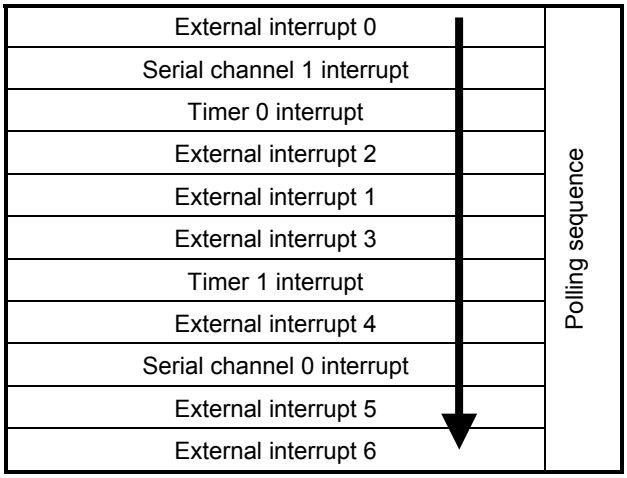


Table 49: Interrupt Polling Sequence

Interrupt Sources and Vectors

Table 50 shows the interrupts with their associated flags and vector addresses.

Interrupt Request Flag	Description	Interrupt Vector Address
IE0	External interrupt 0	0x0003
TF0	Timer 0 interrupt	0x000B
IE1	External interrupt 1	0x0013
TF1	Timer 1 interrupt	0x001B
RI0/TI0	Serial channel 0 interrupt	0x0023
RI1/TI1	Serial channel 1 interrupt	0x0083
IEX2	External interrupt 2	0x004B
IEX3	External interrupt 3	0x0053
IEX4	External interrupt 4	0x005B
IEX5	External interrupt 5	0x0063
IEX6	External interrupt 6	0x006B

Table 50: Interrupt Vectors

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On-Chip Resources

DIO Ports

The 71M6402 includes up to 22 pins of general purpose digital I/O. 18 of these pins are dual function and can alternatively be used as LCD drivers. Figure 6 shows a block diagram of the DIO section.

On reset or power-up, all DIO pins are inputs until they are configured for the desired direction. The pins are configured and controlled by the *DIO* and *DIO_DIR* registers (SFRs) and by the five bits of the I/O register *LCD_NUM* (0x2020[4:0]). See the description for *LCD_NUM* in the I/O RAM Section for a table listing the available segment pins versus DIO pins, depending on the selection for *LCD_NUM*. Generally, increasing the value for *LCD_NUM* will configure an increasing number of general purpose pins to be LCD segment pins, starting at the higher pin numbers.

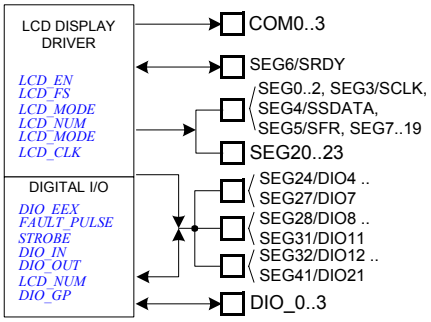


Figure 6: DIO Ports Block Diagram

Each pin declared as DIO can be configured independently as an input or output with the bits of the *DIO_DIRn* registers. Table 51 lists the direction registers and configurability associated with each group of DIO pins. Table 52 shows the configuration for a DIO pin through its associated bit in its *DIO_DIR* register.

DIO Pin Group	Type	MPU Port	Direction Register Name	Direction Register (SFR) Location	Data Register Name	Data Register (SFR) Location	Internal resources selectable when configured as DIO
DIO_0…DIO_3	DIO only	P0	*DIR0*	0xA2 [3:0]	*P0*	0x80 [3:0]	Yes
DIO 4…DIO7	Multi-use	P0		0xA2 [7:4]		0x80 [7:4]	Yes
DIO 8…DIO11	Multi-use	P1	*DIR1*	0x91 [3:0]	*P1*	0x90 [3:0]	Yes
DIO 12…DIO15	Multi-use	P1		0x91[7:4]		0x90[7:4]	No
DIO 16…DIO21	Multi-use	P2	*DIR2*	0xA1[5:0]	*P2*	0xA0[5:0]	No

Table 51: Direction Registers and Internal Resources for DIO Pin Groups

	***DIO_DIR* bit**	
	0	**1**
DIO Pin Function	input	output

Table 52: *DIO_DIR* Control Bit

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Values read from and written into the DIO ports use the data registers *P0*, *P1* and *P2*.

A 3-bit configuration word, I/O RAM register, *DIO_Rx* (0x2009[2:0] through 0x200E[6:4]) can be used for certain pins, when configured as DIO, to individually assign an internal resource such as an interrupt or a timer control (see Table 51 for DIO pins available for this option). This way, DIO pins can be tracked even if they are configured as outputs. This feature is useful for pulse counting. The control resources selectable for the DIO pins are listed in Table 53. If more than one input is connected to the same resource, the resources are combined using a logical OR.

***DIO_R* Value**	**Resource Selected for DIO Pin**
0	NONE
1	Reserved
2	T0 (counter0 clock)
3	T1 (counter1 clock)
4	High priority I/O interrupt (INT0 rising)
5	Low priority I/O interrupt (INT1 rising)
6	High priority I/O interrupt (INT0 falling)
7	Low priority I/O interrupt (INT1 falling)

Table 53: Selectable Controls using the *DIO_DIR* Bits

Additionally, if DIO6 and DIO7 are declared outputs, they can be configured as dedicated pulse outputs (STROBE = DIO6, FAULT_PULSE = DIO7) using the I/O RAM registers *DIO_PW* (0x2008[2]) and *DIO_PV* (0x2008[3]). In this case, DIO6 and DIO7 are under CE control. DIO4 and DIO5 can be configured to implement the EEPROM Interface by setting the I/O RAM register *DIO_EEX* (0x2008[4]).

Physical Memory

Data bus address space is allocated to on-chip memory as shown in Table 54.

Address (hex)	**Memory Technology**	**Memory Type**	**Typical Usage**	**Wait States (at 5MHz)**	**Memory Size (bytes)**
0000-FFFF	Flash Memory	Non-volatile	Program and non-volatile data	0	64KB
0000-07FF	Static RAM	Battery-buffered	MPU data XRAM,	0	2KB
1000-13FF	Static RAM	Volatile	CE data	5	1KB
2000-20FF	Static RAM	Volatile	configuration RAM (I/O RAM)	0	256
3000-3FFF	Static RAM	Volatile	CE Program code	5	4KB

Table 54: MPU Data Memory Map

Flash Memory: The 71M6403 includes 64KB of on-chip flash memory. The flash memory is intended to primarily contain MPU program code. In a typical application, it also contains images of the CE program code, CE coefficients, MPU RAM, and I/O RAM. On power-up, before enabling the CE, the MPU must copy these images to their respective memory locations.

The I/O RAM bit register *FLASH66Z* defines the pulse width for accessing flash memory. **To minimize supply current draw, this bit should be set to 1**.

Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

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The mass erase sequence is:

1. Write 1 to the *FLSH_MEEN* bit (SFR address 0xB2[1].
2. Write pattern 0xAA to *FLSH_ERASE* (SFR address 0x94)

Note: The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to *FLSH_PGADR* (SFR address 0xB7[7:1]
2. Write pattern 0x55 to *FLSH_ERASE* (SFR address 0x94)

The MPU may write to the flash memory. This is one of the non-volatile storage options available to the user. The I/O RAM register *FLSH_PWE* (flash program write enable, SFR B2[0]) differentiates 80515 data store instructions (MOVX@DPTR,A) between Flash and XRAM writes. Before setting *FLSH_PWE*, all interrupts need to be disabled by setting EAL =1.

Note: Flash write operations in the range 0x2000 to 0x20FF will also affect the I/O RAM. Thus, flash writes to this range have to be either avoided (code must jump around the affected range), or they must contain the data that the I/O RAM expects.

MPU RAM: The 71M6403 includes 2KB of static RAM memory on-chip (XRAM), which are backed-up by the battery plus 256-bytes of internal RAM in the MPU core. The 2KB of static RAM are used for data storage during normal MPU operations.

CE Data RAM: The CE DRAM is the data memory of the CE. The MPU can read and write the CE DRAM as the primary means of data communication between the two processors.

CE Program RAM: The CE PRAM is the program memory of the CE. The CE PRAM has to be loaded with CE code before the CE starts operating. CE PRAM cannot be accessed by the MPU when the CE is running.

Real-Time Clock (RTC)

The RTC is driven directly by an external clock signal provided at the CK38 pin. In the absence of the 3.3V supply, the RTC is powered by the external battery (VBAT pin). The RTC consists of a counter chain and output registers. The counter chain consists of seconds, minutes, hours, day of week, day of month, month, and year. The RTC is capable of processing leap years. Each counter has its own output register. Whenever the MPU reads the seconds register, all other output registers are automatically updated. Since the RTC clock is not coherent to the MPU clock, the MPU must read the seconds register multiple times until two consecutive reads are the same (requires either 2 or 3 reads). At this point, all RTC output registers will have the correct time. Regardless of the MPU clock speed, RTC reads require one wait state.

The RTC interrupt must be enabled using the I/O RAM register *EX_RTC* (address 0x2002[1]). RTC time is set by writing to the I/O RAM registers *RTC_SEC*, *RTC_MIN,* through *RTC_YR*. Each byte written to RTC must be delayed at least 3 CK38 cycles from any previous byte written to the RTC.

The RTC counter chain is designed for use with a 32.768 kHz clock source. The 71M6403 requires a 19.6608 MHz master clock for proper CE filter operation. The external (low cost) 'HC4040 counter generates an approximate clock frequency for the RTC. The 'HC4040's divide-by-512 output provides a 38.4 kHz clock signal. Therefore, the RTC runs about 17% faster using the 'HC4040. A divide-by-600 would generate the ideal 32.768 kHz clock from the 19.6608 MHz oscillator. Alternatively, a 32.768 kHz clock can be sourced independently from the system.

Two time-correction bits, the I/O RAM registers *RTC_DEC_SEC* (0x201C[1]) and *RTC_INC_SEC* (0x201C[0]) are provided to adjust the RTC time. A pulse on one of these bits causes the time to be decremented or incremented by an additional second at the next update of the *RTC_SEC* register. Thus, if the temperature coefficient of the clock source at the CK38 pin is known, the MPU firmware can integrate temperature and correct the RTC time as necessary as discussed in temperature compensation.

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Comparators (V2, INEUTRAL)

The 71M6403 includes two programmable comparators that are connected to the V2 (comparator 2) and INEUTRAL (comparator 3) pins. The I/O RAM register *COMP_INT* (0x2003[4:3]) allows the user to determine if comparators 2 and 3 will trigger an interrupt to the MPU. The output of each comparator is available in the *COMPSTAT* register. VBIAS is used as the threshold, and built-in hysteresis prevents each comparator from repeatedly responding to low-amplitude noise.

Comparators 2 and 3 can be used for early warning of power faults, or for monitoring of battery or other DC voltages. If they are both selected to interrupt the MPU, their outputs will be XORed together. The voltage at INEUTRAL is also available to the ADC in the AFE, but the comparator should not be used when INEUTRAL is used for analog measurements.

LCD Drivers

The 71M6403 contains 24 dedicated LCD segment drivers and an additional 18 multi-purpose pins which may be configured as additional LCD segment drivers (see I/O RAM register *LCD_NUM*). The 71M6403 is capable of driving between 96 to 168 pixels of LCD display with 25% duty cycle. At seven segments per digit, the LCD can be designed for 13 to 24 digits for display. Since each pixel is addressed individually, the LCD display can be a combination of alphanumeric digits and enunciator symbols. The information to be displayed is written into the lower four bits of I/O RAM registers *LCD_SEG0* through *LCD_SEG41*. Bit 0 corresponds to the segment selected when COM0 pin is active while bit 1 is allocated to COM1.

The LCD driver circuitry is grouped into 4 common outputs (COM0 to COM3) and up to 42 segment outputs (see Table 55). The typical LCD map is shown below.

	SEG0	SEG1	SEG2	SEG3	…	SEG30	…	SEG41
COM0	P0	P4	P8	P12	...	P108	...	P164
COM1	P1	P5	P9	P13	…	P109	...	P165
COM2	P2	P6	P10	P14	...	P110	...	P166
COM3	P3	P7	P11	P15	...	P111	...	P167

Table 55: Liquid Crystal Display Segment Table (Typical)

Note: P0, P1, … Represent the pixel/segment numbers on the LCD.

A charge pump suitable for driving VLCD is included on-chip. This circuit creates 5V from the 3.3V supply. A contrast DAC is provided that permits the LCD full-scale voltage to be adjusted between VLCD and 70% of VLCD. The *LCD_NUM* register defines the number of dual purpose pins used for LCD segment interface.

LCD Voltage Boost Circuitry

A voltage boost circuit may be used to generate 5V from the 3.3V supply to support low-power 5V devices, such as LCDs. Figure 7 shows a block diagram of the voltage boost circuitry including the voltage regulators for V2P5 and V2P5NV. When activated using the I/O RAM register *LCD_BSTEN* (0x2020[7]), the boost circuitry provides an AC voltage at the VDRV output pin (see the Applications section for details).

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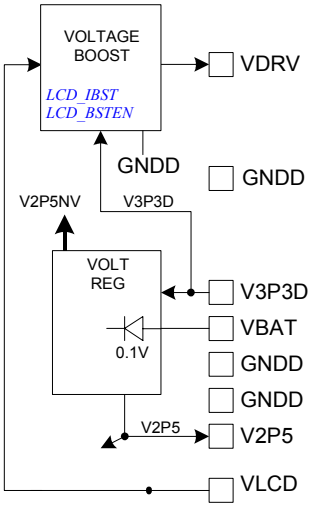


Figure 7: LCD Voltage Boost Circuitry

UART (UART0) and Optical Port (UART1)

The 71M6403 includes an interface to implement an IR or optical port. The pin OPT_TX is designed to directly drive an external LED for transmitting data on an optical link (low-active). The pin OPT_RX, also low-active, is designed to sense the input from an external photo detector used as the receiver for the optical link. These two pins are connected to a dedicated UART port. OPT_TX can be tristated if it is desired to multiplex another I/O pin to the OPT_TX output. The control bit for the OPT_TX output is the I/O RAM register *OPT_TXDIS* (0x2008[5]).

Hardware Reset Mechanisms

Several conditions will cause a hardware reset of the 71M6403:

- Voltage at the RESETZ pin low
- Voltage at the E_RST pin low

Reset Pin (RESETZ)

When the RESETZ pin is pulled low, all digital activity in the chip stops while analog circuits are still active. Additionally, all I/O RAM bits are cleared.

Hardware Watchdog Timer

In addition to the basic software watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, hardware watchdog timer (WDT) is included in the 71M6403. This timer will reset the MPU if it is not refreshed periodically, and can be used to recover the MPU in situations where program control is lost.

The watchdog timer uses the RTC clock source as its time base and requires a reset under MPU program control at least every 1.3 (for CK38 = 38.4 kHz) seconds. When the WDT overflow occurs, the MPU is momentarily reset as if RESETZ were pulled low for half of a clock cycle. Thus, after 4100 cycles of CK38, the MPU program will be launched from address 00.

An I/O RAM register status bit, *WD_OVF* (0x2002[2]), is set when WDT overflow occurs. This bit is powered by the VBAT pin and can be read by the MPU to determine if the part is initializing after a WDT overflow event or after a power up. After reading this bit, MPU firmware must clear *WD_OVF*. The *WD_OVF* bit is also cleared by the RESETZ pin.

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Because the watchdog timer uses CK38 as its clock reference, if the CK clock signal stops or slows down, *WD_OVF* is set and a system reset will be performed when the CK clock resumes.

In normal operation, the WDT is reset by periodically writing a one to the *WDT_RST* bit. The watchdog timer is also reset when WAKE=0 and, during development, when a 0x14 command is received from the ICE port.

There is no internal digital state that deactivates the WDT. For debug purposes, the WDT can be disabled by tying the V1 pin to V3P3. This also deactivates the power fault detection implemented with V1. Since there is no way in firmware to disable the WDT, it is guaranteed that whatever state the MPU might find itself in, it will be reset to a known state upon watchdog timer overflow.

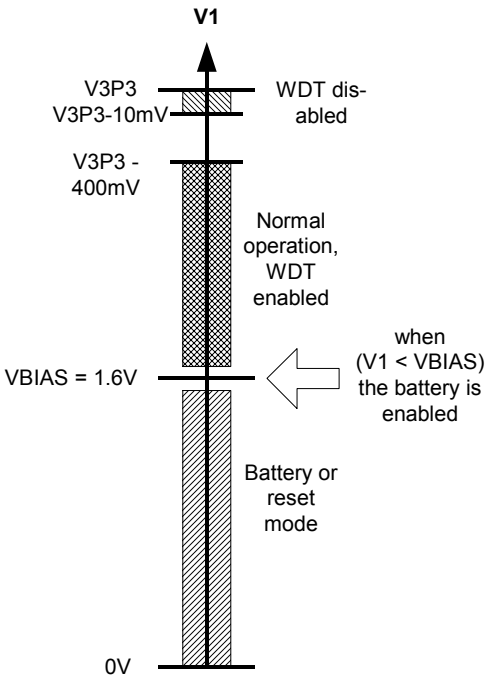


Figure 8: V1 Input Voltage Thresholds

Internal Voltages (VBIAS and V2P5)

The 71M6403 requires two supply voltages, V3P3A, for the analog section, and V3P3D, for the digital section. Both voltages can be tied together outside the chip. The internal supply voltage V2P5 is generated by an internal regulator from the 3.3V supplies.

VBIAS (1.6V) is generated internally and is used by the comparators V2 and INEUTRAL.

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Internal Clocks and Clock Dividers

All internal clocks are based on CK. This frequency is divided by 4 to generate 4.9152MHz, the frequency supplied to the ADC, the FIR filter (CKFIR), the CE DRAM and the clock generator. The clock generator provides two clocks, one for the MPU (CKMPU) and one for the CE (CKCE).

The MPU clock frequency is determined by the I/O RAM register *MPU_DIV* (0x2004[2:0]) and can be $CE*2^{-MPU_DIV}$ Hz where *MPU_DIV* varies from 0 to 7 (*MPU_DIV* is 0 on power-up). This makes the MPU clock scalable from 4.9152MHz down to 38.4kHz. The circuit also generates a 2x MPU clock for use by the emulator. This clock is not generated when the I/O RAM register *ECK_DIS* (0x2005[5]) is asserted by the MPU.

I^2C Interface (EEPROM)

A dedicated 2-pin serial interface implements an I^2C driver that can be used to communicate with external EEPROM devices (type 24C1024). The I^2C interface can be enabled onto the DIO pins DIO4 (SCK) and DIO5 (SDA) by setting the I/O RAM register *DIO_EEX* (0x2008[4]). The MPU communicates with the interface through two SFR registers: *EEDATA* (0x9E) and *EECTRL* (0x9F). If the MPU wishes to write a byte of data to the EEPROM, it places the data in *EEDATA* and then writes the 'Transmit' code to *EECTRL*. The write to *EECTRL* initiates the transmit sequence. By observing the *BUSY* bit in *EECTRL* the MPU can determine when the transmit operation is finished (i.e. when the *BUSY* bit transitions from 1 to 0). INT5 is also asserted when *BUSY* falls. The MPU can then check the *RX_ACK* bit to see if the EEPROM acknowledged the transmission.

A byte is read by writing the 'Receive' command to *EECTRL* and waiting for *BUSY* to fall. Upon completion, the received data will appear in *EEDATA*. The serial transmit and receive clock is 78kHz during each transmission, and SCL is held in a high state until the next transmission. The bits in *EECTRL* are shown in Table 56. The EEPROM interface can also be operated by controlling the DIO4 and DIO5 pins directly.

Note: Clock stretching and multi-master operation is not supported for the I^2C interface.

<table>
<tr><th>Status Bit</th><th>Name</th><th>Read/ Write</th><th>Polarity</th><th>Description</th></tr>
<tr><td>7</td><td>ERROR</td><td>R</td><td>High</td><td>Asserted when an illegal command is received.</td></tr>
<tr><td>6</td><td>BUSY</td><td>R</td><td>High</td><td>Asserted when serial data bus is busy.</td></tr>
<tr><td>5</td><td>RX_ACK</td><td>R</td><td>High</td><td>Indicates that the EEPROM sent an ACK bit.</td></tr>
<tr><td>4</td><td>TX_ACK</td><td>R</td><td>High</td><td>Indicates when an ACK bit has been sent to the EEPROM</td></tr>
<tr><td>3-0</td><td>CMD[3:0]</td><td>W</td><td>See CMD Table</td><td>
<table>
<tr><th>CMD</th><th>Operation</th></tr>
<tr><td>0</td><td>No-op. Applying the no-op command will stop the I^2C clock (SCK, DIO4). Failure to issue the no-op command will keep the SCK signal toggling.</td></tr>
<tr><td>2</td><td>Receive a byte from EEPROM and send ACK.</td></tr>
<tr><td>3</td><td>Transmit a byte to EEPROM</td></tr>
<tr><td>5</td><td>Issue a 'STOP' sequence</td></tr>
<tr><td>6</td><td>Receive the last byte from EEPROM and don't send ACK.</td></tr>
<tr><td>9</td><td>Issue a 'START' sequence</td></tr>
<tr><td>Others</td><td>No Operation, assert ERROR bit</td></tr>
</table>
</td></tr>
</table>

Table 56: *EECTRL* Status Bits

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Test Ports

TMUXOUT Pin: One out of 16 digital or 4 analog signals can be selected to be output on the TMUXOUT pin. The function of the multiplexer is controlled with the I/O RAM register *TMUX* (0x2000[3:0]), as shown in Table 57.

TMUX[3:0]	Mode	Function
0	analog	DGND
1	analog	IBIAS
2	analog	Reserved for production test
3	analog	VBIAS
4	digital	RTM (Real time output from CE)
5	digital	Reserved for production test
6	digital	V2_OK (Comparator 2 Output)
7	digital	INEUTRAL_OK (Comparator 3 Output)
8	digital	RXD (from Optical interface)
9	digital	MUX_SYNC
A	digital	CK_10M
B	digital	CK_MPU
C	--	reserved for production test
D	digital	CK38
E	digital	Reserved
F	digital	Reserved

Table 57: *TMUX[3:0]* Selections

Emulator Port: The emulator port, consisting of the pins E_RST, E_TCLK and E_RXTX provides control of the MPU through an external in-circuit emulator. The E_TBUS[3:0] pins, together with the E_ISYNC/BRKRQ add trace capability to the emulator. The emulator port is compatible with the ADM51 emulators manufactured by Signum Systems.

The signals of the emulator port have weak pull-ups. Adding 3kΩ pull-up resistors on the PCB is recommended.

Real-Time Monitor: The RTM output of the CE is available as one of the digital multiplexer options. RTM data is read from the CE DRAM locations specified by I/O RAM registers *RTM0*, *RTM1*, *RTM2*, and *RTM3* after the rise of MUX_SYNC. The RTM can be enabled and disabled with I/O RAM register *RTM_EN*. The RTM output is clocked by CK/4. Each RTM word is clocked out in 35 cycles and contains a leading flag bit. Figure 9 in the System Timing Section illustrates the RTM output format. RTM is low when not in use.

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Synchronous Serial Interface (SSI): A high-speed serial interface with handshake capability is available to send a contiguous block of CE data to an external data logger or DSP. The block of data, configurable as to location and size, is sent starting 1 cycle of 32kHz before each CE code pass begins. If the block of data is big enough such that transmission has not completed when the code pass begins, it will complete during the CE code pass with no timing impact to the CE or the serial data. In this case, care must be taken that the transmitted data is not modified unexpectedly by the CE. The SSI interface is enabled by the *SSI_EN* bit and consists of SCLK, SSDATA, and SFR as outputs and, optionally, SRDY as input. The interface is compatible with 16bit and 32bit processors. The operation of each pin is as follows:

SCLK is the serial clock. The clock can be 5MHz or 10MHz, as specified by the *SSI_10M* bit. The *SSI_CKGATE* bit controls whether SCLK runs continuously or is gated off when no SSI activity is occurring. If SCLK is gated, it will begin 3 cycles before SFR rises and will persist 3 cycles after the last data bit is output.

The pins used for the SSI are multiplexed with the LCD segment outputs, as shown in Table 58. **Thus, the LCD should be disabled when the SSI is in use.**

SSI Signal	LCD Segment Output Pin
SCLK	SEG3
SSDATA	SEG4
SFR	SEG5
SRDY	SEG6

Table 58: SSI Pin Assignment

SRDY is an optional handshake input that indicates that the DSP or data-logging device is ready to receive data. SRDY must be high to enable SFR to rise and initiate the transfer of the next field. It is expected that SRDY changes state on the rising edges of SCLK. If SRDY is not high when the SSI port is ready to transmit the next field, transmission will be delayed until it is. SRDY is ignored except at the beginning of a field transmission. If SRDY is not enabled (by *SSI_RDYEN*), the SSI port will behave as if SRDY is always one.

SSDATA is the serial output data. SSDATA changes on the rising edge of SCLK and outputs the contents of a block of CE RAM words starting with address *SSI_STRT* and ending with *SSI_END*. The words are output MSB first.

The field size is set with the *SSI_FSIZE* register: 0 entire data block, 1-8 bit fields, 2-16 bit fields, 3-32 bit fields. The polarity of the SFR pulse can be inverted with *SSI_FPOL*. If SRDY does not delay it, the first SFR pulse in a frame will rise on the third SCLK after MUX_SYNC (fourth SCLK if 10MHz). MUX_SYNC can be used to synchronize the fields arriving at the data logger or DSP.

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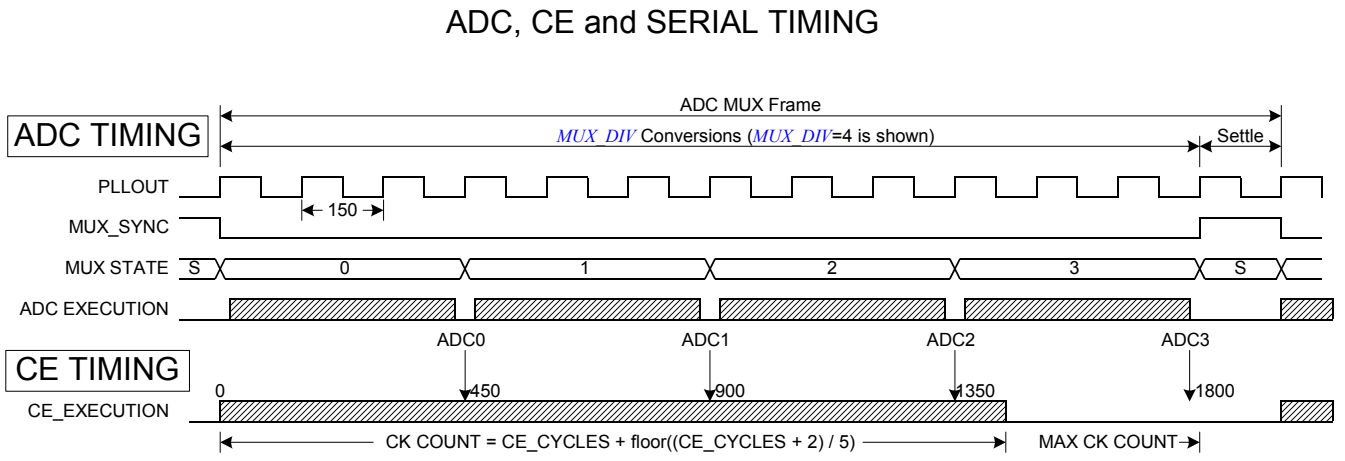
FUNCTIONAL DESCRIPTION

System Timing Summary

Figure 9 summarizes the timing relationships between the input MUX states. In this example, *MUX_DIV*=0 (six mux states) and *FIR_LEN* = 0 (2 PLLOUT cycles). Since FIR filter conversions require two or three PLLOUT cycles, the duration of each MUX cycle is 1 + 2 * states defined by *MUX_DIV* if *FIR_LEN* = 0, and 1 + 3 * states defined by *MUX_DIV* if *FIR_LEN* = 1. Followed by the conversions is a single PLLOUT cycle.

Each CE program pass begins when MUX_SYNC falls. Depending on the length of the CE program, it may continue running until the end of the ADC5 conversion. CE opcodes are constructed to ensure that all CE code passes consume exactly the same number of cycles. The result of each ADC conversion is inserted into the CE DRAM when the conversion is complete. The CE code is designed to tolerate sudden changes in ADC data. The exact CK count when each ADC value is loaded into DRAM is shown in Figure 9.

Figure 9 also shows that the two serial data streams, RTM and SSI, begin transmitting at the beginning of MUX_SYNC. RTM, consisting of 140 CK cycles, will always finish before the next code pass starts. The SSI port begins transmitting at the same time as RTM, but may significantly overrun the next code pass if a large block of data is required. Neither the CE nor the SSI port will be affected by this overlap.



NOTES:

1. ALL DIMENSIONS ARE 5MHZ CK COUNTS.
2. THE PRECISE FREQUENCY OF CK COUNTS IS 150*CRYSTAL FREQUENCY = 4.9152MHz.

Figure 9: Timing Relationship between ADC MUX, CE, and Serial Transfers

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Figure 10, Figure 11, and Figure 12 show the RTM and SSI timing, respectively.

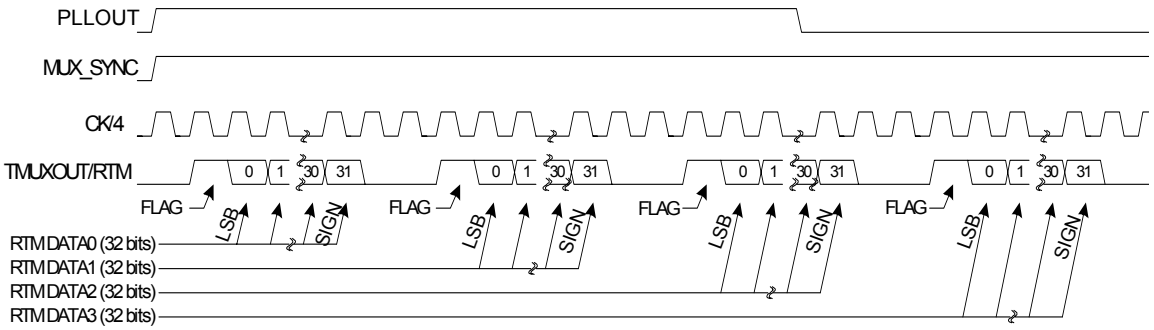


Figure 10: RTM Output Format

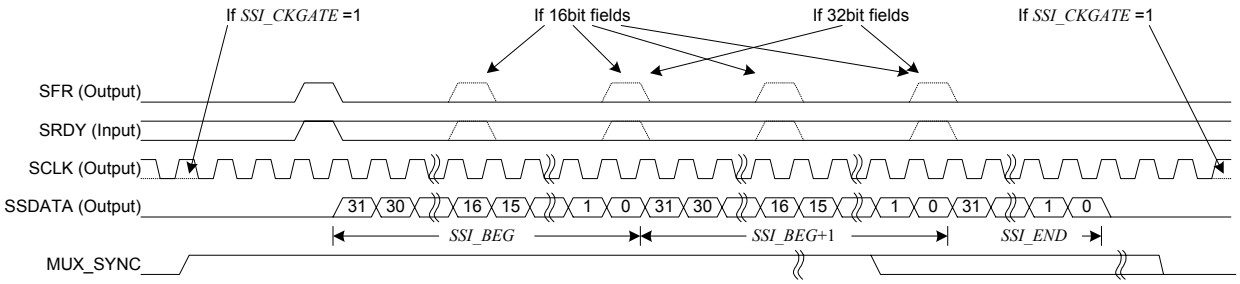


Figure 11: SSI Timing, (*SSI_FPOL* = *SSI_RDYPOL* = 0)

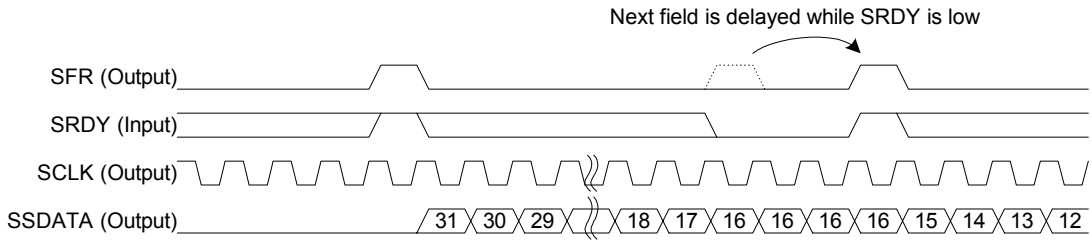


Figure 12: SSI Timing, 16-bit Field Example (External Device Delays SRDY)

SFR is the framing pulse. Although CE words are always 32 bits, the SSI interface will frame the entire data block as a single field, as multiple 16-bit fields, or as multiple 32-bit fields. The SFR pulse is one SCLK clock cycle wide, changes state on the rising edge of SCLK and precedes the first bit of each field.

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Data Flow

The data flow between CE and MPU is shown in Figure 13. In a typical application, the 32-bit compute engine (CE) sequentially processes the samples from the inputs on pins I0 through I5, performing calculations to measure the currents for circuit breaker operation. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

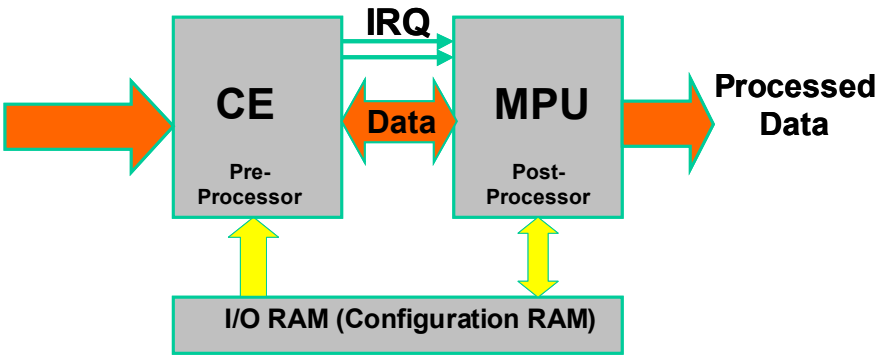


Figure 13: MPU/CE Data Flow

CE/MPU Communication

Figure 14 shows the functional relationship between CE and MPU. The CE is controlled by the MPU via shared registers in the I/O RAM and by registers in the CE DRAM.

Figure 15 shows the sequence of events between CE and MPU upon reset or power-up. In a typical application, the sequence of events is as follows:

1) Upon power-up, the MPU initializes the hardware, including disabling the CE
2) The MPU loads the code for the CE into the CE PRAM
3) The MPU loads CE data into the CE DRAM.
4) The MPU starts the CE by setting the *CE_EN* bit in the I/O RAM.
5) The CE then repetitively executes its code, generating results and storing them in the CE DRAM

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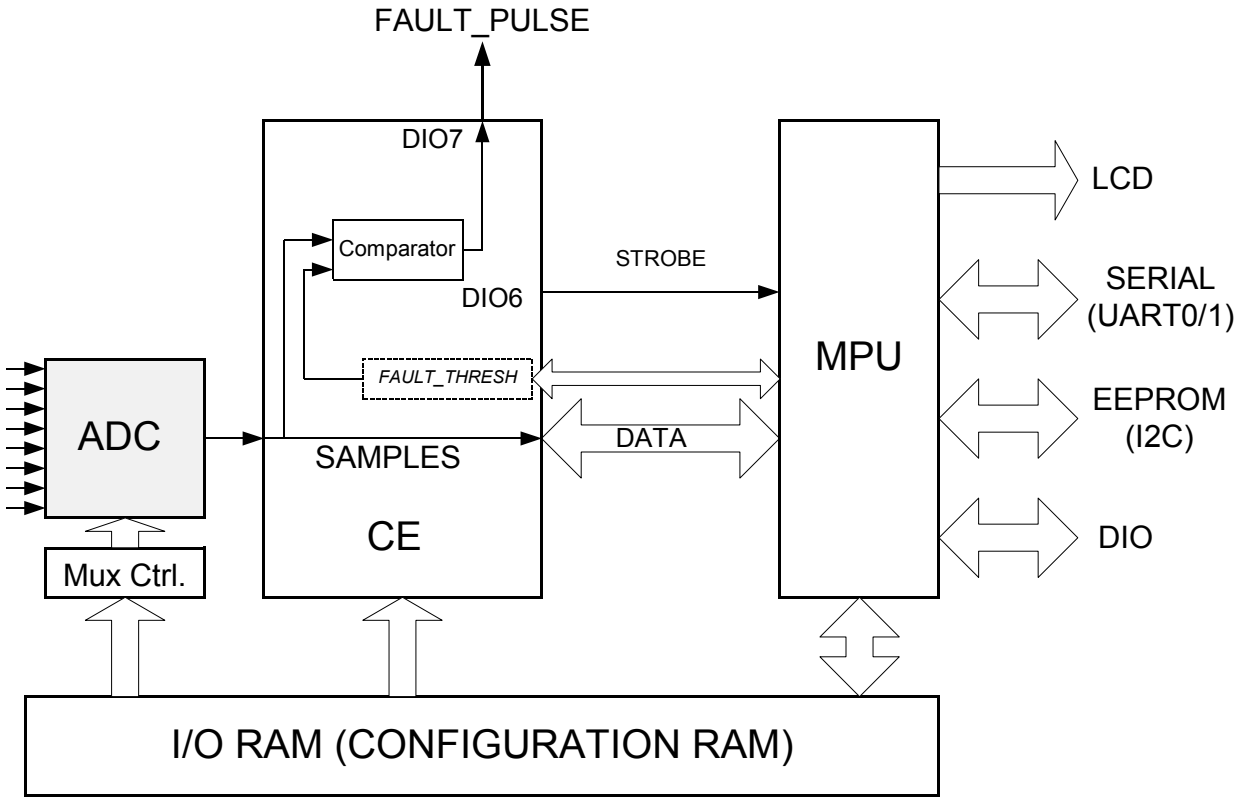


Figure 14: MPU/CE Communication (Functional)

The MPU will wait for the CE to signal that fresh data is ready (the XFER interrupt). It will read the data and perform additional processing.

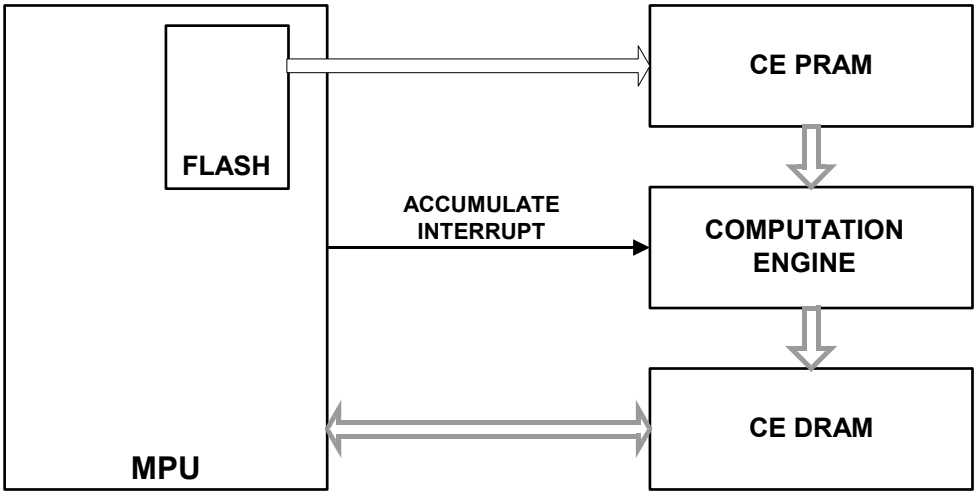


Figure 15: MPU/CE Communication (Processing Sequence)

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Fault, Reset, Power-Up

Reset Mode: When the RESETZ pin is pulled low, all digital activity in the chip stops while analog circuits are still active. Additionally, all I/O RAM bits are cleared..

When RESETZ goes high the MPU will begin executing its preboot and boot sequences from address 00. See the security section for more description of preboot and boot.

Chopping Circuitry

As explained in the hardware section, the bits of the I/O RAM register *CHOP_ENA[1:0]* have to be toggled in between multiplexer cycles to achieve the desired elimination of DC offset.

The amplifier within the reference is auto-zeroed by means of an internal signal that is controlled by the *CHOP_EN* bits. When this signal is HIGH, the connection of the amplifier inputs is reversed. This preserves the overall polarity of the amplifier gain but inverts the input offset. By alternately reversing the connection, the offset of the amplifier is averaged to zero. The function of the two bits of the *CHOP_EN* register are described in Table 59.

CHOP_EN[1]	*CHOP_EN[0]*	Function
0	0	Toggle chop signal
0	1	Reference connection positive
1	0	Reference connection reversed
1	1	Toggle chop signal

Table 59: *CHOP_EN* Bits

For automatic chopping, the *CHOP_EN* bits are set to either 00 or 11. In this mode, the polarity of the signals feeding the reference amplifier will be automatically toggled for each multiplexer cycle as shown in Figure 16. With an even number of multiplexer cycles in each accumulation interval, the number of cycles with positive reference connection will equal the number of cycles with reversed connection, and the offset for each sampled signal will be averaged to zero. This sequence is acceptable when only the primary signals (circuit breaker voltage, circuit breaker current) are of interest.

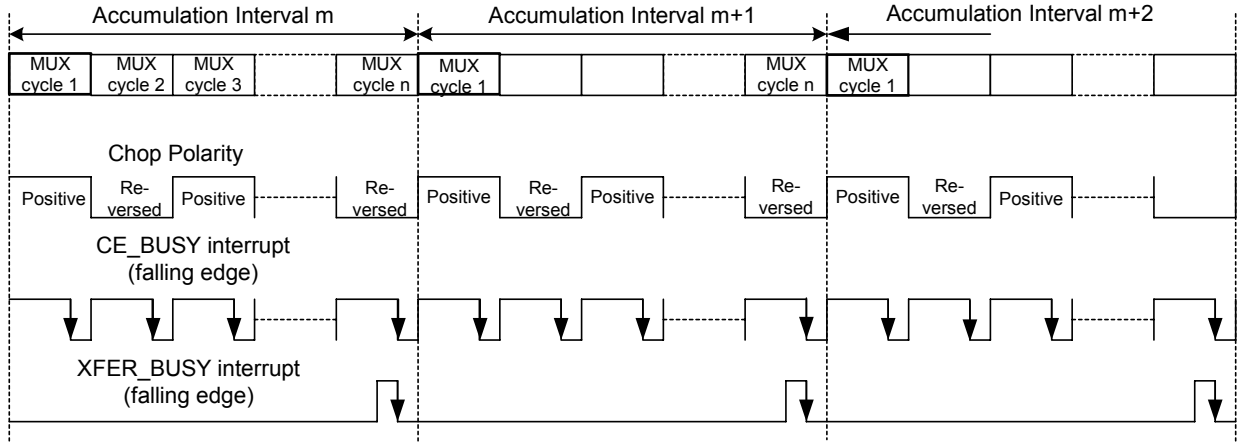


Figure 16: Chop Polarity w/ Automatic Chopping

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Program Security

When enabled, the security feature limits the ICE to global flash erase operations only. All other ICE operations are blocked. This guarantees the security of the user's MPU and CE program code. Security is enabled by MPU code that is executed in a 32 cycle preboot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the flash memory, followed by a chip reset. Global flash erase also clears the CE PRAM.

The first 32 cycles of the MPU boot code are called the preboot phase because during this phase the ICE is inhibited. A read-only status bit, *PREBOOT* (SFR 0xB2[7]), identifies these cycles to the MPU. Upon completion of the preboot sequence, the ICE can be enabled and is permitted to take control of the MPU.

SECURE (SFR 0xB2[6]), the security enable bit, is reset whenever the MPU is reset. Hardware associated with the bit permits only ones to be written to it. Thus, preboot code may set *SECURE* to enable the security feature but may not reset it. Once *SECURE* is set, the preboot code is protected and no external read of program code is possible.

Specifically, when *SECURE* is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's preboot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases CE program RAM whether *SECURE* is set or not.
- Writes to page zero, whether by MPU or ICE, are inhibited.

Additionally, by setting the I/O RAM register *ECK_DIS* to 1, the emulator clock is disabled, inhibiting access to the program with the emulator.

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FIRMWARE INTERFACE

I/O RAM MAP – In Numerical Order

'Not Used' bits are blacked out and contain no memory and are read by the MPU as zero. *RESERVED* bits are in use and should not be changed.

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration:									
CE0	2000	*EQU* [1]			*CE_EN*	*TMUX[3:0]*			
CE1	2001	*PRE_SAMPS[1:0]*		*SUM_CYCLES[5:0]*					
CE2	2002	*MUX_DIV[1:0]*		*CHOP_EN[1:0]*		*RTM_EN*	*WD_OVF*	*EX_ZP8*	*EX_XFR*
COMP0	2003				*COMP_INT[1:0]*		*COMP_STAT[2:0]*		
CONFIG0	2004	*VREF_CAL*		*RESERVED*	*Reserved* [2]	*VREF_DIS*	*MPU_DIV*		
CONFIG1	2005	*RESERVED*		*ECK_DIS*	*FIR_LEN*	*ADC_DIS*	*MUX_ALT*	*FLASH66Z*	*MUX_E*
VERSION	2006	*VERSION[7:0]*							
Digital I/O:									
DIO0	2008			*OPT_TXDIS*	*DIO_EEX*	*DIO_STR*	*DIO_FLT*		
DIO1	2009		*DIO_R1[2:0]*				*DIO_R0[2:0]*		
DIO2	200A		*DIO_R3[2:0]*				*DIO_R2[2:0]*		
DIO3	200B		*DIO_R5[2:0]*				*DIO_R4[2:0]*		
DIO4	200C		*DIO_R7[2:0]*				*DIO_R6[2:0]*		
DIO5	200D		*DIO_R9[2:0]*				*DIO_R8[2:0]*		
DIO6	200E		*DIO_R11[2:0]*				*DIO_R10[2:0]*		
LCD Display Interface:									
LCDX	2020	*LCD_BSTEN*			*LCD_NUM[4:0]*				
LCDY	2021			*LCD_EN*	*LCD_MODE[2:0]*			*LCD_CLK[1:0]*	
LCDZ	2022				*LCD_FS[4:0]*				
LCD0	2030					*LCD_SEG0[3:0]*			
LCD1	2031					*LCD_SEG1[3:0]*			
LCD2	2032					*LCD_SEG2[3:0]*			
LCD3	2033					*LCD_SEG3[3:0]*			
…	…			...		...			
LCD39	2057					*LCD_SEG39[3:0]*			
LCD40	2058					*LCD_SEG40[3:0]*			
LCD41	2059					*LCD_SEG41[3:0]*			

Note 1: Set EQU = 101.

Note 2: Set bit 2004:4 to 0.

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RTM Probes:								
RTM0	2060	*RTM0[7:0]*						
RTM1	2061	*RTM1[7:0]*						
RTM2	2062	*RTM2[7:0]*						
RTM3	2063	*RTM3[7:0]*						
Synchronous Serial Interface:								
SSI	2070	*SSI_EN*	*SSI_10M*	*SSI_CKGATE*	*SSI_FSIZE[1:0]*	*SSI_FPOL*	*SSI_RDYEN*	*SSI_RDYPOL*
SSI_BEG	2071	*SSI_BEG[7:0]*						
SSI_END	2072	*SSI_END[7:0]*						
Fuse Selection Registers:								
TRIMSEL	20FD	*TRIMSEL[7:0]*						
TRIM	20FF	*TRIM[7:0]*						

SFR MAP (SFRs Specific to TERIDIAN 80515) – In Numerical Order

'Not Used' bits are blacked out and contain no memory and are read by the MPU as zero. *RESERVED* bits are in use and should not be changed. This table lists only the SFR registers that are not generic 8051 SFR registers.

Name	SFR Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Digital I/O:									
P0	80	*DIO_0[7:0]* (Port 0)							
DIR0	A2	*DIO_DIR0[7:0]*							
P1	90	*DIO_1[7:0]* (Port 1)							
DIR1	91	*DIO_DIR1[7:0]*							
P2	A0			*DIO_2[5:0]* (Port 2)					
DIR2	A1			*DIO_DIR2[5:0]*					
Interrupts and WD Timer:									
INTBITS	F8		*INT6*	*INT5*	*INT4*	*INT3*	*INT2*	*INT1*	*INT0*
WDI	E8	*WD_RST*						*IE_ZP8*	*IE_XFER*
Flash:									
ERASE	94	*FLSH_ERASE[7:0]*							
FLSHCTL	B2	*PREBOOT*	*SECURE*					*FLSH_MEEN*	*FLSH_PWE*
PGADR	B7	*FLSH_PGADR[6:0]*							
Serial EEPROM:									
EEDATA	9E	*EEDATA[7:0]*							
EECTRL	9F	*EECTRL[7:0]*							

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I/O RAM (Configuration RAM) – Alphabetical Order

Many functions of the chip can be controlled via the I/O RAM (Configuration RAM). The CE will also take some of its parameters from the I/O RAM.

Bits with a W (write) direction are written by the MPU into I/O RAM. Typically, they are initially stored in flash memory and copied to the I/O RAM by the MPU. Some of the more frequently programmed bits are mapped to the MPU SFR memory space. The remaining bits are mapped to 2xxx. Bits with R (read) direction can only be read by the MPU. **On power up, all bits are cleared to zero unless otherwise stated.** Generic SFR registers are not listed.

Name	Location [Bit(s)]	Dir	Description
ADC_DIS	2005[3]	R/W	Disables ADC and removes bias current
CE_EN	2000[4]	R/W	CE enable.
CHOP_EN[1:0]	2002[5:4]	R/W	Chop enable for the reference band gap circuit. 00: enabled 01: disabled 10: disabled 11: enabled
RESERVED	2004[5]	R/W	Must be 0.
COMP_INT[1:0]	2003[4:3]	R/W	Two bits establishing whether a comparator state change should create MPU interrupts. 1: interrupt, 0: no interrupt. If 11, the comparator outputs are XOR'ed. Bit0 = comp2, Bit1 = comp3
COMP_STAT[2:0]	2003[2:0]	R	Three bits containing comparator output status. Bit0 = comp1, Bit1 = comp2, Bit2 = comp3
DIO_R0[2:0] *DIO_R1[2:0]* *DIO_R2[2:0]* *DIO_R3[2:0]* *DIO_R4[2:0]* *DIO_R5[2:0]* *DIO_R6[2:0]* *DIO_R7[2:0]* *DIO_R8[2:0]* *DIO_R9[2:0]* *DIO_R10[2:0]* *DIO_R11[2:0]*	2009[2:0] 2009[6:4] 200A[2:0] 200A[6:4] 200B[2:0] 200B[6:4] 200C[2:0] 200C[6:4] 200D[2:0] 200D[6:4] 200E[2:0] 200E[6:4]	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	Connects dedicated I/O pins 0 to 11 to selectable internal resources. If more than one input is connected to the same resource, the 'Multiple' column below specifies how they are combined. See Software User's Guide for details).
DIO_DIR0[7:0]	SFR A2	R/W	Programs the direction of DIO pins 7 through 0. 1 indicates output. Ignored if the pin is not configured as I/O. See *DIO_EEX* for special option for DIO4 and DIO5.
DIO_DIR1[7:0]	SFR 91	R/W	Programs the direction of DIO pins 15 through 8. 1 indicates output. Ignored if the pin is not configured as I/O.
DIO_DIR2[5:0]	SFR A1[5:0]	R/W	Programs the direction of DIO pins 21 through 16. 1 indicates output. Ignored if the pin is not configured as I/O.

DIO_GP	Resource	Multiple
0	NONE	--
1	Reserved	OR
2	T0 (counter0 clock)	OR
3	T1 (counter1 clock)	OR
4	High priority I/O interrupt (int0 rising)	OR
5	Low priority I/O interrupt (int1 rising)	OR
6	High priority I/O interrupt (int0 falling)	OR
7	Low priority I/O interrupt (int1 falling)	OR

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DIO_0[7:0] *DIO_1[7:0]* *DIO_2[5:0]*	SFR 80 SFR 90 SFR A0[5:0]	R/W R/W R/W	Port 0 Port 1 Port 2	The value on the DIO pins. Pins configured as LCD will read zero. When written, changes data on pins configured as outputs. Pins configured as LCD or input will ignore writes.
DIO_FLT	2008[2]	R/W	Causes FAULT_PULSE to be output on DIO7, if DIO7 is configured as output. *LCD_NUM* must be less than 15. Initialize *DIO_FLT* to 1.	
DIO_STR	2008[3]	R/W	Causes STROBE to be output on DIO6, if DIO6 is configured as output. *LCD_NUM* must be less than 16. Initialize *DIO_STR* to 1.	
DIO_EEX	2008[4]	R/W	When set, converts DIO4 and DIO5 to interface with external EEPROM. DIO4 becomes SCK and DIO5 becomes bi-directional SDA. *LCD_NUM* must be less than 18.	
EEDATA[7:0]	SFR 9E	R/W	Serial EEPROM interface data	
EECTRL[7:0]	SFR 9F	R/W	Serial EEPROM interface control	
ECK_DIS	2005[5]	R/W	Emulator clock disable. When one, the emulator clock is disabled.	
EX_XFR *EX_ZP8*	2002[0] 2002[1]	R/W	Interrupt enable bits. These bits enable the XFER_BUSY and the ZP8 interrupts to the MPU. Note that if either interrupt is to be enabled, EX6 in the 80515 must also be set.	
FIR_LEN	2005[4]	R/W	The length of the ADC decimation FIR filter. 1: 22 ADC bits/3 PLLOUT cycles (384 CKFIR cycles), 0: 21 ADC bits/2 PLLOUT cycles (288 CKFIR cycles)	
FLASH66Z	2005[1]	R/W	Should be set to 1 to minimize supply current.	
FLSH_ERASE	SFR 94	W	Flash Erase Initiate FLSH_ERASE is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for FLSH_ERASE in order to initiate the appropriate Erase cycle. (default = 0x00). 0x55 – Initiate Flash Page Erase cycle. Must be preceded by a write to FLSH_PGADR @ SFR 0xB7. 0xAA – Initiate Flash Mass Erase cycle. Must be preceded by a write to FLSH_MEEN @ SFR 0xB2 and the debug (CC) port must be enabled. Any other pattern written to FLSH_ERASE will have no effect.	
FLSH_MEEN	SFR B2[1]	W	Mass Erase Enable 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. ***Must be re-written for each new Mass Erase cycle.***	
FLSH_PGADR	SFR B7[7:1]	W	Flash Page Erase Address FLSH_PGADR[6:0] – Flash Page Address (page 0 thru 127) that will be erased during the Page Erase cycle. (default = 0x00). ***Must be re-written for each new Page Erase cycle.***	

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FLSH_PWE	SFR B2[0]	R/W	Program Write Enable 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
Reserved *IE_ZP8*	SFR E8[0] SFR E8[1]	R/W	Interrupt flags. These flags are part of the *WDI* SFR register and monitor the ZP8 interrupt. The flags are set by hardware and must be cleared by the interrupt handler.
INTBITS	SFR F8[6:0]	R	Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use.
LCD_BSTEN	2020[7]	R/W	Enables the LCD voltage boost circuit.
LCD_CLK[1:0]	2021[1:0]	R/W	Sets the LCD clock frequency for COM/SEG pins (not the frame rate). Note: f_w = CKFIR/128 00: $f_w/2^9$, 01: $f_w/2^8$, 10: $f_w/2^7$, 11: $f_w/2^6$
LCD_EN	2021[5]	R/W	Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs.
LCD_FS[4:0]	2022[4:0]	R/W	Controls the LCD full scale voltage, VLC2: $VLC2 = VLCD \cdot (0.7 + 0.3\frac{LCD_FS}{31})$
LCD_MODE[2:0]	2021[4:2]	R/W	The LCD bias mode. 000: 4 states, 1/3 bias 001: 3 states, 1/3 bias 010: 2 states, ½ bias 011: 3 states, ½ bias 100: static display

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<table>
<tr><td>LCD_NUM[4:0]</td><td>2020[4:0]</td><td>R/W</td><td>Number of dual-purpose LCD/DIO pins to be configured as LCD. This number can be between 0 and 18. The first dual-purpose pin to be used as LCD is SEG41/DIO21. If LCD_NUM = 2, SEG41 and SEG 40 will be configured as LCD. The remaining SEG39 to SEG24 will be configured as DIO19 to DIO4.
<table>
<tr><th>LCD_NUM</th><th>SEG</th><th>DIO</th></tr>
<tr><td>0</td><td>None</td><td>DIO4-21</td></tr>
<tr><td>1</td><td>SEG41</td><td>DIO4-20</td></tr>
<tr><td>2</td><td>SEG40-41</td><td>DIO4-19</td></tr>
<tr><td>3</td><td>SEG39-41</td><td>DIO4-18</td></tr>
<tr><td>4</td><td>SEG38-41</td><td>DIO4-17</td></tr>
<tr><td>5</td><td>SEG37-41</td><td>DIO4-16</td></tr>
<tr><td>6</td><td>SEG36-41</td><td>DIO4-15</td></tr>
<tr><td>7</td><td>SEG35-41</td><td>DIO4-14</td></tr>
<tr><td>8</td><td>SEG34-41</td><td>DIO4-13</td></tr>
<tr><td>9</td><td>SEG33-41</td><td>DIO4-12</td></tr>
<tr><td>10</td><td>SEG32-41</td><td>DIO4-11</td></tr>
<tr><td>11</td><td>SEG31-41</td><td>DIO4-10</td></tr>
<tr><td>12</td><td>SEG30-41</td><td>DIO4-9</td></tr>
<tr><td>13</td><td>SEG29-41</td><td>DIO4-8</td></tr>
<tr><td>14</td><td>SEG28-41</td><td>DIO4-7</td></tr>
<tr><td>15</td><td>SEG27-41</td><td>DIO4-6</td></tr>
<tr><td>16</td><td>SEG26-41</td><td>DIO4-5</td></tr>
<tr><td>17</td><td>SEG25-41</td><td>DIO4</td></tr>
<tr><td>18</td><td>SEG24-41</td><td>None</td></tr>
</table></td></tr>
<tr><td>LCD_SEG0[3:0]
…
LCD_SEG41[3:0]</td><td>2030[3:0]
…
2059[3:0]</td><td>R/W</td><td>LCD Segment Data. Each word contains information for from 1 to 4 time divisions of each segment. In each word, bit 0 corresponds to COM0, on up to bit 3 for COM3.</td></tr>
<tr><td>MPU_DIV[2:0]</td><td>2004[2:0]</td><td>R/W</td><td>The MPU clock divider (from CKCE). These bits may be programmed by the MPU without risk of losing control.
000 - CKCE, 001 - CKCE/2, …, 111 - CKCE/2^7
MPU_DIV is 000 on power-up.</td></tr>
<tr><td>MUX_ALT</td><td>2005[2]</td><td>R/W</td><td>The MPU asserts this bit when it wishes the MUX to perform ADC conversions on an alternate set of inputs.</td></tr>
<tr><td>MUX_DIV[1:0]</td><td>2002[7:6]</td><td>R/W</td><td>The number of states in the input multiplexer.
00 - 6 states (I0-I5)
01 - 4 states (I0-I3)
10 - 3 states (I0-I2)
11 - 2 states (I0-I1)</td></tr>
<tr><td>MUX_E</td><td>2005[0]</td><td>R/W</td><td>MUX_SYNC enable. When high, converts SEG7 into a MUX_SYNC output.</td></tr>
</table>

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OPT_TXDIS	2008[5]	R/W	Tristates the OPT_TX output.
PREBOOT	SFR B2[7]	R	Indicates that the preboot sequence is active.
Reserved[1:0]	2001[7:6]	R/W	Reserved
RTM_EN	2002[3]	R/W	Real Time Monitor enable. When '0', the RTM output is low. This bit enables the two wire version of RTM
RTM0[7:0] *RTM1[7:0]* *RTM2[7:0]* *RTM3[7:0]*	2060 2061 2062 2063	R/W	Four RTM probes. Before each CE code pass, the values of these registers are serially output on the RTM pin. The *RTM* registers are ignored when *RTM_EN*=0.
SECURE	SFR B2[6]	R/W	Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
SSI_EN	2070[7]	R/W	Enables the Synchronous Serial Interface (SSI) on SEG3, SEG4, and SEG5 pins. If *SSI_RDYEN* is set, SEG6 is enabled also. The pins take on the new functions SCLK, SSDATA, SFR, and SRDY, respectively. When *SSI_EN* is high and *LCD_EN* is low, these pins are converted to the SSI function, regardless of *LCDEN* and *LCD_NUM*. For proper LCD operation, *SSI_EN* must not be high when *LCD_EN* is high.
SSI_10M	2070[6]	R/W	SSI clock speed: 0: 5MHz, 1: 10MHz
SSI_CKGATE	2070[5]	R/W	SSI gated clock enable. When low, the SCLK is continuous. When high, the clock is held low when data is not being transferred.
SSI_FSIZE[1:0]	2070[4:3]	R/W	SSI frame pulse format: 0: once at beginning of SSI sequence (whole block of data), 1: every 8 bits, 2: every 16 bits, 3: every 32 bits.
SSI_FPOL	2070[2]	R/W	SFR pulse polarity: 0: positive, 1: negative
SSI_RDYEN	2070[1]	R/W	SRDY enable. If *SSI_RDYEN* and *SSI_EN* are high, the SEG6 pin is configured as SRDY. Otherwise, it is an LCD driver.
SSI_RDYPOL	2070[0]	R/W	SRDY polarity: 0: positive, 1: negative
SSI_BEG[7:0] *SSI_END[7:0]*	2071[7:0] 2072[7:0]	R/W	The beginning and ending address of the transfer region of the CE data memory. If the SSI is enabled, a block of words starting with *SSI_BEG* and ending with *SSI_END* will be sent. *SSI_END* must be larger than *SSI_BEG*. The maximum number of output words is limited by the number of SSI clocks in a CE code pass—see *FIR_LEN, MUX_DIV,* and *SSI_10M*.
Reserved	2001[5:0]	R/W	Reserved

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TMUX[3:0]	2000[3:0]	R/W	Selects one of 16 inputs for TMUXOUT. 0 – DGND (analog) 1 – IBIAS (analog) 2 – Reserved for production test 3 – VBIAS (analog) 4 – RTM (Real time output from CE) 5 – Reserved for production test 6 – V2_OK (Comparator 2 Output) 7 – INEUTRAL_OK (Comparator 3 Output) 8 – RXD (from Optical interface) 9 – MUX_SYNC (from MUX_CTRL) A – CK_10M B – CK_MPU C – reserved for production test D – CK38 E – Reserved F – Reserved
RESERVED	2005[7]	R/W	Must be zero.
TRIMSEL	20FD	W	Selects the temperature trim fuse to be read with the *TRIM* register (*TRIMM[2:0]*: 4, *TRIMBGA*: 5, *TRIMBGB*: 6)
TRIM	20FF	R	Contains *TRIMBGA*, *TRIMBGB*, or *TRIMM[2:0]* depending on the value written to *TRIMSEL.*
VERSION[7:0]	2006	R	The silicon revision number. This data sheet does not apply to revisions preceding revision 000 0100.
VREF_CAL	2004[7]	R/W	Enables VREF out to the VREF pin. This feature is disabled when *VREF_DIS*=1.
VREF_DIS	2004[3]	R/W	Disables the internal voltage reference.

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CE Program and Environment

CE Program

The CE program is supplied by TERIDIAN as a data image that can be merged with the MPU operational code for circuit breaker applications. Typically, the CE program covers most applications and does not need to be modified. Proper operation of the CE requires the following environment variables to be set as follows: *FIR_LEN* = 0, *MUX_DIV* = 0 and *EQU* = 101.

Formats

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement (-1 = 0xFFFFFFFF). 'Calibration' parameters are defined in flash memory (or external EEPROM) and must be copied to CE memory by the MPU before enabling the CE. 'Internal' variables are used in internal CE calculations. 'Input' variables allow the MPU to control the behavior of the CE code. 'Output' variables are outputs of the CE calculations. The corresponding MPU address for the most significant byte is given by 0x1000 + 4 x CE_address and 0x1003 + 4 x CE_address for the least significant byte.

Constants

Constants used in the CE Data Memory tables are:

- Sampling frequency: F_S = 32768Hz/13 = 2520.62Hz.
- *IMAX* is the external rms current corresponding to 250mV pk at the inputs I0 through I5.

The system constant *IMAX* is used by the MPU to convert internal digital quantities (as used by the CE) to external, i.e. current quantities. Their values are determined by the scaling of the current sensors used in an actual circuit breaker. The LSB values used in this document relate digital quantities at the CE or MPU interface to external circuit breaker input quantities.

Environment

Before starting the CE using the *CE_EN* bit, the MPU has to establish the proper environment for the CE by implementing the following steps:

- Loading the image for the CE code into CE PRAM.
- Loading the CE data into CE DRAM.
- *FIR_LEN* = 0 (two cycles per conversion)
- *MUX_DIV* = 0 (6 conversions per mux cycle)
- *EQU* = 101

During operation, the MPU is in charge of controlling the multiplexer cycles. For example, by inserting an alternate multiplexer sequence at regular intervals using *MUX_ALT* to enable temperature measurement. The polarity of CHOP must be altered for each sample. It must also alternate for each alternate multiplexer reading.

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CE Calculations

The CE performs the precision computations necessary to accurately measure and detect current. The compute engine firmware implements the following:

1. Supports 6 current sensing channels
2. Each channel individually configurable for Current Transformer or Rogowski coil
3. Each channel individually configurable for x8 gain for low signal sensors (MAX out < 20 mV)
4. Channel I4 configurable for Ground Fault current with fundamental frequency band pass filter or the vectorial sum of first current input channel data (Insqsum)
5. Channel I5 includes a band pass filter to process the components of fundamental frequency of operation only
6. Programmable accumulation interval generates interrupt on DIO6 for data collection
7. Programmable FAULT_THRESH register sets over current detection to generate FAULT_PULSE on DIO7
8. Individual channel calibration coefficients to adjust the gain for desired accuracy

CE RAM Locations

CE Front End Data (Raw Data)

Access to the raw data provided by the AFE is possible by reading addresses 0 through 7, as listed below. The table also shows the Configuration Register location for each input channel.

Address (HEX)	Input Channel	Configuration Register	Description
0x00	I0	0x28	Current input 0
0x01	I1	0x29	Current input 1
0x02	I2	0x2A	Current input 2
0x03	I3	0x2B	Current input 3
0x04	I4	0x2C	Current input 4
0x05	I5	0x2D	Current input 5
0x06	TEMP	--	Temperature
0x07	INEUTRAL	--	INEUTRAL monitor/comparator input to power fault block

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Input Configuration

The input sensor type and its gain can be set for each current input using the configuration registers 0x28 thru 0x2D, as listed in the table below (bits labeled "X" are "don't care"):

		Bit							
Address	**Channel**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x28	I0	X	X	X	X	X	X	*CT/ROG*	*GAIN*
0x29	I1	X	X	X	X	X	X	*CT/ROG*	*GAIN*
0x2A	I2	X	X	X	X	X	X	*CT/ROG*	*GAIN*
0x2B	I3	X	X	X	X	X	X	*CT/ROG*	*GAIN*
0x2C	I4	X	X	X	X	X	*I4SUM*	*CT/ROG*	*GAIN*
0x2D	I5	X	X	X	X	X	X	*CT/ROG*	*GAIN*

By setting bit 0 = 1, a gain of 8 is applied to the input raw signal associated with the configuration register. When bit 1 is set to 1, the compute engine will process the input signal as a signal from a Rogowski coil sensor.

Example: When 0x03 is written to the configuration register at address 0x29, the I1_RAW input signal is processed with a gain of 8 and is also integrated, assuming that it is generated by a Rogowski coil current sensor.

The processing for I4 can be selected to implement either a regular current input (*I4SUM* = 0) or to calculate a vectorial sum of inputs I0, I1, I2, and I3 (*I4SUM* = 1). When *I4SUM* is set to 1, all other configuration bits for I4 are ignored. Likewise, the CE ignores the *I4SUM* bit for all channels other than I4.

The *NB* (narrow-band) register (0x2E) allows control of the band-pass filtering for fundamental components in the channels I4 and I5. When *NB* is set to 1, the narrow-band filter is activated:

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	X	X	X	X	X	*X*	*X*	*NB*

Accumulation Strobe Output

Since circuit breaker applications tend to have very short accumulation intervals, the CE supports signaling the end of the accumulation interval by a strobe on the DIO6 pin.

This can be used for generating a hardware interrupt. If a hardware interrupt is desired, DIO6 should be configured as an output, and the associated *DIO_Rx* register in I/O RAM should be used to associate an interrupt source with the pin.

The CE generates a low-going strobe of 397µs at the end of each accumulation interval. The control register for the accumulation interval is *STR_CNT* (address 0x31). This register has a resolution of 397 microseconds. The accumulation interval is controlled by *STR_CNT* as follows:

Accumulation interval = (*STR_CNT* + 1) * 397µs

Example: When *STR_CNT* is set to (decimal) 12, the accumulation interval will be 5.1 ms.

The processed data is available in the following registers.

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Processed Current Data

Processed current data is available in CE addresses 0x4A through 0x4F, as listed below:

Output Register	CE Address	Description
I0SQSUM_X	0x4A	LSB = (IMAX/ln8)^2 * 3.3335*10^{-8} A^2 peak
I1SQSUM_X	0x4B	LSB = (IMAX/ln8)^2 * 3.3335*10^{-8} A^2 Peak
I2SQSUM_X	0x4C	LSB = (IMAX/ln8)^2 * 3.3335*10^{-8} A^2 Peak
I3SQSUM_X	0x4D	LSB = (IMAX/ln8)^2 * 3.3335*10^{-8} A^2 Peak
I4SQSUM_X	0x4E	LSB = (IMAX/ln8)^2 * 3.3335*10^{-8} A^2 Peak
I5SQSUM_X	0x4F	LSB = (IMAX/ln8)^2 * 3.3335*10^{-8} A^2 Peak

The CE writes the output data into the I0SQSUM_X, I1SQSUM_X etc. registers at the end of each accumulation interval.

The values for IXSQSUM_X are based on the formula:

$$IXSQSUM_X = \sum_{0}^{STR_CNT+1} IXSQ$$

Overcurrent Detection

The main task in circuit breaker applications is to detect an over-current situation as quickly as possible and to apply the tripping procedures. The CE firmware has an integrated comparator function that helps to verify each measured sample with reference to the value stored in the *FAULT_THRESH* register at address 0x2F. If a sample above the programmed *FAULT_TRHESH* is encountered in one of the input signals I0, I1, I2 or I3, the FAULT_PULSE is generated on the DIO7 pin. This pin should be configured by the MPU to be an output pin and should be internally set to generate an interrupt in order to initiate the necessary routines of the circuit breaker application firmware. The process for generating the FAULT_PULSE from encountering a sample above the programmed threshold can be less than 400µs.

CE Register	CE Address	Description
FAULT_THRESH	0x2F	LSB = (IMAX/ln8) * 5.5719*10^{-9} A peak
STR_CNT	0x31	STROBE_PULSE = (*STR_CNT* + 1) * 3.9673*10^{-4} s

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CE Calibration Parameters

The table below lists the parameters that are typically entered to effect calibration of circuit breaker accuracy.

CE Address	Name	Default	Description
0x08	*CAL_I0*	16384	These six constants control the gain of their respective channels. The nominal value for each parameter is 2^{14} = 16384. The gain of each channel is directly proportional to its calibration parameter. Thus, if the gain of a channel is 1% slow, CAL should be increased by 1%.
0x09	*CAL_I1*	16384	
0x0A	*CAL_I2*	16384	
0x0B	*CAL_I3*	16384	
0x0C	*CAL_I4*	16384	
0x0D	*CAL_I5*	16384	

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Flash Programming

Operational or test code can be programmed into the flash memory using either an in-circuit emulator or the Flash Download Board Module (FDBM) available from TERIDIAN. The flash programming procedure uses the E_RTS, E_RXTX, and E_TCLK pins.

MPU Firmware Library

All application-specific MPU functions mentioned above under “Application Information” are available from TERIDIAN as a standard ANSI C library and as ANSI “C” source code. The code is available as part of the Demonstration Kit for the 71M6403. The Demonstration Kits come with the 71M6403 IC preprogrammed with demo firmware mounted on a functional example of a circuit breaker PCB (Demo Board). The Demo Boards allow for quick and efficient evaluation of the IC without having to write firmware or having to supply an in-circuit emulator (ICE).

A reference guide for firmware development on the 71M6403 is available as a separate document (Software User’s Guide, “SUG”). The User’s Manual supplied with the Demo Kit contains MPU address maps for the demo code as well as other useful information, such as sample calibration procedures.

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SPECIFICATIONS

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

Supplies and Ground Pins:	
V3P3D, V3P3A	–0.5V to 4.6V
| V3P3D - V3P3A |	0V to 0.5V
VLCD	-0.5V to 7V
GNDD	-0.5V to +0.5V
Analog Output Pins:	
VREF, VBIAS	-1mA to 1mA, -0.5 to V3P3A+0.5V
V2P5	-1mA to 1mA, -0.5V to 3.0V
Analog Input Pins:	
I0, I1, I2, I3, I4, I5, V2, INEUTRAL	-0.5V to V3P3A+0.5V
CK38	-0.5V to 3.0V
RX	-0.5V to 3.6V
OPT_RX	-1mA to 1mA -0.5 to V3P3A+0.5V
Digital Input Pins:	
DIO0-21, E_RXTX, E_RST, E_ISYNC/BRKRQ	-0.5 to 6V
RESETZ	-0.5 to V3P3D+0.5V
All Other Pins:	
Input pins	-5mA to 5mA -0.5V to V3P3D+0.5V
Output pins	-30mA to 30mA -0.5 to V3P3D+0.5V
Temperature:	
Operating junction temperature (peak, 100ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	–45 °C to 165 °C
Solder temperature – 10 second duration	250 °C
ESD Stress:	
Pins I0, I1, I2, I3, I4, I5, RX, TX, E_RST, E_TCLK, E_RXTX, E_TBUS[n]	4kV
All other pins	2kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

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RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
3.3V Supply Voltage (**V3P3A, V3P3D**) †	Normal Operation	3.0	3.3	3.6	V
	Battery Backup	0		3.45	V
VLCD		2.9		5.5	V
Operating Temperature		-40		85	ºC

†V3P3A and V3P3D should be shorted together on the circuit board. GNDA and GNDD should also be shorted on the circuit board.

LOGIC LEVELS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Digital high-level input voltage, V_{IH}		2		V3P3D	V
Digital low-level input voltage, V_{IL}		–0.3		0.8	V
Digital high-level output voltage V_{OH}	I_{LOAD} = 1mA	V3P3D –0.4		V3P3D	V
	I_{LOAD} = 15mA	V3P3D-0.6			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 15mA			0.8	V
Input pull-up current, I_{IL} RESETZ E_RXTX, E_ISYNC/BRKRQ E_RST	VIN=0V	10		100	µA
Input pull down current, I_{IH} CK	VIN=V3P3D	10		100	µA
Input current Other digital inputs		-1		1	µA

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SUPPLY CURRENT

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V3P3A + V3P3D + VLCD current	Normal Operation, **V3P3A=V3P3D=VLCD**=3.3V No Flash memory write VBAT = 3.3V RTM_EN = 0 ECK_DIS = 1 MPU_DIV = 3		8.4	9.6	mA
V3P3A current			4.4	4.9	mA
V3P3D current			3.7	4.2	mA
VLCD current			0.2	0.4	mA
V3P3A + V3P3D current	Power save/sleep mode **V3P3A=V3P3D=VLCD**=3.3V ADC_DIS = 1 CE_EN = 0 MPU_DIV = 3		6	7	mA
V3P3D current, Write Flash	Normal Operation as above, except write Flash at maximum rate.		7		mA

2.5V VOLTAGE REGULATOR

Unless otherwise specified, load = 5mA

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage overhead **V3P3-V2P5**	Reduce V3P3 until V2P5 drops 200mV			440	mV
PSSR **ΔV2P5/ΔV3P3**	RESETZ=*1,* iload=*0*	-3		+3	mV/V

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VREF, VBIAS

Unless otherwise specified, *VREF_DIS*=0

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VREF output voltage, VNOM(25)	Ta = 22ºC	1.193	1.195	1.197	V
VREF chop step				40	mV
VREF output impedance	*CAL* =1, I_{LOAD} = 10µA, -10µA			2.5	kΩ
VNOM definition [1]	VNOM(T) = VREF(22) + (T–22)TC1 + $(T–22)^2$TC2				V
VREF temperature coefficients TC1 (linear) TC2 (quadratic)			-6.68 -0.341		µV/ºC µV/°C^2
VREF(T) deviation from VNOM(T) $\frac{VREF(T)-VNOM(T)}{VNOM}\frac{10^6}{\max(\lvert T-22\rvert,40)}$	Ta = -40ºC to +85ºC	-40		+40	ppm/ºC
VBIAS output voltage	Ta = 25ºC Ta = -40ºC to 85ºC	(-1%) (-2%)	1.6 1.6	(+1%) (+2%)	V V
VBIAS output impedance	I_{LOAD} = 1mA, -1mA		240	500	Ω

FOOTNOTE

[1] This relationship describes the nominal behavior of VREF at different temperatures.

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ADC CONVERTER, VDD REFERENCED

FIR_LEN=0, *VREF_DIS*=0, *VDDREFZ*=0

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Recommended Input Range (Vin-**V3P3A**)		-250		250	mV peak
THD (First 10 harmonics) 250mV-pk 20mV-pk	Vin=65Hz, 64kpts FFT, Blackman-Harris window			 -75 -90	 dB dB
Input Impedance	Vin=65Hz	40		90	kΩ
Temperature coefficient of Input Impedance	Vin=65Hz		1.7		Ω/°C
LSB size			355		nV/LSB
Digital Full Scale			±884736		LSB
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100\Delta V3P3A/3.3}$	Vin=200mV pk, 65Hz V3P3A=3.0v, 3.6V			50	ppm/%
Input Offset (Vin-**V3P3A**)		-10		10	mV

OPTICAL INTERFACE

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
OPT_TX VOH (**V3P3D**-**OPT_TX**)	ISOURCE=1mA			0.4	V
OPT_TX VOL	ISINK=20mA			0.7	V
OPT_RX Vin Threshold (VinRISING+VinFALLING)/2		200	250	300	mV
OPT_RX Vin Hysteresis (VinRISING-VinFALLING)		5		30	mV
OPT_RX input impedance	|Vin|≤300mV	1			MΩ

TEMPERATURE SENSOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Nominal Sensitivity (S_n) [2]	TA=25ºC, TA=75ºC Nominal relationship: $N(T)= S_n*T+N_n$		-900		LSB/ºC
Nominal Offset (N_n) [2]			400000		LSB
Temperature Error [3] $ERR = (T-25) - \frac{(N(T)-N(25))}{S_n}$	TA = -40ºC to +85ºC	-3		3	ºC

FOOTNOTES

[2] This parameter defines a nominal relationship rather than a measured parameter. Correct circuit operation is verified with other specs that use this nominal relationship as a reference.

[31] This parameter is has been verified in production samples, but is not measured in production.

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LCD BOOST

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VDRV Frequency			CK / 1200		Hz
VDRV Sink Current	Vol=1.5V	1.6		3.0	mA
VDRV Source Current	Voh=1.5V	1.2		2.6	mA
VLCD Target Voltage		4.5		5.7	V
VLCD Input Current	VLCD=5.0V, LCD_FS=1F, LCD_MODE=0,1,2,3 *LCD_BSTEN*=1			450	µA

LCD DRIVERS

Applies to all COM and SEG pins. Unless otherwise stated, VLCD=5.0V, *LCD_FS*=1F

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VLC0 Max Voltage (*LCD_FS* =1F)	With respect to VLCD	-0.2		0	V
VLC0 Min Voltage (*LCD_FS* =00)	With respect to VLCD*0.7	-0.2		0.2	V
VLC1 Voltage, 1/3 bias ½ bias	 With respect to 2*VLCD/3 With respect to VLCD/2	 -10 -10		 +10 +10	 % %
VLC0 Voltage, 1/3 bias ½ bias	 With respect to VLCD/3 With respect to VLCD/2	 -15 -10		 +15 +10	 % %
Output Impedance	ΔI_{LOAD}=10µA			30	kΩ

RESETZ

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Reset pulse width		5			µs
Reset pulse fall time				1	µs

COMPARATORS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Offset Voltage **V2-VBIAS** **INEUTRAL-VBIAS**		 -20 -20		 15 15	 mV mV
Hysteresis Current **V2** **INEUTRAL**	Vin = VBIAS - 100mV	 0.8 0.8		 1.2 1.2	 µA µA
Response Time **V2** **INEUTRAL**	±100mV overdrive	 0.5 0.5		 50 50	 µs µs

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RAM AND FLASH MEMORY

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
CE RAM wait states	CKMPU = 4.9MHz	5			Cycles
Flash write cycles		20,000			Cycles
Flash data retention	25°C	100			Years

FLASH MEMORY TIMING

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Write Time per Byte			42		µs
Read Time: No wait states					
Page Erase (512 bytes)			20		ms
Mass Erase			200		ms

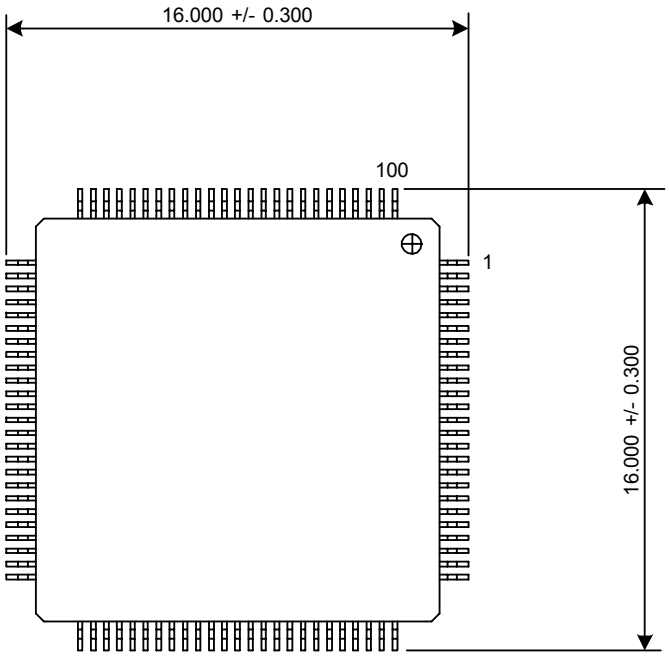
EEPROM INTERFACE

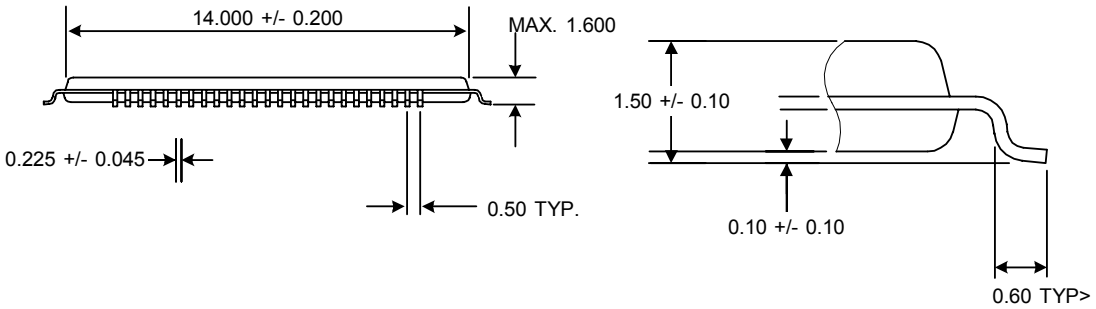
PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Write Clock frequency	CKMPU=4.9MHz, Using interrupts		78		kHz
	CKMPU=4.9MHz, “bit-banging” DIO4/5		150		kHz

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Packaging Information

100-Pin LQFP PACKAGE OUTLINE (Bottom View)

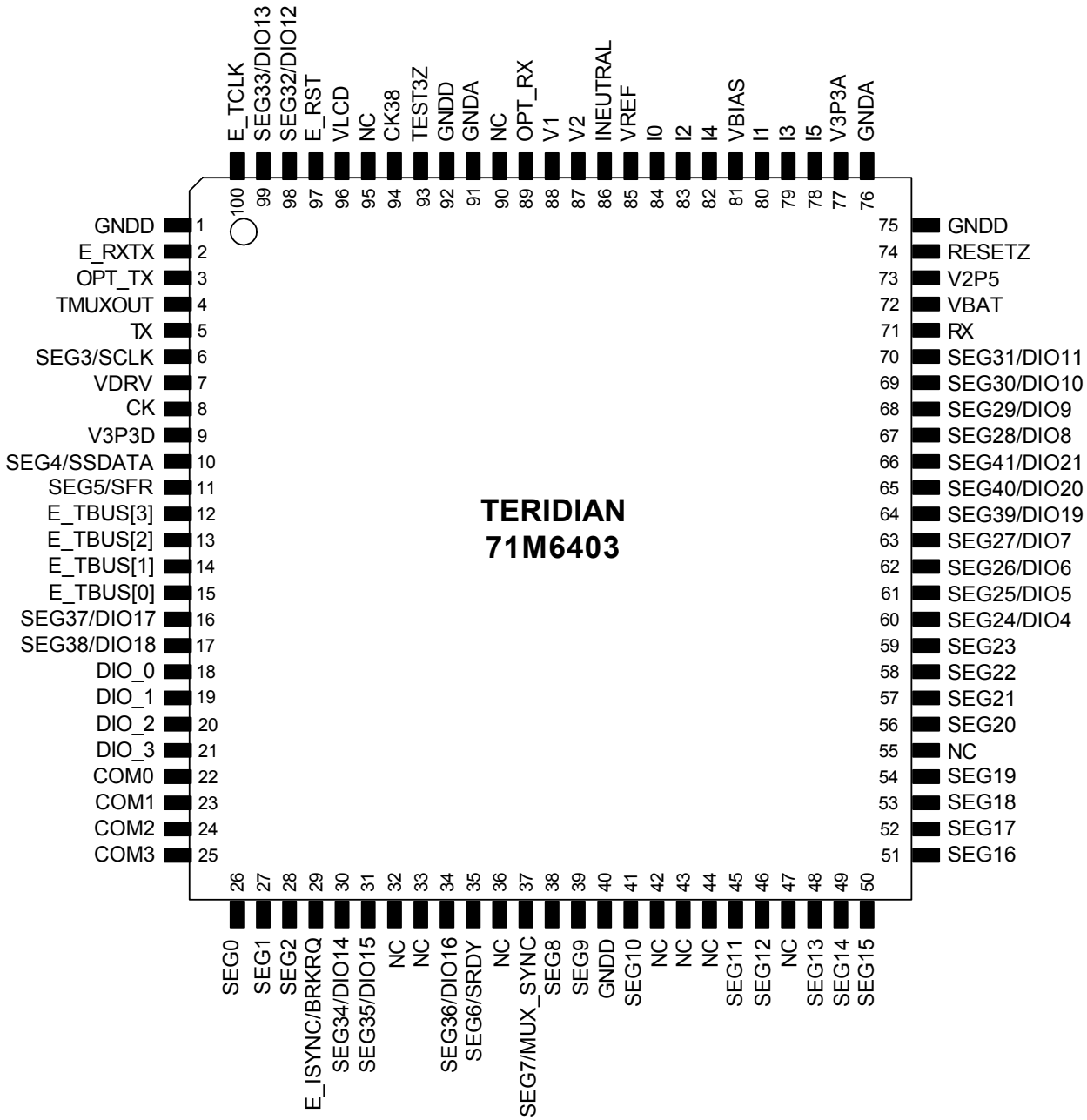




Side View

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Pinout (Top View)



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Pin Descriptions

Power/Ground Pins

NAME	PIN #	TYPE	DESCRIPTION
GNDA	76,91	P	Analog ground: This pin should be connected directly to the analog ground plane. Recommend a common ground plane consisting of both GNDA and GNDD.
GNDD	1, 40, 75, 92	P	Digital ground: This pin should be connected directly to the digital ground plane. Recommend a common ground plane consisting of both GNDA and GNDD.
V3P3A	77	P	Analog power supply: A 3.3V analog power supply should be connected to this pin. Recommend a common power plane consisting of both V3P3A and V3P3D.
V3P3D	9	P	Digital power supply: A 3.3V digital power supply should be connected to this pin. Recommend a common power plane consisting of both V3P3A and V3P3D.
V2P5	73	O	Output of the 2.5V regulator. A 0.1µF capacitor to GNDA should be connected to this pin.
VBAT	72	O	Battery backup power supply pin. A battery or super-capacitor may be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D.
VLCD	96	P	LCD power supply. The DC source for the LCD driver circuitry is connected here.
NC	32,33,36, 42,43,44, 47,55,90,95	--	No Connect

Analog Pins

NAME	PIN #	TYPE	DESCRIPTION
I0 I1 I2 I3 I4 I5	84 80 83 79 82 78	I	Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the output of a current transformer.
V1 V2 INEUTRAL	88 87 86	I	Comparator Inputs - voltage inputs to the internal comparator: The voltages applied to these pins are compared to an internal BIAS voltage of 1.6V. If the input voltage is above VBIAS, the corresponding comparator output will be high (1). V1 is a status signal to the reset circuitry. It may also be used to disable the watchdog timer. Place a 0.1µF capacitor between pin V1 and GNDA. The V2 and INEUTRAL comparator outputs are maintained in *COMP_STAT* as follows: bit 1 = V2, bit 3 = INEUTRAL. A typical application is to sense the voltage on the DC supply.
VBIAS	81	O	Reference voltage used by the power fault detection circuit.
VREF	85	I/O	Voltage Reference for the ADC. A 0.1µF capacitor to GNDA should be connected to this pin.
CK38	94	I	Low-frequency clock input. Provides time base for RTC, watchdog timer and ZP8.
VDRV	7	O	Voltage boost output.

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Digital Pins:

NAME	PIN #	TYPE	DESCRIPTION
DIO_3, DIO_2, DIO_1, DIO_0	21 20 19 18	I/O	Digital input/output pins 0 through 3
COM3, COM2, COM1, COM0	25 24 23 22	O	LCD Common Outputs: These 4 pins provide the select signals for the LCD display.
SEG0…SEG2, SEG8…SEG23	See pinout	O	Dedicated LCD segment outputs
SEG24/DIO4… ……. SEG41/DIO21	See pinout	I/O	Multi-use pins, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface, STROBE = DIO6, FAULT_PULSE = DIO7 when configured as pulse outputs)
SEG7/MUX_SYNC	37	O	Multi-use-pin LCD Segment Output/ MUX_SYNC is output for Synchronous serial interface
SEG6/SRDY	35	I/O	Multi-use-pin, LCD Segment Outputs/ SRDY input for Synchronous serial interface.
SEG5/SFR	11	O	Multi-use-pin, LCD Segment Output/ SFR output for SSI.
SEG4/SDATA	10	O	Multi-use-pin, LCD Segment Output/ SDATA output for SSI.
SEG3/SCLK	6	O	Multi-use-pin, LCD Segment Output/ SCLK output for SSI.
RESETZ	74	I	Chip reset: This pin is used to reset the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0. This pin has an internal 30µA (nominal) current source pull-up but no Schmitt-trigger input circuitry. The minimum width of the pulse is 5µs. A 0.1µF capacitor to GNDA should be connected to this pin.
RX	71	I	UART input. The voltage applied at this input must be below 3.6V.
TX	5	O	UART output.
OPT_RX	89	I	Optical Receive Input: This pin receives a signal from an external photo-detector used in an IR serial interface.
OPT_TX	3	O	Optical LED Transmit Output: This pin is designed to directly drive an LED for transmitting data in an IR serial interface. Can be tristated with *OPT_TXDIS* to be multiplexed with other DIO pins.
CK	8	O	Clock input (19.6608 MHz)
TMUXOUT	4	O	Digital output test multiplexer. Controlled by *DMUX[3:0].*
E_RXTX	2	I/O	Emulator serial data.
E_TBUS[3] E_TBUS[2] E_TBUS[1] E_TBUS[0]	12 13 14 15	O	Emulator trace bus. These pins have internal pull-up resistors.
E_ISYNC/BRKRQ	29	I/O	Emulator handshake. This pin has an internal pull-up resistor.
E_TCLK	100	O	Emulator clock. This pin has an internal pull-up resistor.
E_RST	97	I	Emulator reset. This pin has an internal pull-up resistor.
TEST3	93	I	For TERIDIAN internal use. This pin must be connected to GNDD via a 1kΩ resistor.

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ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING
71M6403 Electronic Trip Unit, 100-pin LQFP	71M6403-IGT	71M6403-IGT xxxxxxxxxxx
71M6403 Electronic Trip Unit, 100-pin Lead-Free LQFP	71M6403-IGT/F	71M6403-IGT xxxxxxxxxxxF
71M6403 Electronic Trip Unit, 100-pin LQFP, T&R	71M6403-IGTR	71M6403-IGT xxxxxxxxxxx
71M6403 Electronic Trip Unit, 100-pin Lead-Free LQFP, T&R	71M6403-IGTR/F	71M6403-IGT xxxxxxxxxxxF

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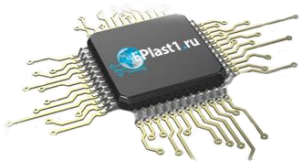
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