2.5-GHz, High Dynamic Range, Low-Noise Down-Converter

FEATURES

- **Performs First Down-Conversion in MMDS / WCS Radio 2300 MHz to 2700 MHz**
- **Integrated Low Noise, Variable Gain Amplifier**
- **Provisions For An External Image Reject / Band Pass Filter**
- **Differential Mixer Provides Extra Noise Immunity**
- **Integrated LO Buffer Amplifier**
- **20 dB of Gain With 10 dB of Gain Control**
- **3-dB Noise Figure, Typical**
- **Input Third Order Intercept of 0 dBm, Typical**
- **Input P-1 dB of –5 dBm, Typical**
- **LO Input Power: 3 dBm**

DESCRIPTION

The TRF1115 is the first of two ASICs used in the receiver section of Texas Instruments MMDS/MDS/WCS/802.16x chipset. The TRF1115 down-converts the input frequency to an IF frequency in the range of 420 MHz to 480 MHz. The device provides a differential output that passes through a SAW filter before connecting to a second down converter chip. (Note: For the best performance, the Texas Instruments TRF1112 should be used to perform both the second down conversion and provide the local oscillator for the TRF1115.)

In order to provide exceptional image rejection and extra jammer rejection, the TRF1115 offers a signal path to an off-chip filter. Specifications are provided assuming an in-band 1.5-dB loss in this filter. The TRF1115 includes a differential LO buffer, mixer, and IF amplifier for improved performance. After the filter, an on-chip balun converts the signal from single-ended to differential in order to provide better noise immunity in the mixer.

DEVICE INFORMATION

TRF1115
(TOP VIEW)

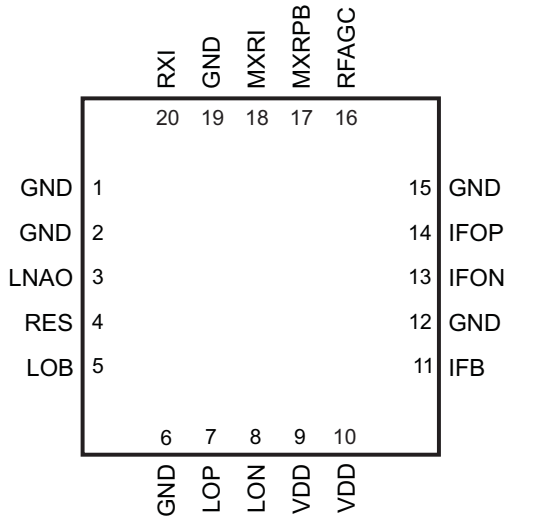


Figure 1. TRF1115 Pin Out

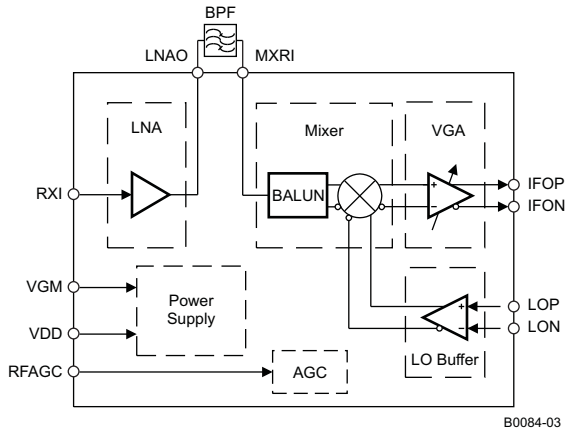


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

		VALUE	UNIT
VDD	Positive DC Supply Voltage, VDD	0.0 to +5.5	V
IDD	Current consumption	200	mA
Pin	RF Input Power	5	dBm
T_J	Junction Temperature	200	°C
Pd	Power Dissipation	1.1	W
	Digital Input Pins	–0.3 to 5.5	
θ_{JC}	Thermal Resistance Junction to Case(1)	9.1	°C/W
T_{stg}	Storage Temperature	–40 to 105	°C
T_{op}	Operating Temperature	–40 to 85	°C
	Lead Temperature (40 sec max)	260	°C

(1) Thermal resistance is junction to ambient assuming thermal pad with 16 thermal vias under package metal base. See Recommended PCB layout.

DC SPECIFICATIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Supply Voltage			5	5.25	V
IDD	Supply Current (Total)			130	180	mA
I_{LNA}	Supply Current, LNA, pin 3			30		mA
I_{LO}	Supply Current, LO, pin 9			45		mA
I_{IF}	Supply Current, IF	Pins 10 plus IF drain bias on pins 13 and 14.		55		mA
V_C	Gain Control Voltage		0		2	V
I_C	Gain Control Current		0		1.2	mA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated VDD = 5.0 V, External Filter loss = 1.5 dB, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{RF}	RF input frequency		2300		2700	MHz
f_{LO}	LO input frequency		1820		2220	MHz
f_{IF}	IF output frequency		400	480	500	MHz
G	Gain	V_C = 0 V	16	18		dB
	Gain control range	V_C > 1.5 V		10		dB
G_{NB}	Gaub fkatbess / 6 MHz				0.2	dB
NF_{HG}	Noise figure, high gain	V_C = 0 V		3	4	dB
NF_{LG}	Noise figure with AGC on	V_C > 1.5 V		6	7	dB
IP-1dB	Input power at 1 dB compression, high gain	V_C = 0 V, Without RF BPF	-6	-2		dBm
IP-1dB	Input power at 1 dB compression with AGC on	V_C > 1.5 V, Without RF BPF	-1	2		dBm
IIP3	Input third order intercept point, high gain	V_C = 0 V, Without RF BPF	-3	0		dBm
IIP3	Input third order intercept point with AGC on	V_C > 1.5 V, Without RF BPF	5	8		dBm
Z_{RF}	RF input impedance	Differential		50		Ω
RL_{RF}	RF input return loss	Z = 50 Ω, P_{LO} = 3 dBm, F_{RF} = 2500 to 2700 MHz	8	10		dB
Z_{LO}	LO input impedance	Differential		100		Ω
P_{LO}	LO input power	Referenced to 100 Ω differential	0	3	6	dB
RL_{LO}	LO input return loss	Differential, with external matching circuit. LO input = 3 dBm	–10	–12		dB
Z_{IF}	IF output impedance	Differential		100		Ω
RL_{IF}	IF1 output return loss	Differential, with external matching circuit	–7	–10		dB
	LO to RF leakage, differential	LO input = 3 dBm, V_C = 0 V	–35	–45		dBm
	LO to IF1 leakage, differential	LO input = 3 dBm, V_C = 0 V	–40	–50		dBm
	RF to IF1 isolation, differential	LO input = 3 dBm, V_C = 0 V	35	45		dBc
	RF to LO insolation, differential	LO input = 3 dBm, V_C = 0 V		25		dBc

TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
1, 2, 6, 12, 15, 19	GND			Ground
3	LNAO	O	Analog/Power	Output of LNA, before mixer, Also provides DC bias to FET. Apply 5 V bias thru bias network.
4	RES			Reserved. Do not connect or ground this pin.
5	LOB			Not connected for normal operation. Internal bias for LO buffer. Normal voltage at this pin is 3.0 to 3.2 V. Do not ground this pin or connect.
7	LOP	I	Analog	LO input, Positive, ac coupled internally
8	LON	I	Analog	LO input, Negative, ac coupled internally
9	VDD	I	Power	DC bias for LO Buffer +5 V
10	VDD	I	Power	DC bias for IF circuit +5 V
11	IFB			Not connected for normal operation. Internal bias for IF circuitry Normal voltage at this pin is 2.8 to 3.0 V. Do not ground this pin or connect.
13	IFON	O	Analog/Power	IF output, negative, and dc bias for IF amplifier. Apply +5 V through bias network.
14	IFOP	O	Analog/Power	IF output, Positive, and dc bias for IF amplifier. Apply +5 V through bias network.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
16	RFAGC	I	Analog	Input voltage for gain control: V_C = 0 to 1.5 V Maximum gain at V_C = 0 V Minimum gain at V_C = 1.5 V
17	MXRPB			Not connected for normal operation. Internal bias for mixer circuitry. Normal voltage at this pin is 1.8 V to 2.5 V. Do not ground this pin or connect to any other pin.
18	MXRI	I	Analog	Input to RF mixer, ac coupled, 50 Ω
20	RXI	I	Analog	RF input, ac coupled, 50 Ω
Back	GND			Back of package has metal base that must be grounded for thermal and RF performance.

TYPICAL CHARACTERISTICS

TYPICAL DATA

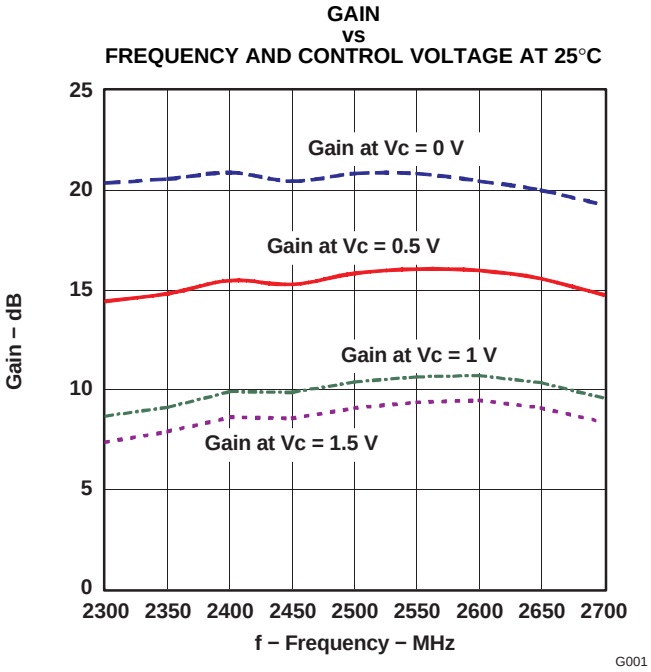


Figure 3.

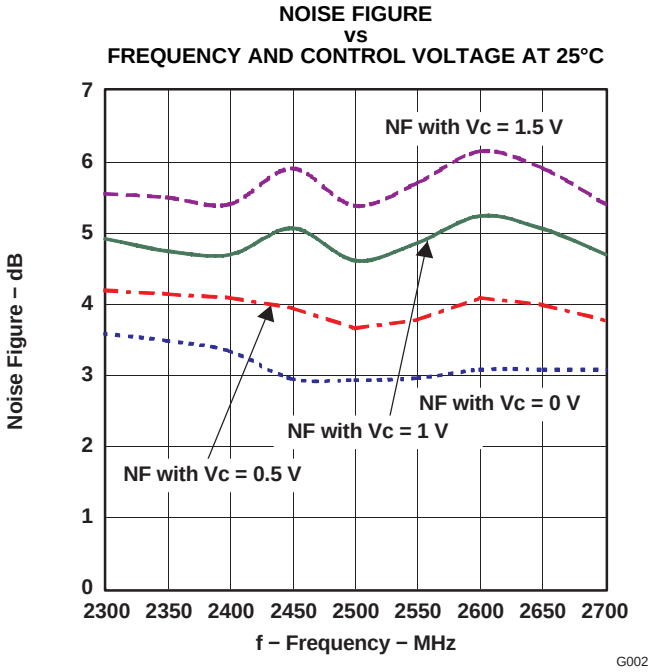


Figure 4.

TYPICAL CHARACTERISTICS (continued)

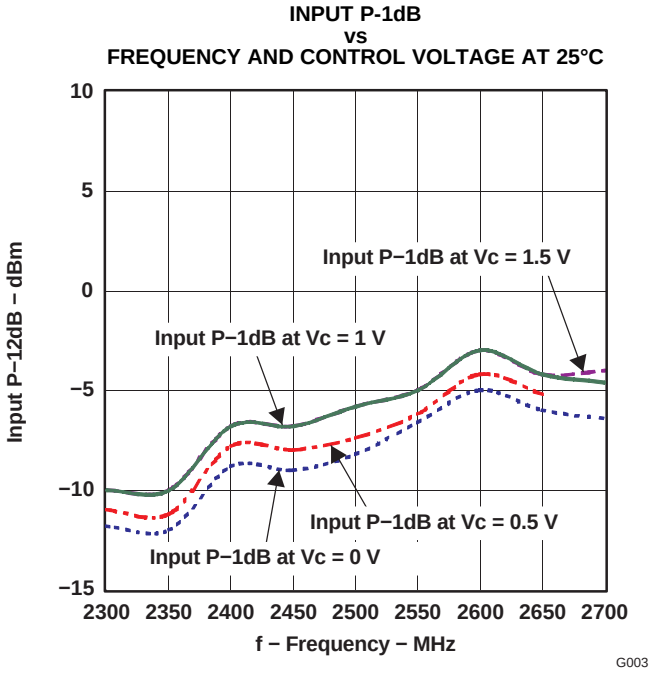


Figure 5.

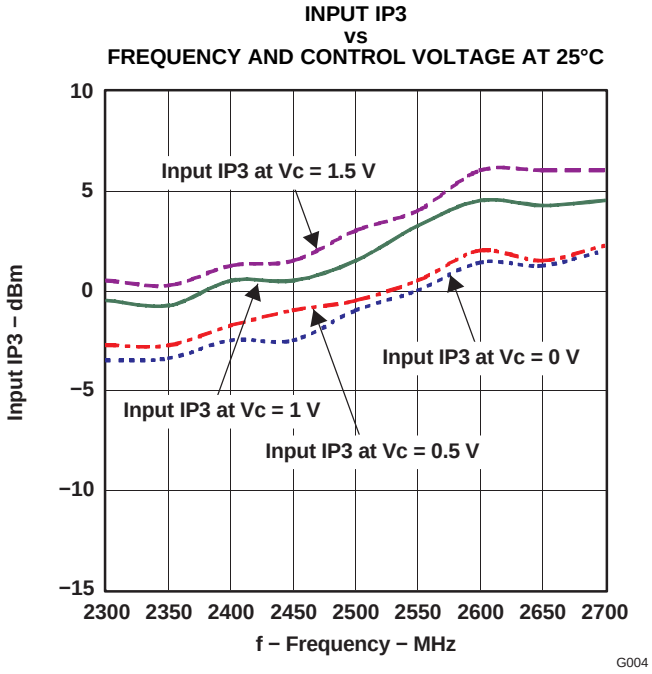


Figure 6.

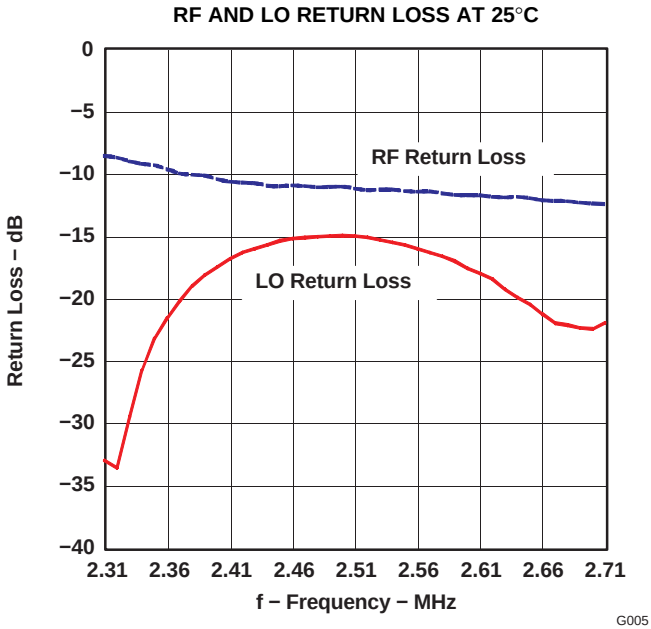
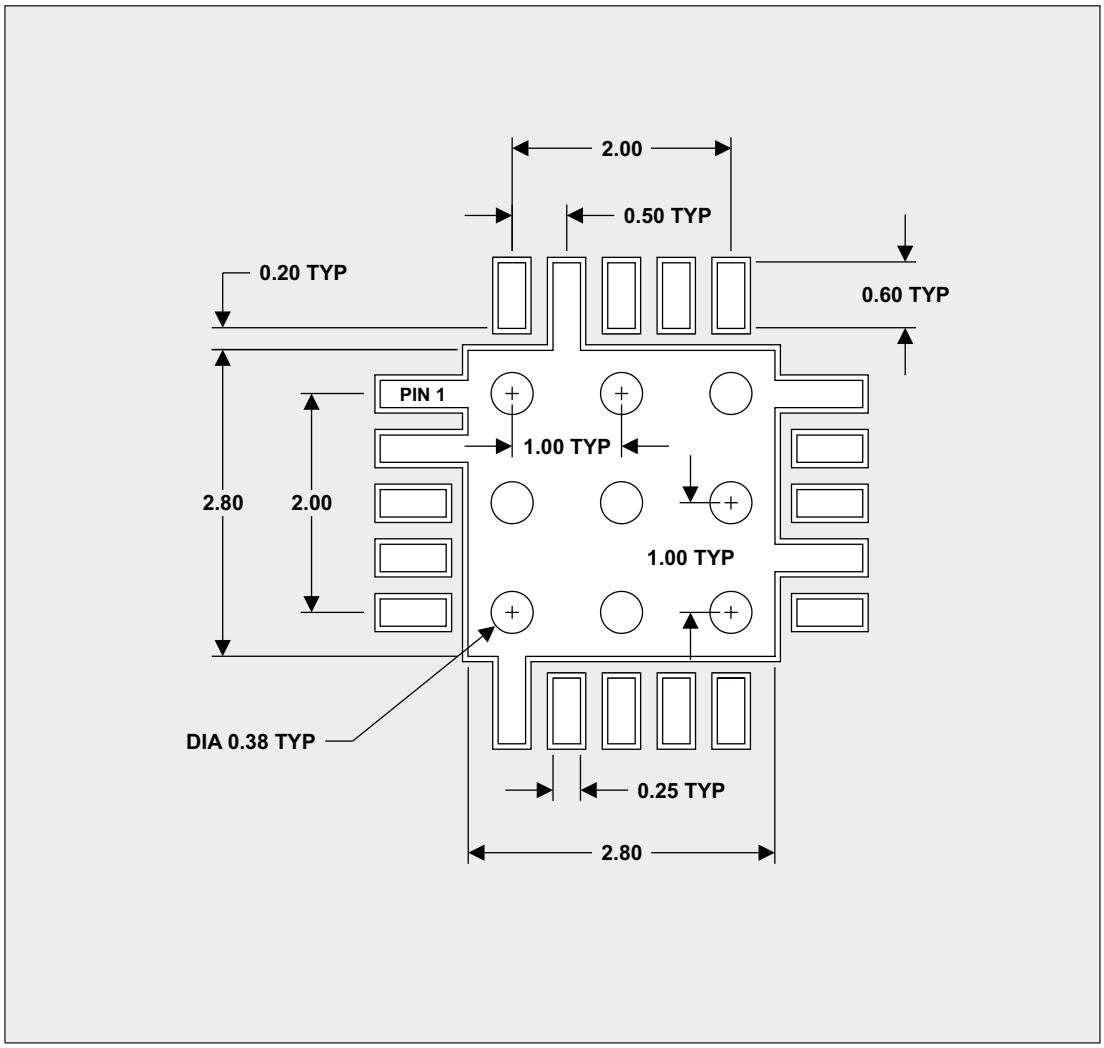


Figure 7.

RECOMMENDED PCB LAYOUT



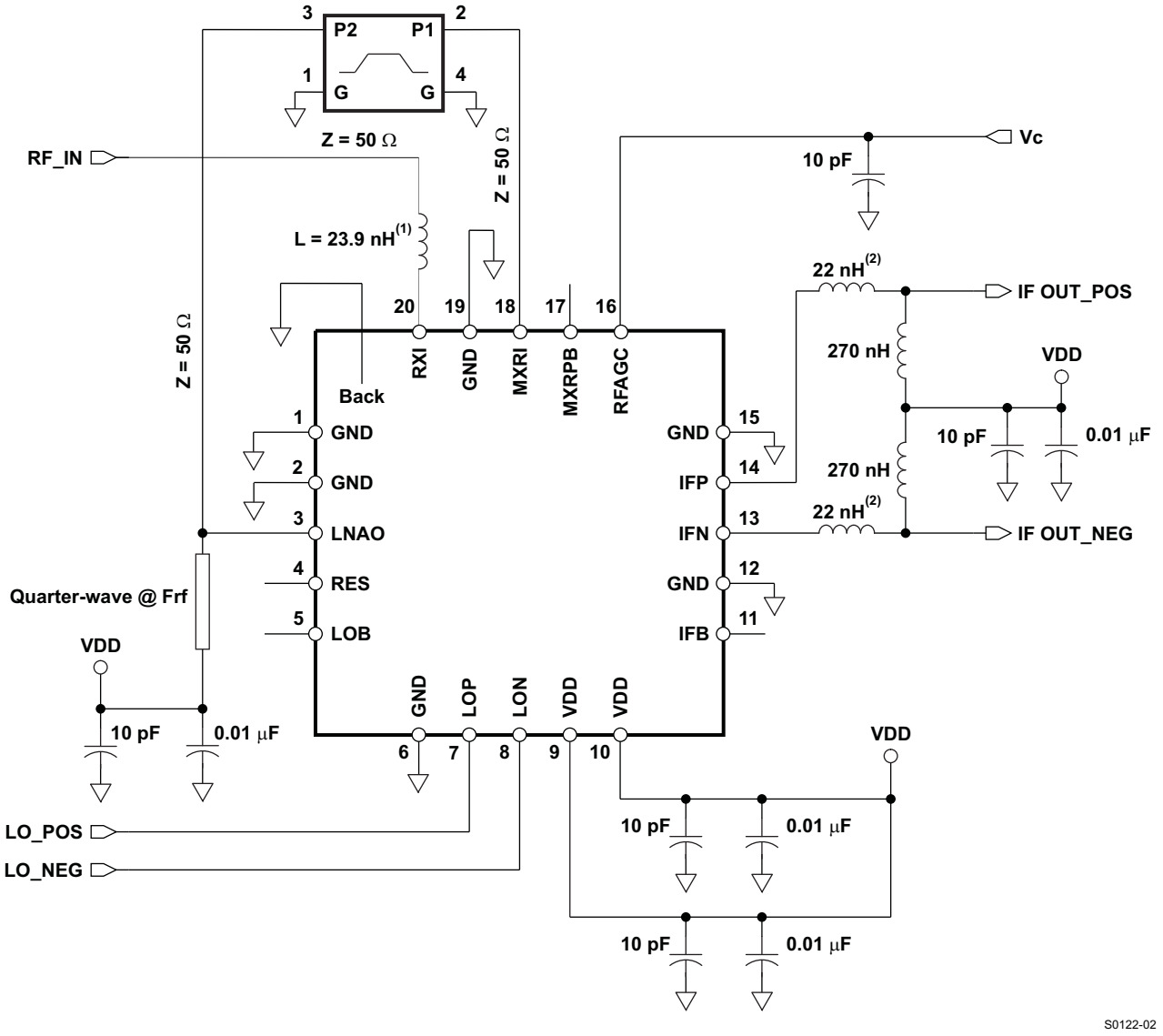
Solder Mask. No Solder Mask Under Chip, On Lead Pads or On Ground Connections.

Notes: **9 Via Holes, Each 0.38 mm.**
DIMENSIONS in mm

M0022-04

A. Four layer Board, Starting material: two: 10 mil core FR4 with 1 oz copper, both sides, pressed with 8 mil thick prepreg. Via plating ½ oz copper plate, final plate White immersion tin. Final thickness: 0.033" to 0.037" thick.

APPLICATION SCHEMATIC



APPLICATION INFORMATION

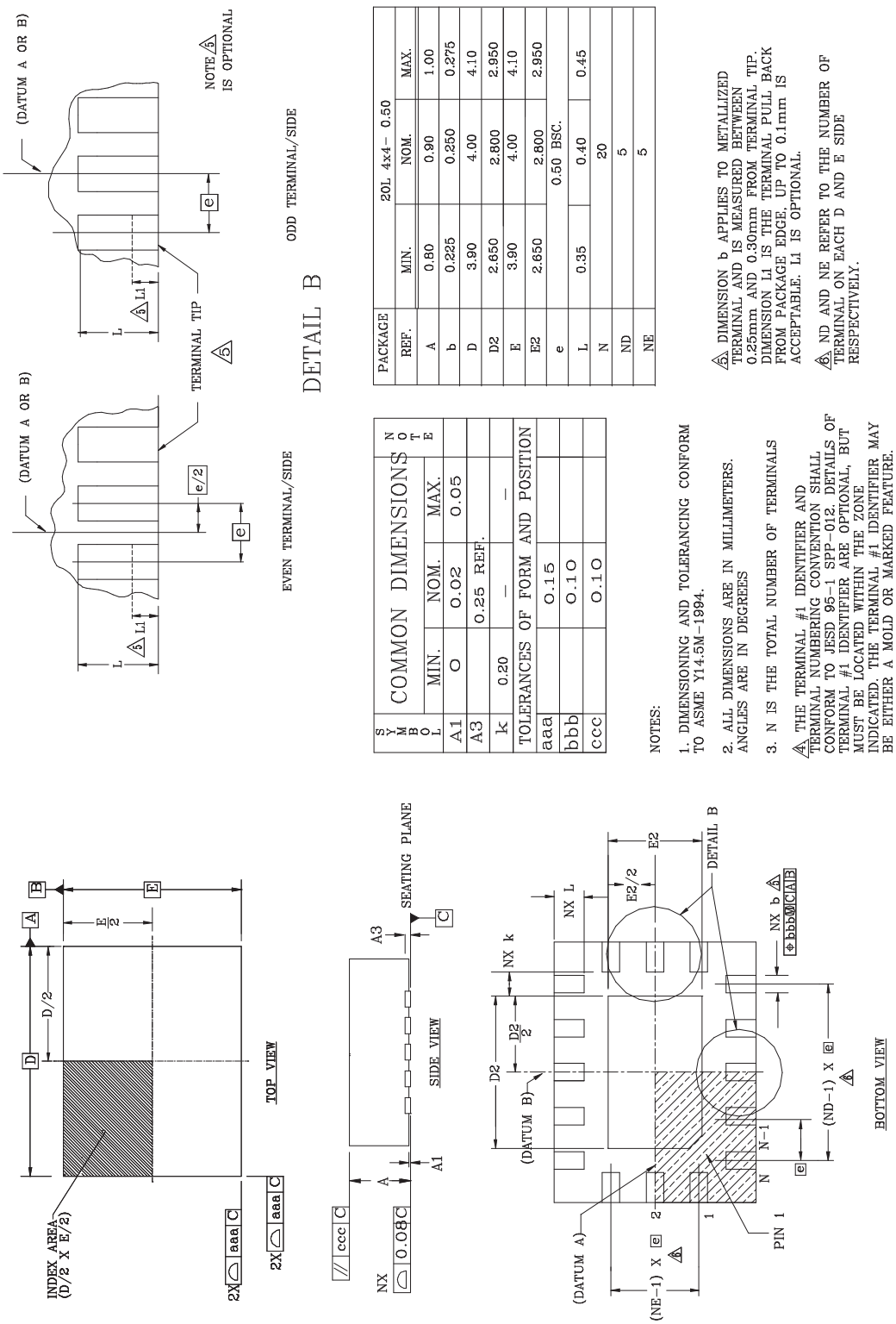


Figure 8. Package Outline: 4 mm x 4 mm LPCC 20-Pin Leadless Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TRF1115IRGPR	ACTIVE	QFN	RGP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	
TRF1115IRGPRG3	ACTIVE	QFN	RGP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	
TRF1115IRGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	
TRF1115IRGPTG3	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	

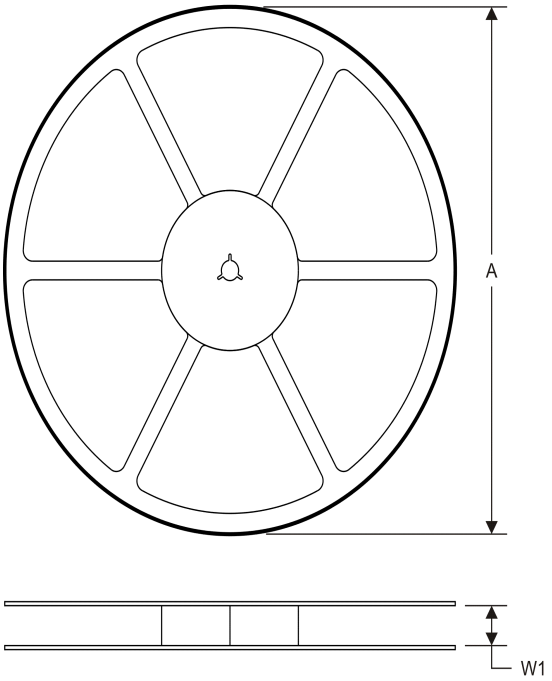
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

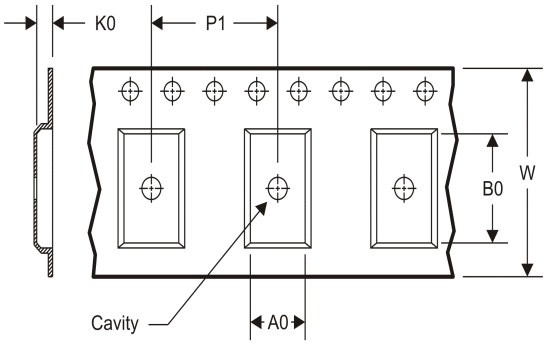
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



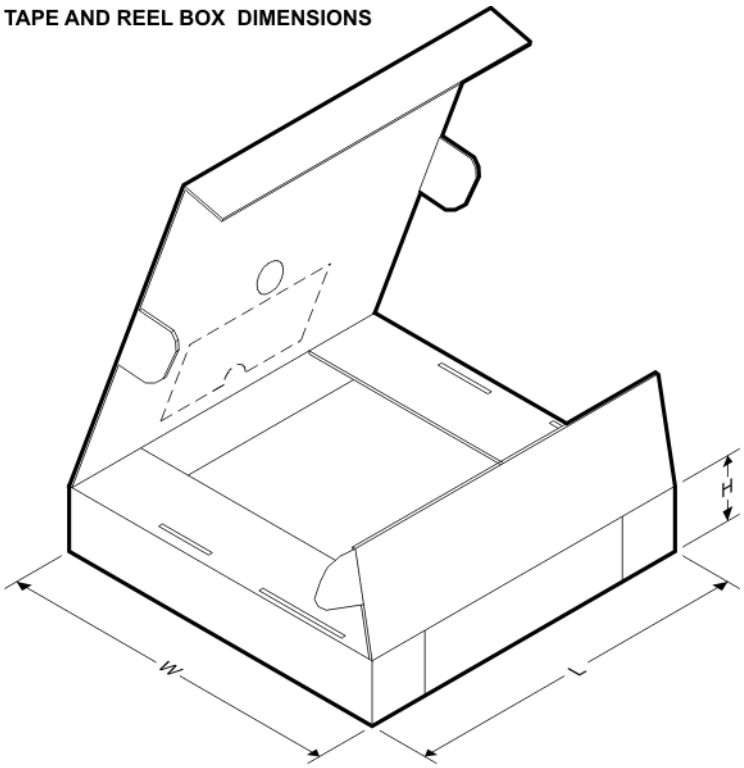
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1115IRGPR	QFN	RGP	20	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TRF1115IRGPT	QFN	RGP	20	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

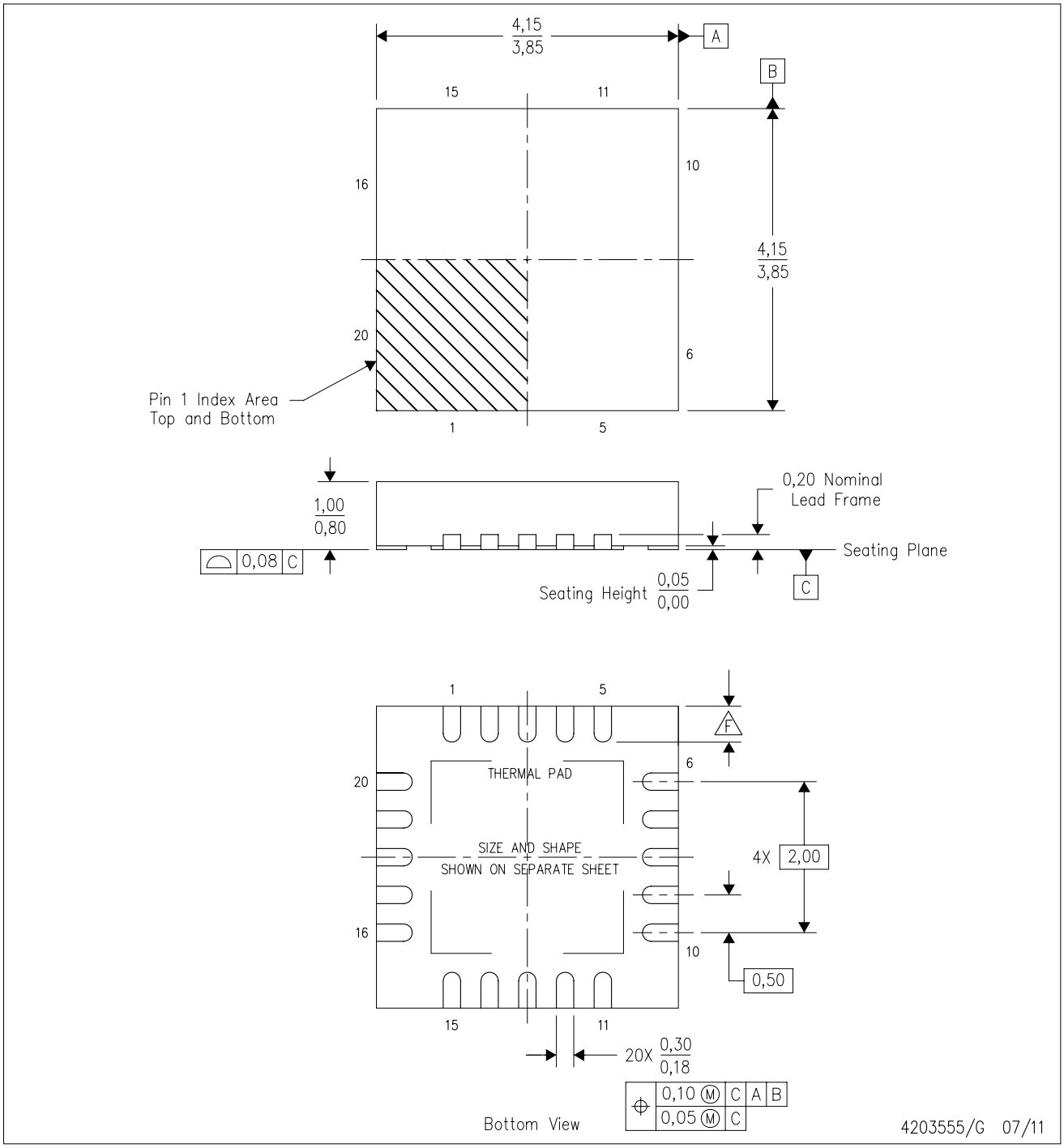
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1115IRGPR	QFN	RGP	20	2500	338.1	338.1	20.6
TRF1115IRGPT	QFN	RGP	20	250	338.1	338.1	20.6

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

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- Подбор аналогов;
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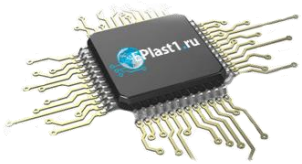
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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