SN74AVCB164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES394D−JUNE 2002−REVISED JUNE 2005

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of $\pm$24 mA at 2.5-V V_{CC}**
- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCB} Voltage**
- **If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**

- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over Full 1.4-V to 3.6-V Power-Supply Range**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DESCRIPTION

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCB164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCB164245 is designed so that the control pins (1DIR, 2DIR, 1$\overline{OE}$, and 2$\overline{OE}$) are supplied by V_{CCB}.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CCB} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, both ports are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	FBGA – GRD	Tape and reel	74AVCB164245GRDR	WB4245
	FBGA – ZRD (Pb-Free)	Tape and reel	74AVCB164245ZRDR	
	TSSOP – DGG	Tape and reel	SN74AVCB164245GR	AVCB164245
	TVSOP – DGV	Tape and reel	SN74AVCB164245VR	WB4245
	VFBGA – GQL	Tape and reel	SN74AVCB164245KR	
	VFBGA – ZQL (Pb-Free)	Tape and reel	74AVCB164245ZQLR	WB4245

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
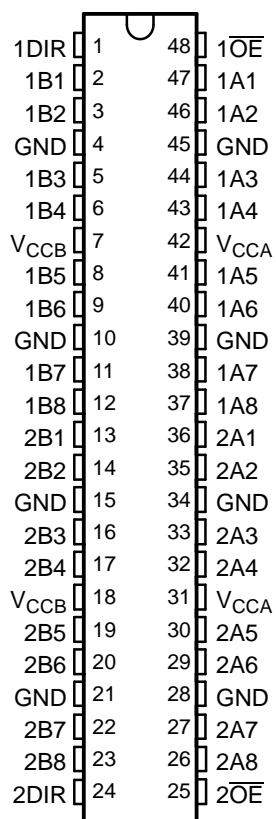
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

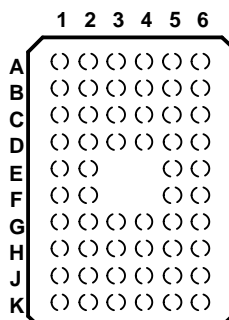Widebus, DOC are trademarks of Texas Instruments.

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TERMINAL ASSIGNMENTS

DGG OR DGV PACKAGE
(TOP VIEW)

Pin	Left		Right	Pin
1	1DIR		$1\overline{OE}$	48
2	1B1		1A1	47
3	1B2		1A2	46
4	GND		GND	45
5	1B3		1A3	44
6	1B4		1A4	43
7	V_{CCB}		V_{CCA}	42
8	1B5		1A5	41
9	1B6		1A6	40
10	GND		GND	39
11	1B7		1A7	38
12	1B8		1A8	37
13	2B1		2A1	36
14	2B2		2A2	35
15	GND		GND	34
16	2B3		2A3	33
17	2B4		2A4	32
18	V_{CCB}		V_{CCA}	31
19	2B5		2A5	30
20	2B6		2A6	29
21	GND		GND	28
22	2B7		2A7	27
23	2B8		2A8	26
24	2DIR		$2\overline{OE}$	25

GQL OR ZQL PACKAGE
(TOP VIEW)

GRD OR ZRD PACKAGE
(TOP VIEW)

TERMINAL ASSIGNMENTS
(56-Ball GQL/ZQL Package)[1]

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{\text{OE}}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CCB}	V_{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{\text{OE}}$

(1) NC - No internal connection
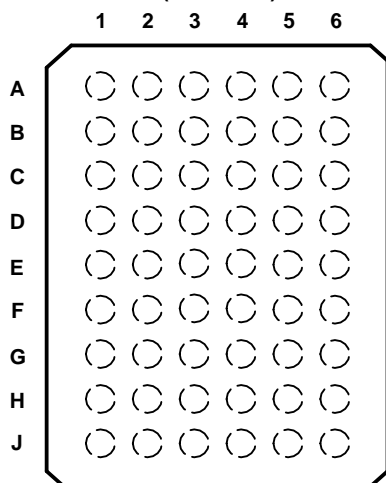
TERMINAL ASSIGNMENTS
(54-Ball GRD/ZRD Package)[1]

	1	2	3	4	5	6
A	1B1	NC	1DIR	1$\overline{\text{OE}}$	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V_{CCB}	V_{CCA}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V_{CCB}	V_{CCA}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2$\overline{\text{OE}}$	NC	2A8

(1) NC - No internal connection

FUNCTION TABLE
(EACH 8-BIT SECTION)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels   To Seven Other Channels
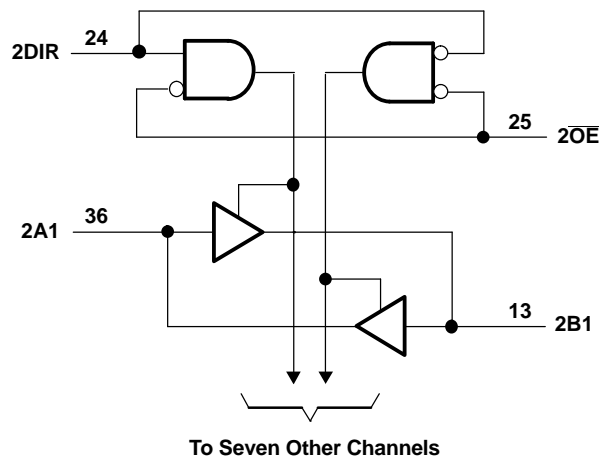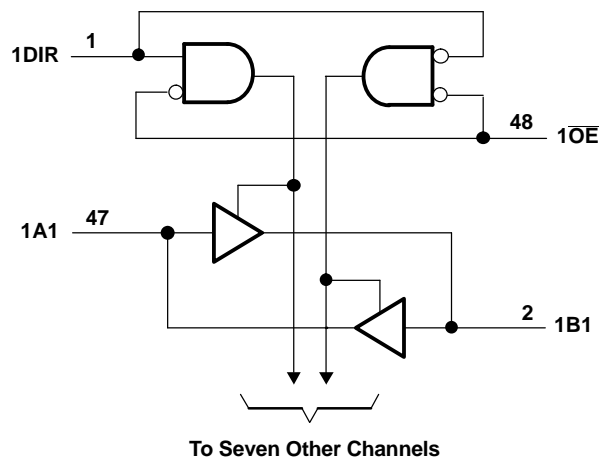
Pin numbers shown are for the DGG and DGV packages.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[2]	I/O ports (A port)	−0.5	4.6	V
		I/O ports (B port)	−0.5	4.6	
		Control inputs	−0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	A port	−0.5	4.6	V
		B port	−0.5	4.6	
V_O	Voltage range applied to any output in the high or low state[2][3]	A port	−0.5	V_{CCA} + 0.5	V
		B port	−0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			100	mA
θ_{JA}	Package thermal impedance[4]	DGG package		70	°C/W
		DGV package		58	
		GQL/ZQL package		28	
		GRD/ZRD package		36	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[(1)(2)(3)]

over operating free-air temperature range (unless otherwise noted)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.4	3.6	V
V_{CCB}	Supply voltage				1.4	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V			$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V		$V_{CCB} \times 0.65$		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V			$V_{CCB} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.4 V to 1.6 V		−2	mA
				1.65 V to 1.95 V		−4	
				2.3 V to 2.7 V		−8	
				3 V to 3.6 V		−12	
I_{OL}	Low-level output current			1.4 V to 1.6 V		2	mA
				1.65 V to 1.95 V		4	
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				−40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the data output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics[1][2]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP[3]	MAX	UNIT
V_{OH}		$I_{OH} = -100$ µA	$V_I = V_{IH}$	1.4 V to 3.6 V	1.4 V to 3.6 V	$V_{CCO} - 0.2$			V
		$I_{OH} = -2$ mA	$V_I = V_{IH}$	1.4 V	1.4 V	1.05			
		$I_{OH} = -4$ mA	$V_I = V_{IH}$	1.65 V	1.65 V	1.2			
		$I_{OH} = -8$ mA	$V_I = V_{IH}$	2.3 V	2.3 V	1.75			
		$I_{OH} = -12$ mA	$V_I = V_{IH}$	3 V	3 V	2.3			
V_{OL}		$I_{OH} = 100$ µA	$V_I = V_{IL}$	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	V
		$I_{OH} = 2$ mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35	
		$I_{OH} = 4$ mA	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	
		$I_{OH} = 8$ mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.55	
		$I_{OH} = 12$ mA	$V_I = V_{IL}$	3 V	3 V			0.7	
I_I	Control inputs	$V_I = V_{CCB}$ or GND		1.4 V to 3.6 V	3.6 V			±2.5	µA
I_{off}	A port	V_I or $V_O = 0$ to 3.6 V		0 V	0 to 3.6 V			±10	µA
	B port			0 to 3.6 V	0 V			±10	
I_{OZ}[4]	A or B ports	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V			±12.5	µA
	B port		$\overline{OE}$ = don't care	0 V	3.6 V			±12.5	
	A port			3.6 V	0 V			±12.5	
I_{CCA}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.6 V	1.6 V			20	µA
				1.95 V	1.95 V			20	
				2.7 V	2.7 V			30	
				0 V	3.6 V			−40	
				3.6 V	0 V			40	
				3.6 V	3.6 V			40	
I_{CCB}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.6 V	1.6 V			20	µA
				1.95 V	1.95 V			20	
				2.7 V	2.7 V			30	
				0 V	3.6 V			40	
				3.6 V	0 V			−40	
				3.6 V	3.6 V			40	
C_i	Control inputs	$V_I = 3.3$ V or GND		3.3 V	3.3 V		4		pF
C_{io}	A or B ports	$V_O = 3.3$ V or GND		3.3 V	3.3 V		5		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) All typical values are at $T_A = 25°C$.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V 0.1 V		V_{CCB} = 1.8 V 0.15 V		V_{CCB} = 2.5 V 0.2 V		V_{CCB} = 3.3 V 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t_{en}	$\overline{OE}$	A	2.5	8.4	2.4	7.4	2.1	5.2	1.9	4.2	ns
		B	2.1	9	2.9	9.8	3.2	10	3	9.8	
t_{dis}	$\overline{OE}$	A	2.2	6.9	2.3	6.1	1.3	3.6	1.3	3	ns
		B	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V 0.1 V		V_{CCB} = 1.8 V 0.15 V		V_{CCB} = 2.5 V 0.2 V		V_{CCB} = 3.3 V 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t_{en}	$\overline{OE}$	A	2.6	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
t_{dis}	$\overline{OE}$	A	2.3	7	2.3	6.1	1.3	3.6	1.3	3	ns
		B	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V 0.1 V		V_{CCB} = 1.8 V 0.15 V		V_{CCB} = 2.5 V 0.2 V		V_{CCB} = 3.3 V 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t_{en}	$\overline{OE}$	A	3.1	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
t_{dis}	$\overline{OE}$	A	2.4	7	3	6.1	1.4	3.6	1.2	3	ns
		B	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V 0.1 V		V_{CCB} = 1.8 V 0.15 V		V_{CCB} = 2.5 V 0.2 V		V_{CCB} = 3.3 V 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	$\overline{OE}$	A	2.6	8.3	2.5	7.4	2.2	5.2	1.9	4.1	ns
		B	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
t_{dis}	$\overline{OE}$	A	2.3	7	3	6	1.3	3.5	1.2	3.5	ns
		B	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	

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Operating Characteristics

V_{CCA} and V_{CCB} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdA} (V_{CCA})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	
C_{pdB} (V_{CCB})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	20	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		14	
		Outputs disabled		7	

Output Description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.
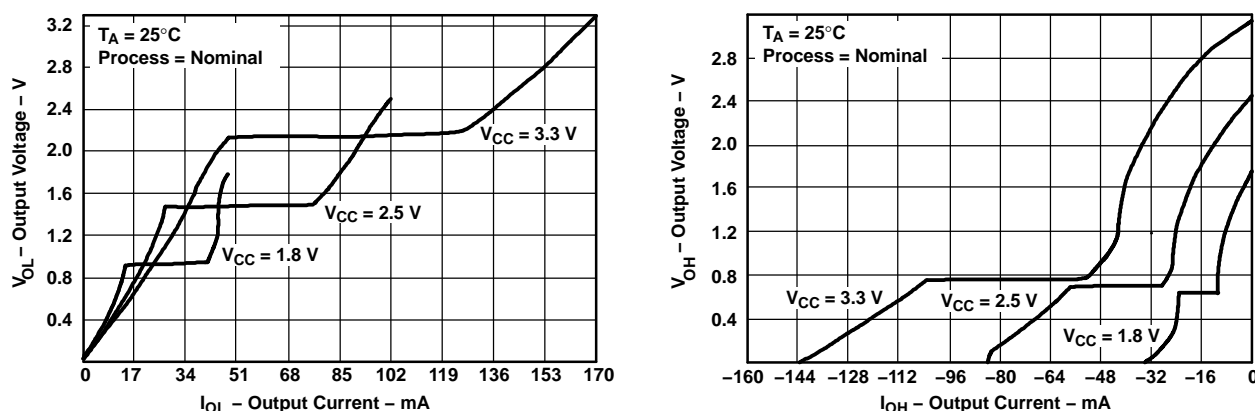
Figure 1. Typical Output Voltage vs Output Current

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND
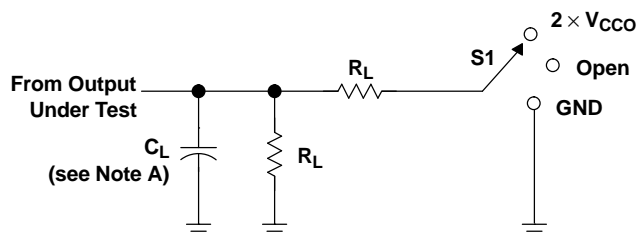
V_{CCO}	C_L	R_L	V_{TP}
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	30 pF	500 Ω	0.3 V
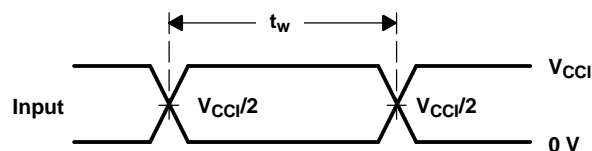
**VOLTAGE WAVEFORMS
PULSE DURATION**
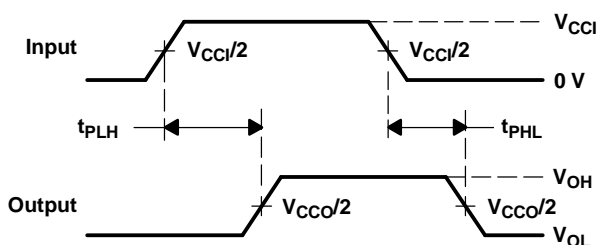
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**
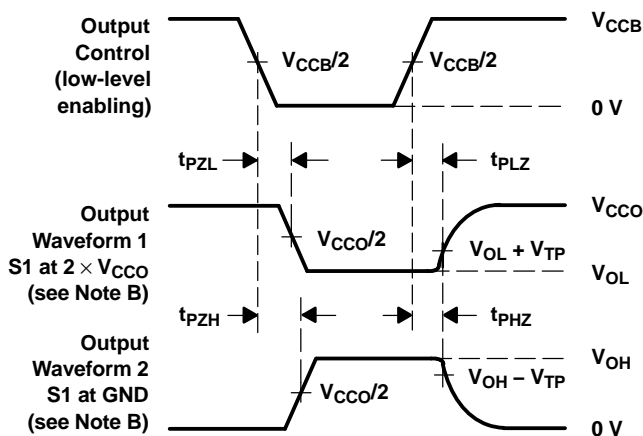
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74AVCB164245GRDR	OBSOLETE	BGA MICROSTAR JUNIOR	GRD	54		TBD	Call TI	Call TI	-40 to 85	WB4245	
74AVCB164245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCB164245	Samples
74AVCB164245GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCB164245	Samples
74AVCB164245VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WB4245	Samples
74AVCB164245VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WB4245	Samples
74AVCB164245ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WB4245	Samples
74AVCB164245ZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WB4245	Samples
SN74AVCB164245GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCB164245	Samples
SN74AVCB164245KR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	WB4245	
SN74AVCB164245VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WB4245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN74AVCB164245 :

- Automotive: SN74AVCB164245-Q1

- Enhanced Product: SN74AVCB164245-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVCB164245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
74AVCB164245ZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1
SN74AVCB164245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AVCB164245VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVCB164245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6
74AVCB164245ZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	336.6	336.6	28.6
SN74AVCB164245GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AVCB164245VR	TVSOP	DGV	48	2000	367.0	367.0	38.0

ZQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY

4,60
4,40   B

A

7,10
6,90

A1 Corner

1,00 Max

0,35
0,15

Seating Plane

C

3,25

0,65

0,325

K
J
H
G
F
E
D
C
B
A

3X Via Hole
Without Ball

Missing Via Hole
Indicates Pin A1
Quadrant

1   2   3   4   5   6

Bottom View

0,65

5,85

0,325

56X Ø 0,45
       0,35

⌖ | Ø 0,15 Ⓜ | C | A | B
  | Ø 0,08 Ⓜ | C

0,10 C

4204437−3/H 11/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−285 variation BA−2.
         D.   This package is Pb−free. Refer to the 56 GQL package (drawing 4200583) for tin−lead (SnPb).

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GRD (R−PBGA−N54)   PLASTIC BALL GRID ARRAY

5,60
5,40

8,10
7,90

A1 Corner

4,00

0,80

0,40

J
H
G
F
E
D
C
B
A

0,80

6,40

1   2   3   4   5   6

Bottom View

△C 0,80
    0,70

1,20 Max

54X Ø 0,55
        0,45

⊕ Ø 0,08 Ⓜ

⌒ 0,10

Seating Plane

0,45
0,35

4204759/B 06/04

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
     △C   Falls within JEDEC MO−205 variation DD.
         D.   This package is tin−lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead−free.

ZRD (R–PBGA–N54)   PLASTIC BALL GRID ARRAY
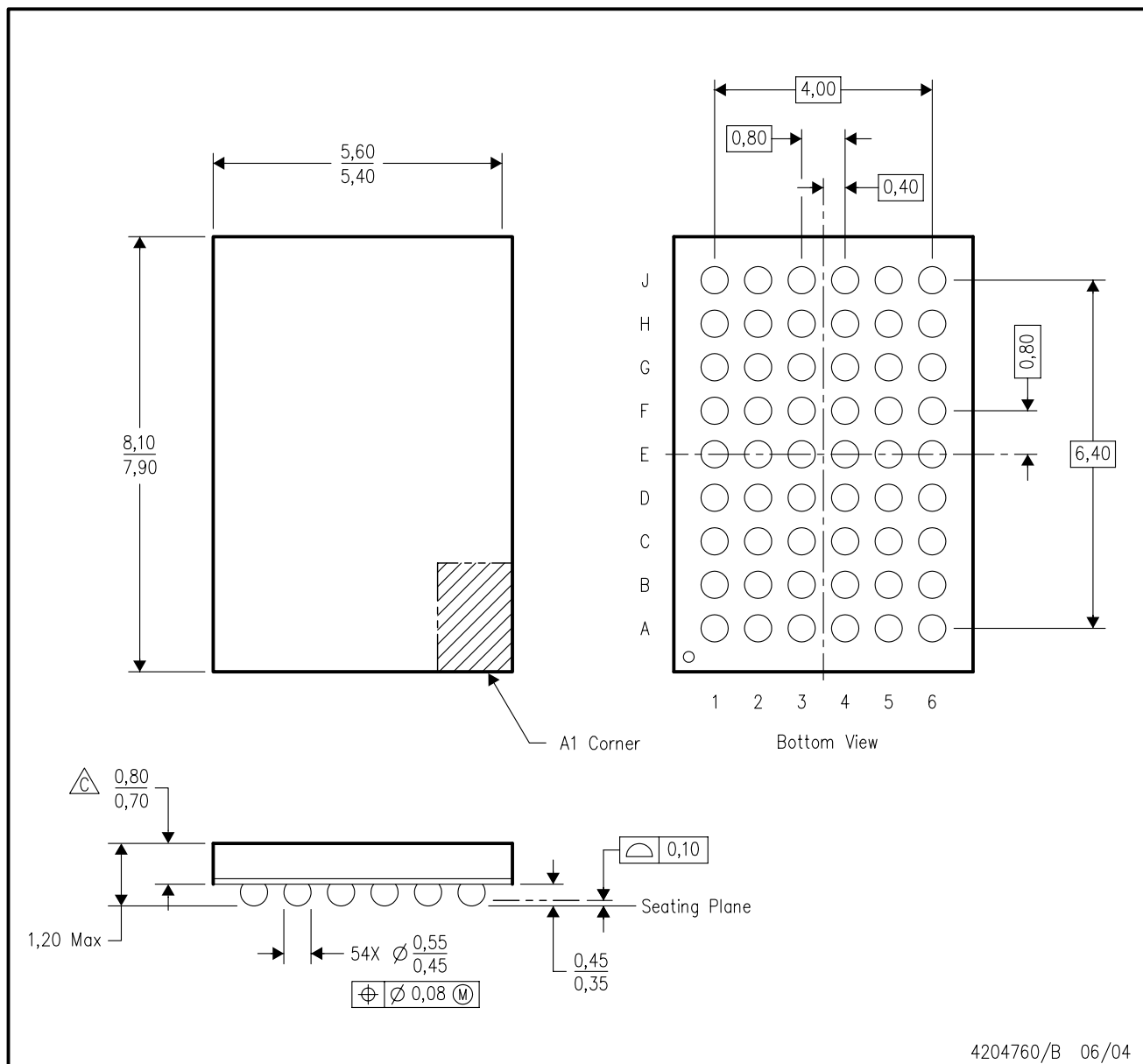
5,60
5,40

8,10
7,90

A1 Corner

4,00

0,80

0,40

J
H
G
F
E
D
C
B
A

1 2 3 4 5 6

Bottom View

0,80

6,40

C 0,80
   0,70

1,20 Max

54X Ø 0,55
        0,45

⊕ Ø 0,08 Ⓜ

0,10

Seating Plane

0,45
0,35

4204760/B 06/04

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO–205 variation DD.
         D.   This package is lead–free. Refer to the 54 GRD package (drawing 4204759) for tin–lead (SnPb).

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

DIM	PINS **	14	16	20	24	38	48	56
A MAX		3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN		3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GQL (R−PBGA−N56) PLASTIC BALL GRID ARRAY

4,60 / 4,40 B

A

7,10 / 6,90

3X Via Hole Without Ball

Missing Via Hole Indicates Pin A1 Quadrant

A1 Corner

3,25

0,65

0,325

K J H G F E D C B A

1 2 3 4 5 6

Bottom View

0,65

5,85

0,325

56X Ø 0,45 / 0,35

⊕	Ø 0,15 Ⓜ	C	A	B
	Ø 0,08 Ⓜ	C		

1,00 Max

0,10 C

Seating Plane

0,35 / 0,15

C

4200583−3/K 06/2007

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
   B. This drawing is subject to change without notice.
   C. Falls within JEDEC MO−285 variation BA−2.
   D. This package is tin−lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead−free.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold protrusion not to exceed 0,15.
           D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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