

### Driver Characteristics

| Parameter                        | Rating  | Units |
|----------------------------------|---------|-------|
| $V_{\text{OFFSET}}$              | 600     | V     |
| $I_{\text{O} \pm}$ (Source/Sink) | 2/2     | A     |
| $V_{\text{OUT}}$                 | 10-20   | V     |
| $t_{\text{on}}/t_{\text{off}}$   | 113/100 | ns    |
| Delay Matching (Max)             | 20      | ns    |

### Features

- Floating Channel for Bootstrap Operation to +600V with Absolute Maximum Rating of +700V
- Outputs Capable of Sourcing and Sinking 2A
- Gate Drive Supply Range From 10V to 20V
- Enhanced Robustness due to SOI Process
- Tolerant to Negative Voltage Transients:  $dV/dt$  Immune
- 3.3V Logic Compatible
- Undervoltage Lockout for Both High-side and Low-Side Outputs
- Matched Propagation Delays

### Description

The IX2113 is a high voltage integrated circuit that can drive high speed MOSFETs and IGBTs that operate at up to +600V. The IX2113 is configured with independent high-side and low-side referenced output channels, both of which can source and sink 2A. The floating high-side channel can drive an N-channel power MOSFET or IGBT 600V from the common reference.

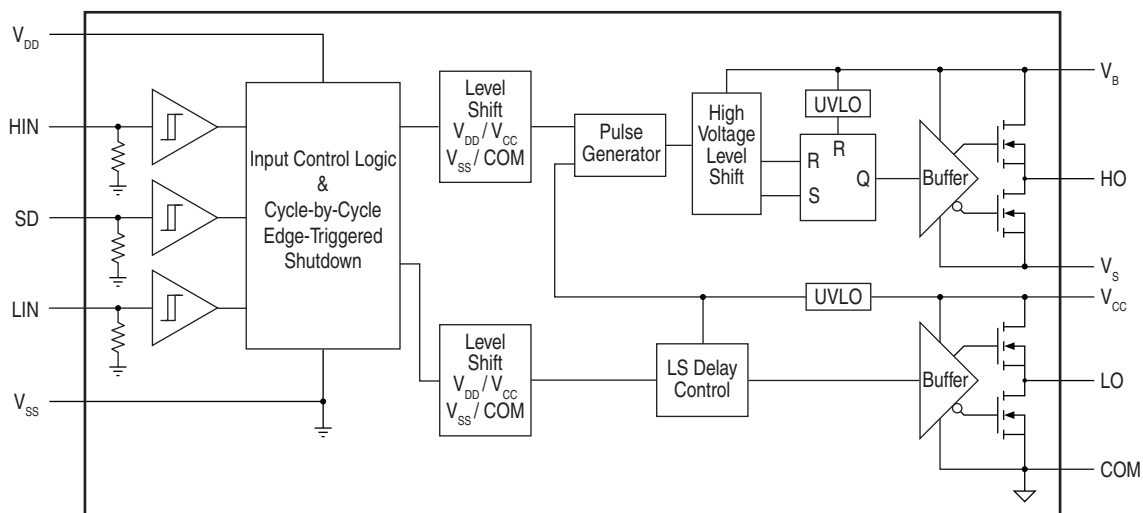
Manufactured on IXYS Integrated Circuits Division's proprietary high-voltage BCDMOS on SOI (silicon on insulator) process, the IX2113 is extremely robust, and is virtually immune to negative transients. The UVLO circuit prevents the turn-on of the MOSFET or IGBT until there is sufficient  $V_{\text{BS}}$  or  $V_{\text{CC}}$  supply voltage. Propagation delays are matched for use in high frequency applications.

The IX2113 is available in a 14-pin DIP package and in a 16-pin SOIC package.

### Ordering Information

| Part      | Description             |
|-----------|-------------------------|
| IX2113G   | 14-Pin DIP (25/Tube)    |
| IX2113B   | 16-Pin SOIC (50/Tube)   |
| IX2113BTR | 16-Pin SOIC (1000/Reel) |

### IX2113 Functional Block Diagram

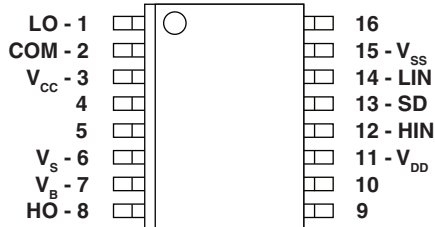


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# 1 Specifications

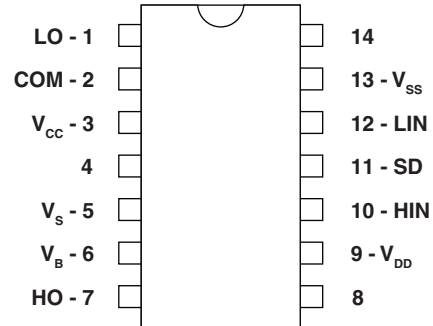
## 1.1 Package Pinout: 16-Pin SOIC Package



## 1.2 Pin Description: 16-Pin SOIC Package

| Pin# | Name            | Description   |
|------|-----------------|---|
| 1    | LO              | Low-Side Gate Drive Output                                  |
| 2    | COM             | Low-Side Return   |
| 3    | V <sub>CC</sub> | Low-Side Supply   |
| 4    | -               | No Connection   |
| 5    | -               | No Connection   |
| 6    | V <sub>S</sub>  | High-Side Floating Supply Return                            |
| 7    | V <sub>B</sub>  | High-Side Floating Supply                                   |
| 8    | HO              | High-Side Gate Drive Output                                 |
| 9    | -               | No Connection   |
| 10   | -               | No Connection   |
| 11   | V <sub>DD</sub> | Logic Supply  |
| 12   | HIN             | Logic Input for High-Side Gate Driver Output (HO), In-Phase |
| 13   | SD              | Logic Input for Shutdown                                    |
| 14   | LIN             | Logic Input for Low-Side Gate Driver Output (LO), In-Phase  |
| 15   | V <sub>SS</sub> | Logic Ground  |
| 16   | -               | No Connection   |

## 1.3 Package Pinout: 14-Pin DIP Package



## 1.4 Pin Description: 14-Pin DIP Package

| Pin# | Name            | Description   |
|------|-----------------|---|
| 1    | LO              | Low-Side Gate Drive Output                                  |
| 2    | COM             | Low-Side Return   |
| 3    | V <sub>CC</sub> | Low-Side Supply   |
| 4    | -               | No Connection   |
| 5    | V <sub>S</sub>  | High-Side Floating Supply Return                            |
| 6    | V <sub>B</sub>  | High-Side Floating Supply                                   |
| 7    | HO              | High-Side Gate Drive Output                                 |
| 8    | -               | No Connection   |
| 9    | V <sub>DD</sub> | Logic Supply  |
| 10   | HIN             | Logic Input for High-Side Gate Driver Output (HO), In-Phase |
| 11   | SD              | Logic Input for Shutdown                                    |
| 12   | LIN             | Logic Input for Low-Side Gate Driver Output (LO), In-Phase  |
| 13   | V <sub>SS</sub> | Logic Ground  |
| 14   | -               | No Connection   |

### 1.5 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board-mounted and still-air conditions.

| Parameter   | Symbol      | Min             | Max          | Units            |                    |
|---|-------------|-----------------|--------------|------------------|--------------------|
| High-Side Floating Supply Voltage                       | $V_B$       | -0.3            | 700          | V                |                    |
| High-Side Floating Supply Offset Voltage                | $V_S$       | $V_B-20$        | $V_B+0.3$    | V                |                    |
| High-Side Floating Output Voltage                       | $V_{HO}$    | $V_S-0.3$       | $V_B+0.3$    | V                |                    |
| Low-Side Fixed Supply Voltage                           | $V_{CC}$    | -0.3            | 20           | V                |                    |
| Low-Side Output Voltage                                 | $V_{LO}$    | -0.3            | $V_{CC}+0.3$ | V                |                    |
| Logic Supply Voltage                                    | $V_{DD}$    | -0.3            | $V_{SS}+20$  | V                |                    |
| Logic Supply Offset Voltage                             | $V_{SS}$    | $V_{CC}-20$     | $V_{CC}+0.3$ | V                |                    |
| Logic Input Voltage (HIN, LIN, SD)                      | $V_{IN}$    | $V_{SS}-0.3$    | $V_{DD}+0.3$ | V                |                    |
| Allowable Offset Supply Voltage Transient               | $dV_S/dt$   | -               | 50           | V/ns             |                    |
| Package Power Dissipation @ $T_A \leq 25^\circ\text{C}$ | 16-Pin SOIC | PD              | -            | 1.25             | W                  |
|   | 14-Pin DIP  |                 | -            | 1.6              |                    |
| Thermal Resistance, Junction to Ambient                 | 16-Pin SOIC | $R_{\theta JA}$ | -            | 100              | $^\circ\text{C/W}$ |
|   | 14-Pin DIP  |                 | -            | 75               |                    |
| Junction Temperature                                    | $T_J$       | -               | 150          | $^\circ\text{C}$ |                    |
| Storage Temperature                                     | $T_S$       | -55             | 150          | $^\circ\text{C}$ |                    |
| Lead Temperature (Soldering, 10 Seconds)                | $T_L$       | -               | 300          | $^\circ\text{C}$ |                    |

### 1.6 Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. The  $V_S$  and  $V_{SS}$  offset ratings are tested with all supplies biased at a 15V differential.

| Parameter                                  | Symbol   | Min        | Max         | Units            |
|--|----------|------------|-------------|------------------|
| High-Side Floating Supply Absolute Voltage | $V_B$    | $V_S+10$   | $V_S+20$    | V                |
| High-Side Floating Supply Offset Voltage   | $V_S$    | -          | 600         |                  |
| High-Side Floating Output Voltage          | $V_{HO}$ | $V_S$      | $V_B$       |                  |
| Low-Side Fixed Supply Voltage              | $V_{CC}$ | 10         | 20          |                  |
| Low-Side Output Voltage                    | $V_{LO}$ | 0          | $V_{CC}$    |                  |
| Logic Supply Voltage                       | $V_{DD}$ | $V_{SS}+3$ | $V_{SS}+20$ |                  |
| Logic Supply Offset Voltage                | $V_{SS}$ | -5         | 5           |                  |
| Logic Input Voltage (HIN, LIN, SD)         | $V_{IN}$ | $V_{SS}$   | $V_{DD}$    |                  |
| Ambient Temperature                        | $T_A$    | -40        | +125        | $^\circ\text{C}$ |

**1.7 Dynamic Electrical Characteristics**
 $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ )=15V,  $C_L$ =1000 pF,  $T_A$ =25°C, and  $V_{SS}$ =COM unless otherwise specified.

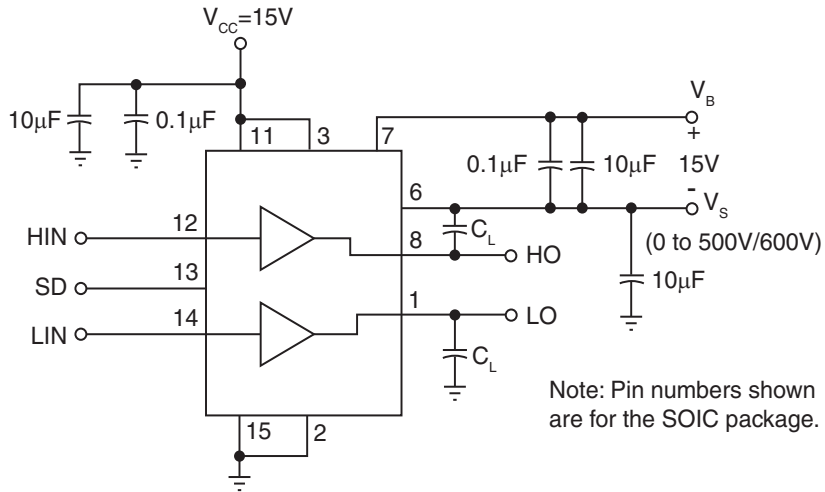
| Parameter                           | Conditions | Symbol    | Min | Typ | Max | Units |
|-------------------------------------|------------|-----------|-----|-----|-----|-------|
| Turn-On propagation Delay           | $V_S=0V$   | $t_{on}$  | -   | 113 | 160 | ns    |
| Turn-Off propagation Delay          | $V_S=600V$ | $t_{off}$ | -   | 100 | 150 |       |
| Shutdown propagation Delay          |            | $t_{SD}$  | -   | 94  | 160 |       |
| Turn-On Rise Time                   | -          | $t_r$     | -   | 9.4 | 35  |       |
| Turn-Off Fall Time                  | -          | $t_f$     | -   | 9.7 | 25  |       |
| Delay Matching, HS & LS Turn-On/Off | -          | MT        | -   | -   | 20  |       |

**1.8 Static Electrical Characteristics**
 $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ )=15V,  $T_A$ =25°C and  $V_{SS}$ =COM unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input leads: HIN, LIN, and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

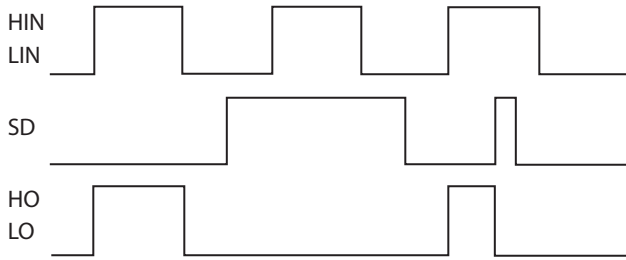
| Parameter   | Conditions                                     | Symbol      | Min | Typ | Max  | Units   |
|---|--|-------------|-----|-----|------|---------|
| Logic "1" Input Voltage                               | $V_{DD}=15V$                                   | $V_{IH}$    | 9.5 | -   | -    | V       |
| Logic "0" Input Voltage                               |  | $V_{IL}$    | -   | -   | 6    |         |
| Logic "1" Input Voltage                               | $V_{DD}=3V$                                    | $V_{IH}$    | 2.5 | -   | -    | V       |
| Logic "0" Input Voltage                               |  | $V_{IL}$    | -   | -   | 0.8  |         |
| High-Level Output Voltage, $V_{BIAS}-V_O$             | $I_O=0A$                                       | $V_{OH}$    | -   | 1.6 | 2.5  | V       |
| Low-Level Output Voltage, $V_O$                       | $I_O=20mA$                                     | $V_{OL}$    | -   | -   | 0.15 |         |
| Offset Supply Leakage Current                         | $V_B=V_S=600V$                                 | $I_{LK}$    | -   | -   | 60   | $\mu A$ |
| Quiescent $V_{BS}$ Supply Current                     | $V_{IN}=0V$ or $V_{DD}$                        | $I_{QBS}$   | -   | 187 | 310  |         |
| Quiescent $V_{CC}$ Supply Current                     | $V_{IN}=0V$ or $V_{DD}$                        | $I_{QCC}$   | -   | 300 | 420  |         |
| Quiescent $V_{DD}$ Supply Current                     | $V_{IN}=0V$ or $V_{DD}$                        | $I_{QDD}$   | -   | -   | 1    |         |
| Logic "1" Input Bias Current                          | $V_{IN}=V_{DD}$                                | $I_{IN+}$   | -   | 22  | 40   | $\mu A$ |
| Logic "0" Input Bias Current                          | $V_{IN}=0V$                                    | $I_{IN-}$   | -   | -   | 5    |         |
| $V_{BB}$ Supply Undervoltage Positive Going Threshold | -  | $V_{BSUV+}$ | 7.5 | 8.4 | 9.7  | V       |
| $V_{BB}$ Supply Undervoltage Negative Going Threshold | -  | $V_{BSUV-}$ | 7   | 7.8 | 9.4  |         |
| $V_{CC}$ Supply Undervoltage Positive Going Threshold | -  | $V_{CCUV+}$ | 7.4 | 8.4 | 9.6  |         |
| $V_{CC}$ Supply Undervoltage Negative Going Threshold | -  | $V_{CCUV-}$ | 7   | 7.8 | 9.4  |         |
| Output High Short Circuit Pulsed Current              | $V_O=0V$ , $V_{IN}=V_{DD}$ , $PW \leq 10\mu s$ | $I_{O+}$    | 2   | 2.5 | -    | A       |
| Output Low Short Circuit Pulsed Current               | $V_O=15V$ , $V_{IN}=0V$ , $PW \leq 10\mu s$    | $I_{O-}$    | 2   | 2.5 | -    |         |

1.9 Test Waveforms

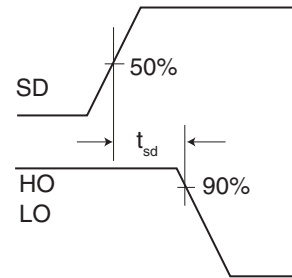
1.9.1 Switching Time Test Circuit



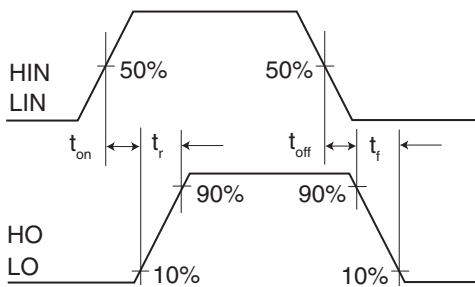
1.9.2 Input/Output Timing Diagram



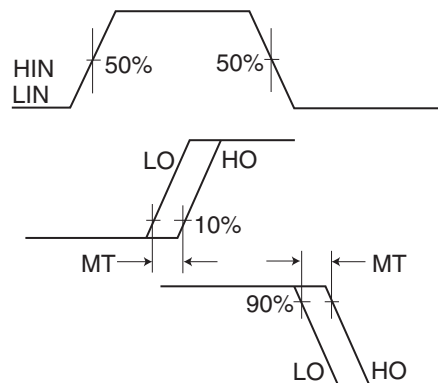
1.9.4 Shutdown Waveform Definitions



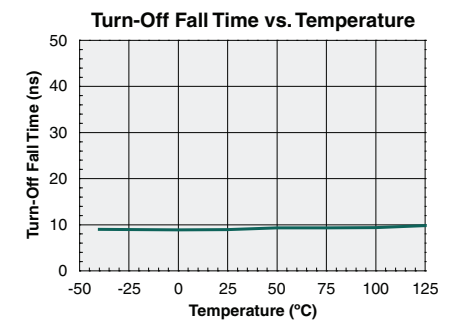
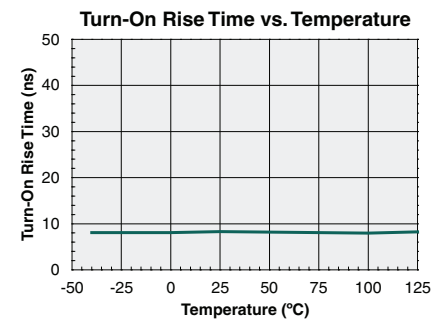
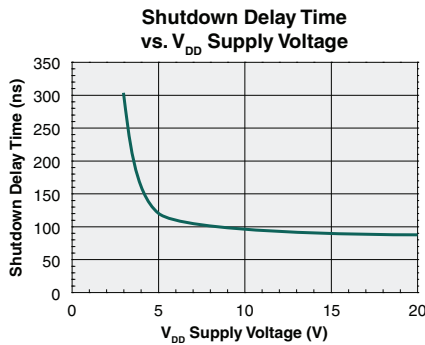
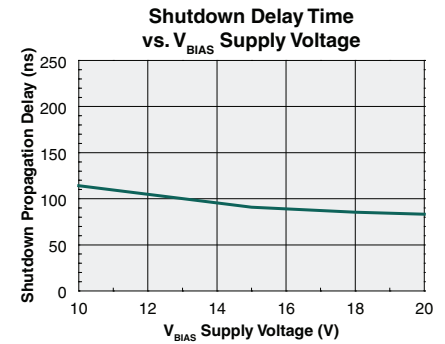
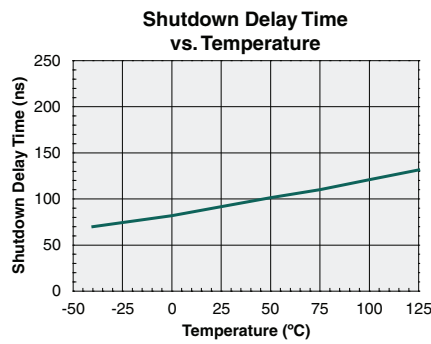
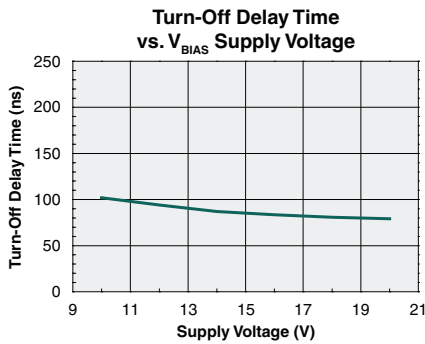
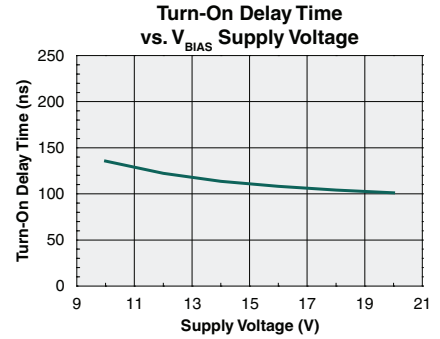
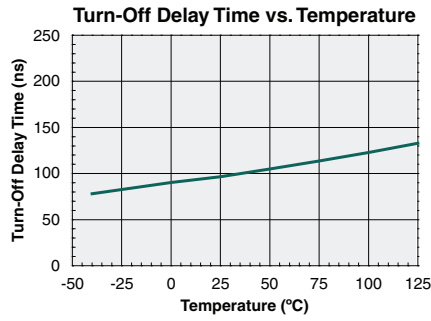
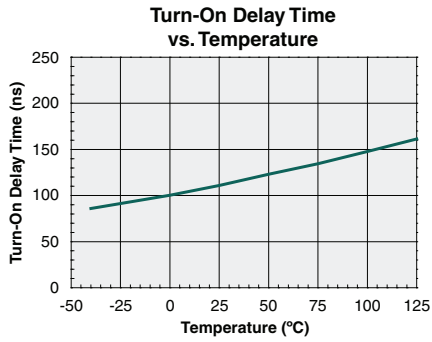
1.9.3 Switching Time Waveform Definition

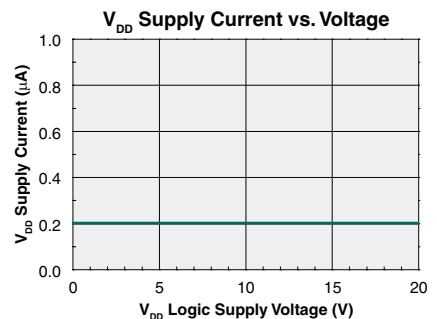
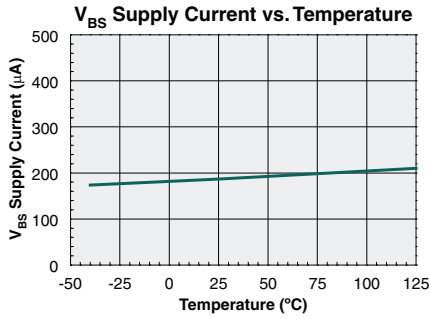
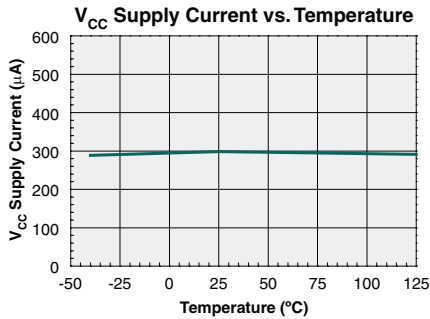
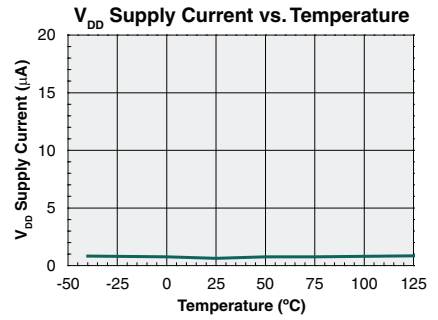
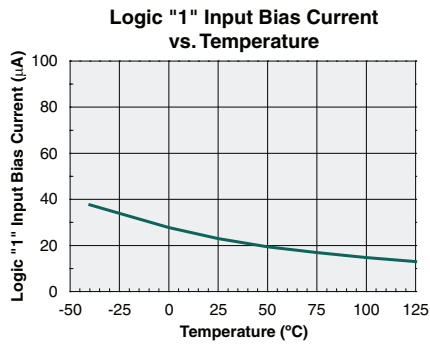
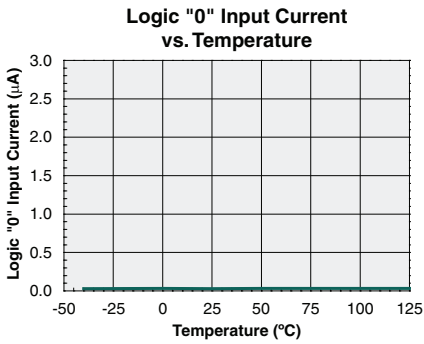
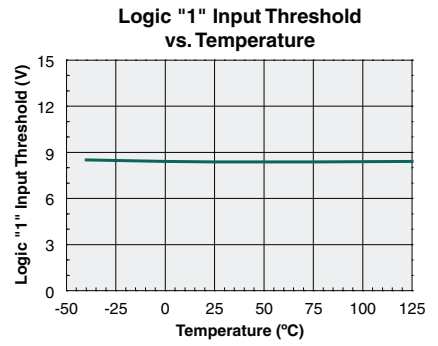
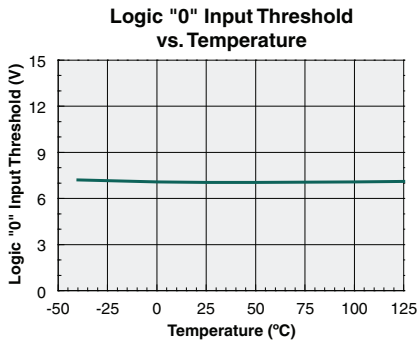
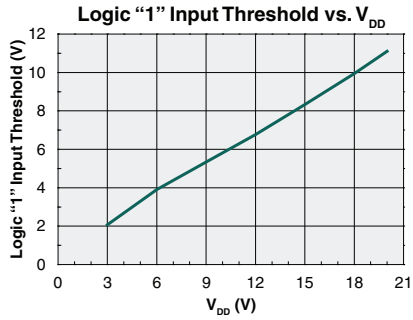
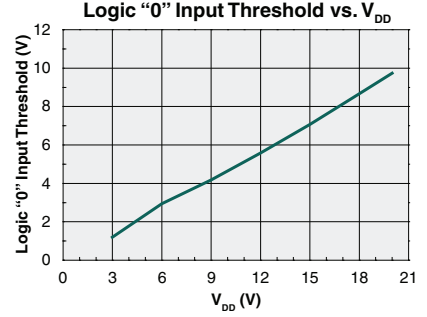
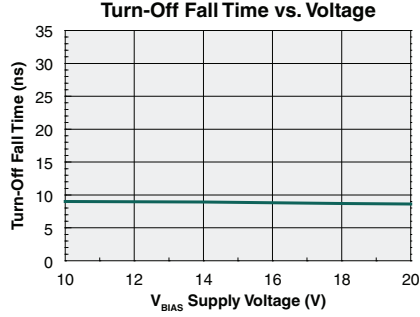
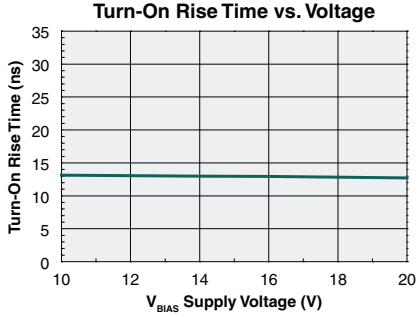


1.9.5 Delay Matching Waveform Definitions

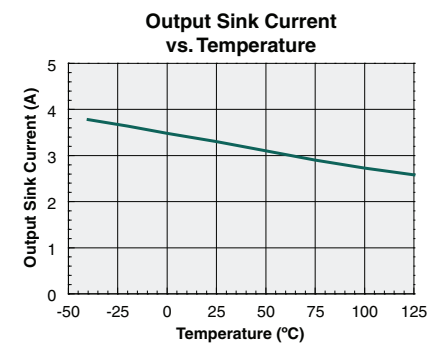
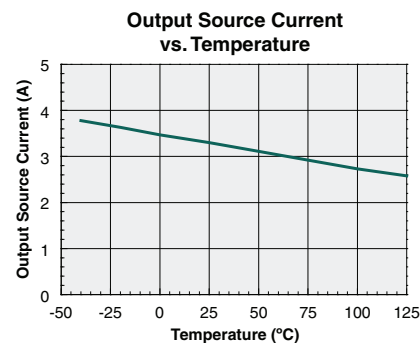
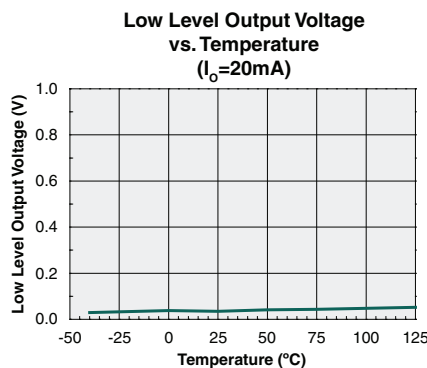
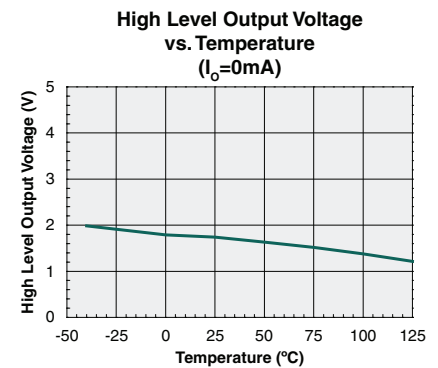
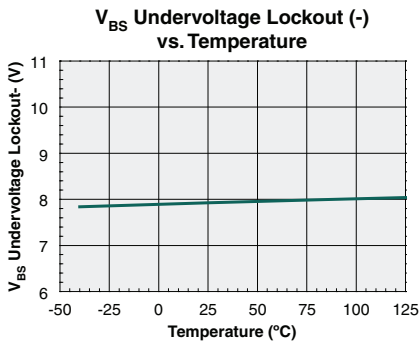
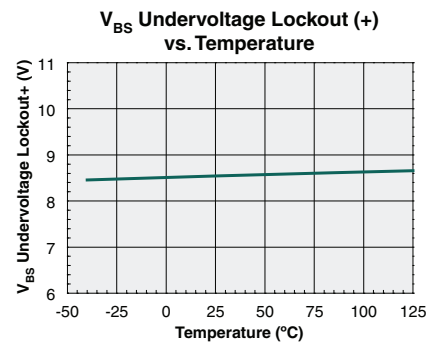
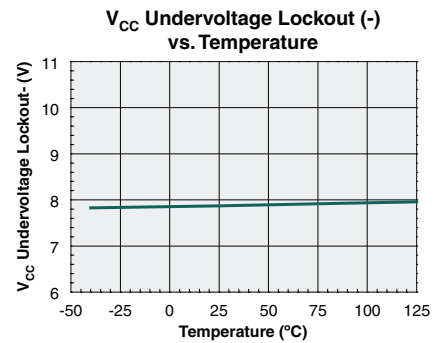
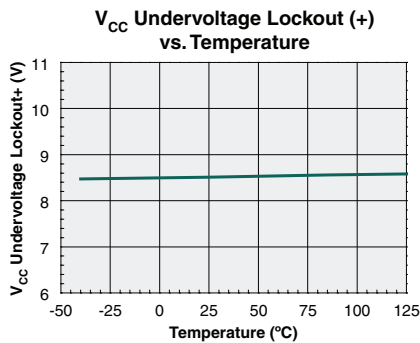
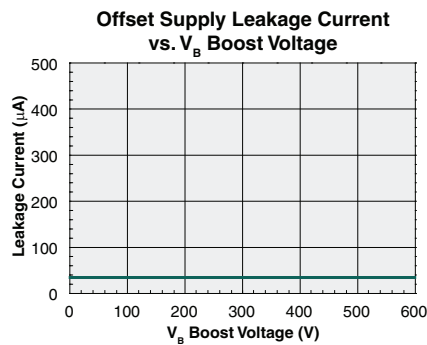
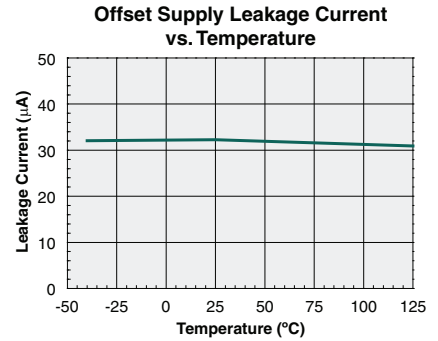
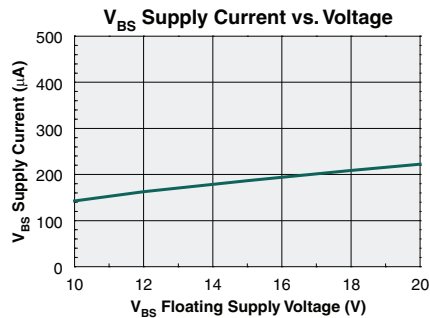
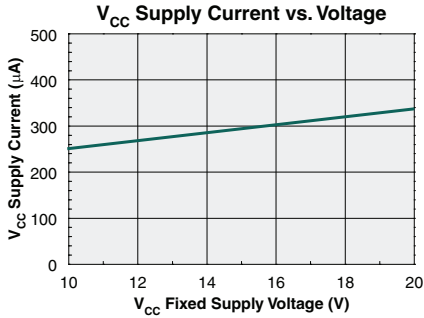


2 Typical Performance Data









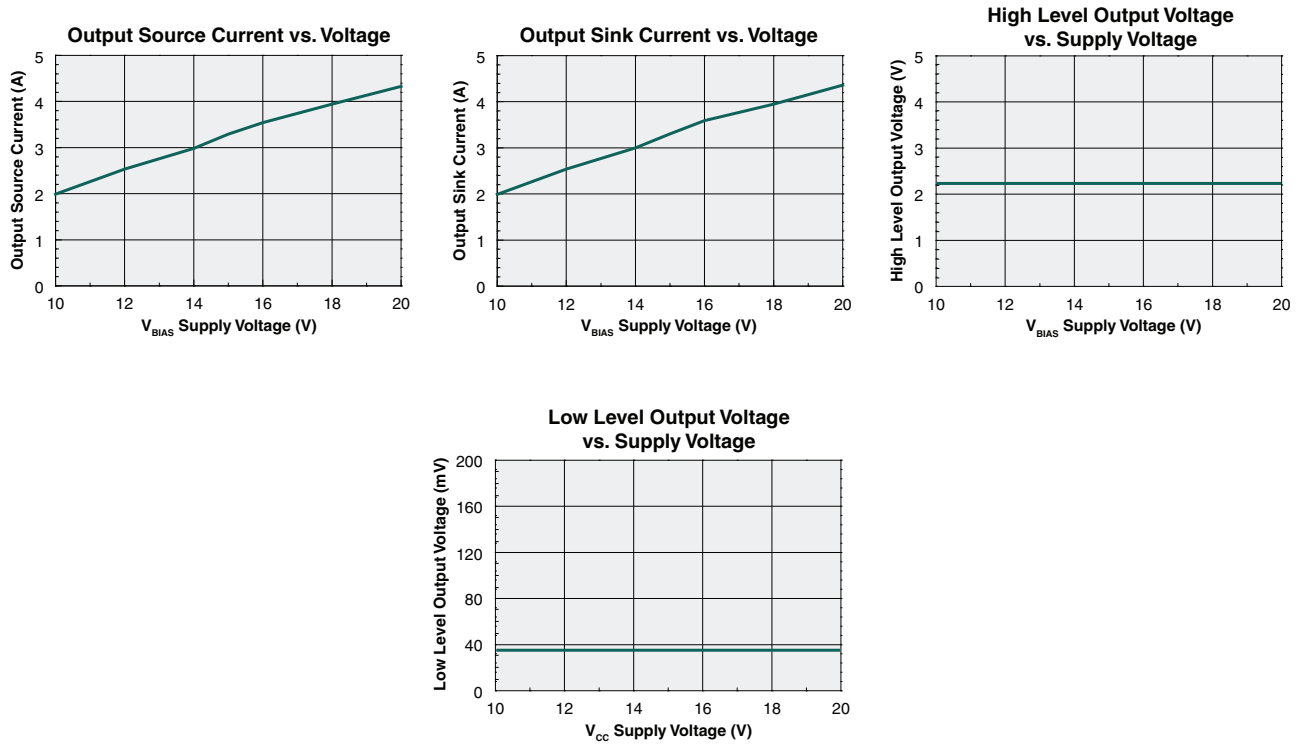
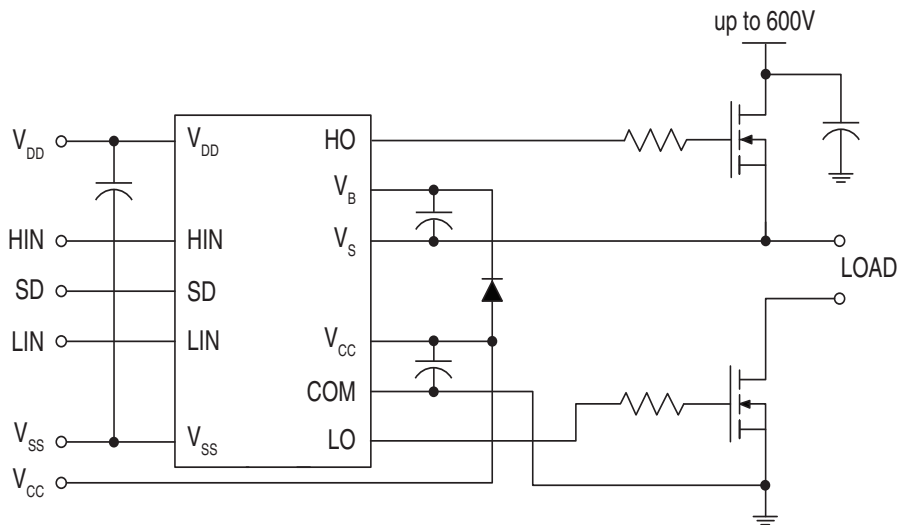


Figure 1. Typical Connection Diagram



### 3 Manufacturing Information

#### 3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

| Device           | Moisture Sensitivity Level (MSL) Rating |
|------------------|---|
| IX2113B, IX2113G | MSL 1                                   |

#### 3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

#### 3.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

| Device  | Maximum Temperature x Time |
|---------|----------------------------|
| IX2113B | 260°C for 30 seconds       |
| IX2113G | 245°C for 30 seconds       |

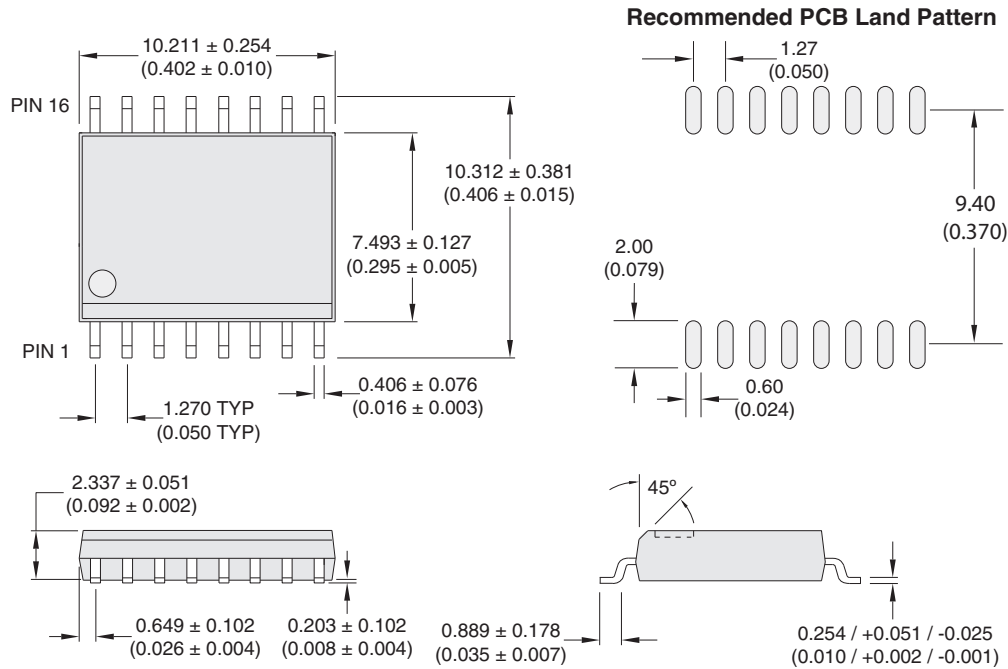
#### 3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.



### 3.5 Mechanical Dimensions

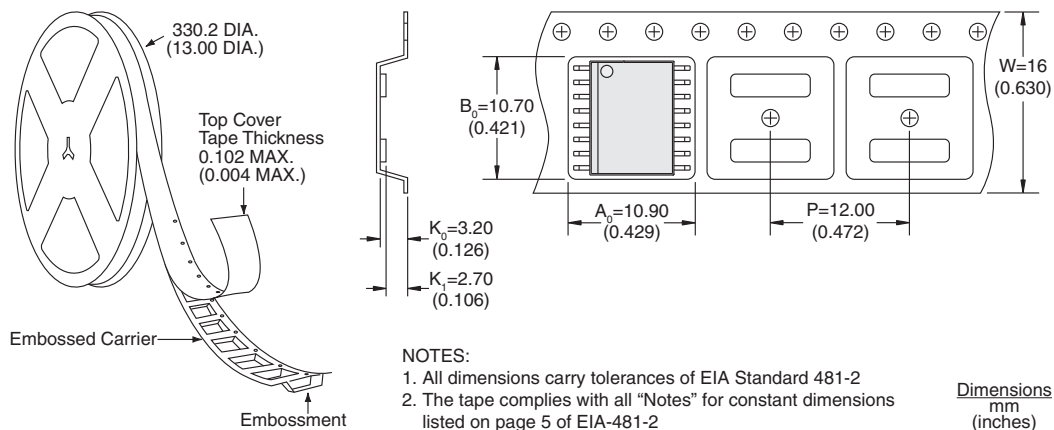
#### 3.5.1 IX2113B: 16-Pin SOIC Package



- NOTES:
1. Coplanarity = 0.1016 (0.004) max.
  2. Leadframe thickness does not include solder plating (1000 microinch maximum).

**DIMENSIONS**  
mm  
(inches)

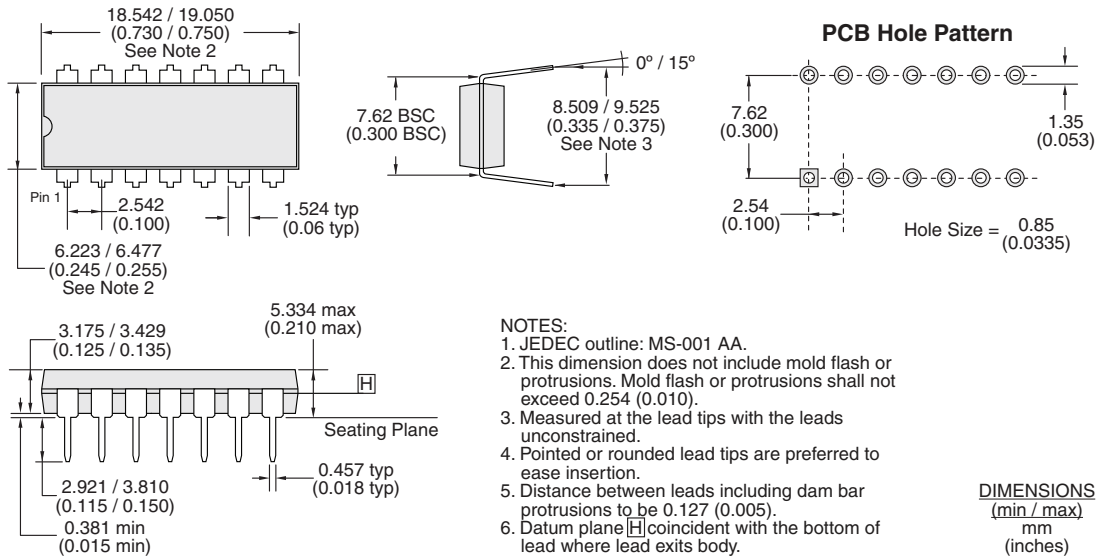
#### 3.5.2 IX2113BTR: Tape & Reel Packaging for 16-Pin SOIC Package



- NOTES:
1. All dimensions carry tolerances of EIA Standard 481-2
  2. The tape complies with all "Notes" for constant dimensions listed on page 5 of EIA-481-2

**Dimensions**  
mm  
(inches)

3.5.3 IX2113G: 14-Pin DIP Through-Hole Package



For additional information please visit our website at: [www.ixysic.com](http://www.ixysic.com)

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Specification: DS-IX2113-R03  
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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