

## INTEGRATED ADSL CMOS ANALOG FRONT-END CIRCUIT

### Features

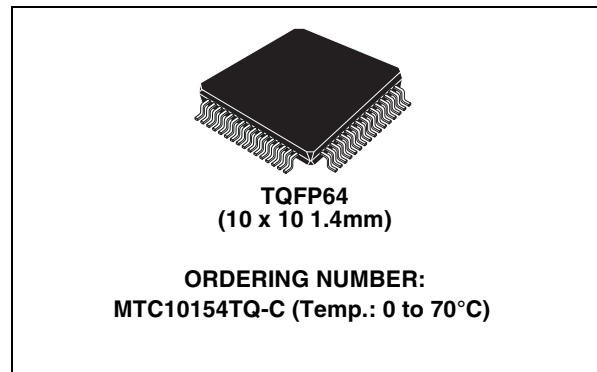
- Fully integrated AFE for ADSL
- Overall 12 bit resolution, 1.1MHz signal bandwidth
- 8.8 MS/s ADC
- 8.8 MS/s DAC
- THD: -60 dB @ full scale
- 1V full scale input
- Differential analog I/O
- Accurate continuous-time channel filtering
- 3<sup>rd</sup> & 4<sup>th</sup> order tunable continuous time LP Filters
- 64 pin TQFP package
- 350mW power consumption

### Applications

- ADSL Front-end for all full rate and Lite standards

### DESCRIPTION

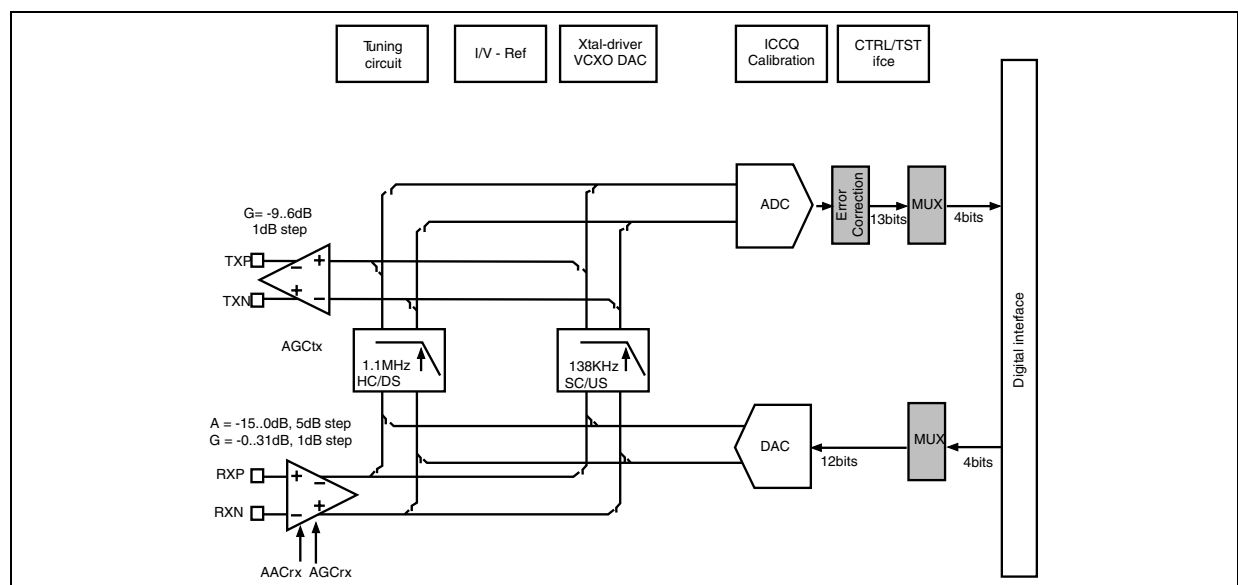
The MTC20154 is the fifth generation Analog Front End (AFE) designed for DMT based ADSL (Asynchronous Digital Subscriber Line) modems compliant with ANSI T1.413 category 2 standard. It includes one 12 bit DAC and one 13 bit ADC. It is



intended to be used with the MTC20156/ MTC20147 DMT/ATM processors as part of the MTK20150/MTK20141 chipsets, but may also be used to support other xDSL signal processors.

The MTC20154 provides programmable low pass filters for each of the two channels and automatic gain control. A configuration pin allows the filters to be switched from ATU-R mode to ATU-C mode. The pipeline ADC architecture provides 13 bit dynamic range and a signal bandwidth of 1.1 MHz. The device consumes only 0.35 Watt in full operation and has a power down mode for standby. It is housed in a compact 64 pin thin plastic quad flat package.

**Figure 1. Block Diagram**



### Functional Description

The MTC20154 chip can be used on the ATU-C side (LT), and on the ATU-R (NT) side (defined by LTNT pin). The selection consists mainly of a filter interchange between the RX and TX path. The filters (with a programmable cutoff frequency) use automatic continuous time tuning to avoid time varying phase characteristics which can be of dramatic consequence for DMT modems. It requires few external components, uses a 3.3 V supply and is packaged in a 64 pins TQFP in order to reduce PCB area.

### The Receiver (RX)

The DMT signal coming from the line to the MTC20154 is first filtered by the two following external filters:

- POTS HP filter: Attenuation of speech and POTS signalling.
- Channel filter: Attenuation of echo signal to improve RX dynamic.

The signal is amplified by a low noise gain stage (-15..+31 dB) then low-pass filtered to avoid anti-aliasing and to ease further digital processing by removing unwanted high frequency out-of-band noise.

A 12 bits A/D converter samples the data at 8.832 MS/s, transforms the signal into a digital representation and sends it to the DMT signal processor via the digital interface.

### The Transmitter (TX/TXE)

The 12 bits data at 8.832 Ms coming from the DMT signal processor through the digital interface are transformed by a D/A converter into an analog signal. This signal is then filtered to decrease DMT sidelobes levels and meet the ANSI transmitter spectral response but also to reduce the out-of-band noise (which can be echoed to the RX path) to an acceptable level. The pre-driver buffers the signal for the external line driver and in case of short loops provide attenuation provision (-9..+6 dB).

### The VCXO

The VCXO is divided in a XTAL driver and an auxilliary 8 bits DAC for timing recovery.

The XTAL driver is able to operate at 35.328 MHz or 17.664 MHz. An internal PLL will be used to double the frequency in the 17.664 MHz case. It also provides an amplitude regulation mechanism to avoid temperature/-supply/technology dependent frequency pulling.

The DAC which is driven by the CTRLIN pin provides a current output with 8 bits resolution and can be used to tune the XTAL frequency with the help of external components. A time constant between DAC input and VCXO output can be introduced (via the CTRLIN interface) and programmed with the help of an external capacitor (on VCOCAP pin).

### The Digital Interface

The digital part of the MTC20154 can be divided into two parts: The data interface converts the multiplexed data from/to the DMT signal processor into a valid representation for the TX DAC and RX ADC. The control interface allows the board processor to configure the MTC20154 paths (RX/TX gains, filter band, ...) or settings.

### Package

The MTC20154 is housed in a 64-pin TQFP package.

## Pin Assignment

Table 1. Pinning Description MTC20154 AFE

| Pin                      | Name    | Description                           | Connection       | Type     | Dir. | Main characteristics                                   |
|--------------------------|---------|---------------------------------------|------------------|----------|------|--------------------------------------------------------|
| <b>Digital interface</b> |         |                                       |                  |          |      |                                                        |
| 64                       | DVSS    | Negative supply for input I/Os + core | Dig supply       | Direct   | Bi   | $Z = 0 \equiv \Omega$                                  |
| 1                        | TX3     | Transmit data bus bit 3 (MSB)         | MTC20156/146/147 | Schmitt  | In   | high Z                                                 |
| 2                        | TX2     | Transmit data bus bit 2               | MTC20156/146/147 | Schmitt  | In   | high Z                                                 |
| 3                        | TX1     | Transmit data bus bit 1               | MTC20156/146/147 | Schmitt  | In   | high Z                                                 |
| 4                        | TX0     | Transmit data bus bit 0 (LSB)         | MTC20156/146/147 | Schmitt  | In   | high Z                                                 |
| 5                        | CTRLIN  | Serial control interface input        | MTC20156/146/147 | Schmitt  | In   | high Z                                                 |
| 6                        | DVDD    | Positive supply for input I/Os + core | Dig supply       | Direct   | Bi   | $Z = 0 \equiv \Omega$                                  |
| 7                        | DVDD    | Positive supply for output I/Os       | Dig supply       | Direct   | Bi   | $Z = 0 \equiv \Omega$                                  |
| 8                        | CLKM    | Master clock output                   | System           | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 9                        | CLKWD   | Word clock output                     | System           | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 10                       | RX3     | Receive data bus bit 3 (MSB)          | MTC20156/146/147 | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 11                       | RX2     | Receive data bus bit 2                | MTC20156/146/147 | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 12                       | RX1     | Receive data bus bit 1                | MTC20156/146/147 | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 13                       | RX0     | Receive data bus bit 0 (LSB)          | MTC20156/146/147 | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 14                       | PD      | General power down                    | System           | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 15                       | DVSS    | Negative supply for output I/Os       | Dig supply       | Direct   | Bi   | $Z = 0 \equiv \Omega$                                  |
| 16                       | RESET   | General reset (active low)            | System           | Schmitt  | In   | High Z                                                 |
| <b>Analog interface</b>  |         |                                       |                  |          |      |                                                        |
| 17                       | AVSSADC | ADC analog negative supply            | Ana supply       | Direct   | Bi   | $Z = 0 \equiv \Omega$                                  |
| 18                       | DRVSD   | External TX driver shutdown           | TX driver        | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 19                       | DRV1    | External TX driver bias control MSB   | TX driver        | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 20                       | DRV0    | External TX driver bias control LSB   | TX driver        | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 22                       | VREF    | ADC virtual ground decoupling         | C network        | Analog   | Bi   | NoDC current                                           |

Table 1. Pinning Description MTC20154 AFE (continued)

| Pin | Name        | Description                             | Connection | Type     | Dir. | Main characteristics                                   |
|-----|-------------|-----------------------------------------|------------|----------|------|--------------------------------------------------------|
| 23  | VRAN        | ADC negative reference decoupling       | C network  | Analog   | Bi   | NoDC current                                           |
| 24  | VRAP        | ADC positive reference decoupling       | C network  | Analog   | Bi   | NoDC current                                           |
| 25  | AVDDADC     | ADC analog positive supply              | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 29  | AVDD TXDRV  | Internal TX pre--driver positive supply | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 30  | TXN         | Analog TX signal negative output (diff) | TX output  | Analog   | Out  | $V_{com} = VDD/2$                                      |
| 31  | TXP         | Analog TX signal positive output (diff) | TX output  | Analog   | Out  | $V_{com} = VDD/2$                                      |
| 32  | AVSS TXDRV  | Internal pre--driver negative supply    | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 33  | GP3         | Analog general purpose control pin      | Board      | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 34  | GP2         | Analog general purpose control pin      | Board      | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 35  | GP1         | Analog general purpose control pin      | Board      | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 36  | GP0         | Analog general purpose control pin      | Board      | Tristate | Out  | $I_{max} = 4 \text{ mA}$<br>$C_{max} = 100 \text{ pF}$ |
| 39  | AVDDFILT    | Filter analog positive supply           | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 40  | AGND        | Analog virtual ground                   | C network  | Analog   | Bi   | NoDC current                                           |
| 43  | AVSSFILT    | Filter analog negative supply           | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 44  | AVSSLNA     | LNA analog negative supply              | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 48  | AVDDLNA     | LNA analog positive supply              | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 50  | RXN         | Analog RX signal negative input (diff)  | RX input   | Analog   | In   | $V_{com}$ forced at $VDD/2$                            |
| 51  | RXP         | Analog RX signal positive input (diff)  | RX input   | Analog   | In   | $V_{com}$ forced at $VDD/2$                            |
| 52  | XTAL bypass | Crystal oscillator bypass selection pin | Strap      | Schmitt  | In   | High Z                                                 |
| 53  | PLL         | PLL enable/disable selection pin        | Strap      | Schmitt  | In   | High Z                                                 |
| 54  | DACVREF     | DAC voltage reference decoupling        | C network  | Analog   | Bi   | NoDC current                                           |
| 55  | AVDDDAC     | DAC analog positive supply              | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 56  | AVDD XTAL   | Crystal driver analog positive supply   | Ana supply | Direct   | Bi   | $Z = 0 \cong \Omega$                                   |
| 57  | XTALO       | Crystal driver connection 1             | Crystal    | Analog   | Bi   | X cap sensitive                                        |
| 58  | XTALI       | Crystal driver connection 2             | Crystal    | Analog   | Bi   | X cap sensitive                                        |

Table 1. Pinning Description MTC20154 AFE (continued)

| Pin                                 | Name      | Description                           | Connection | Type    | Dir. | Main characteristics |
|-------------------------------------|-----------|---------------------------------------|------------|---------|------|----------------------|
| 59                                  | AVSS XTAL | Crystal driver analog negative supply | Ana supply | Direct  | Bi   | $Z = 0 \cong \Omega$ |
| 60                                  | AVSSDAC   | DAC analog negative supply            | Ana supply | Direct  | Bi   | $Z = 0 \cong \Omega$ |
| 61                                  | IVCO      | VCO steering current reference        | VCO        | Analog  | Bi   | DC current           |
| 62                                  | VCOcap    | VCO external capacity connection      | Capacity   | Analog  | Bi   | No Dc current        |
| 63                                  | VCXOI     | VCO steering current output           | VCO        | Analog  | Bi   | DC current           |
| <b>Mode selection interface</b>     |           |                                       |            |         |      |                      |
| 26                                  | LTNT      | Mode selection: LT or NT (static)     | Strap      | Schmitt | In   | high Z               |
| 27                                  | TEST      | Test mode selection (static)          | Strap      | Schmitt | In   | high Z               |
| <b>Analog test access interface</b> |           |                                       |            |         |      |                      |
| 41                                  | T2N       | Neg. diff input/output test access    | Test       | Analog  | Bi   | $V_{com} = VDD/2$    |
| 42                                  | T2P       | Pos. diff. input/output test access   | Test       | Analog  | Bi   | $V_{com} = VDD/2$    |
| 46                                  | T1P       | Pos. diff output test access          | Test       | Analog  | Out  | $V_{com} = VDD/2$    |
| 47                                  | T1N       | Neg. diff output test access          | Test       | Analog  | Out  | $V_{com} = VDD/2$    |

Figure 2. MTC20154 Grounding and Decoupling Networks

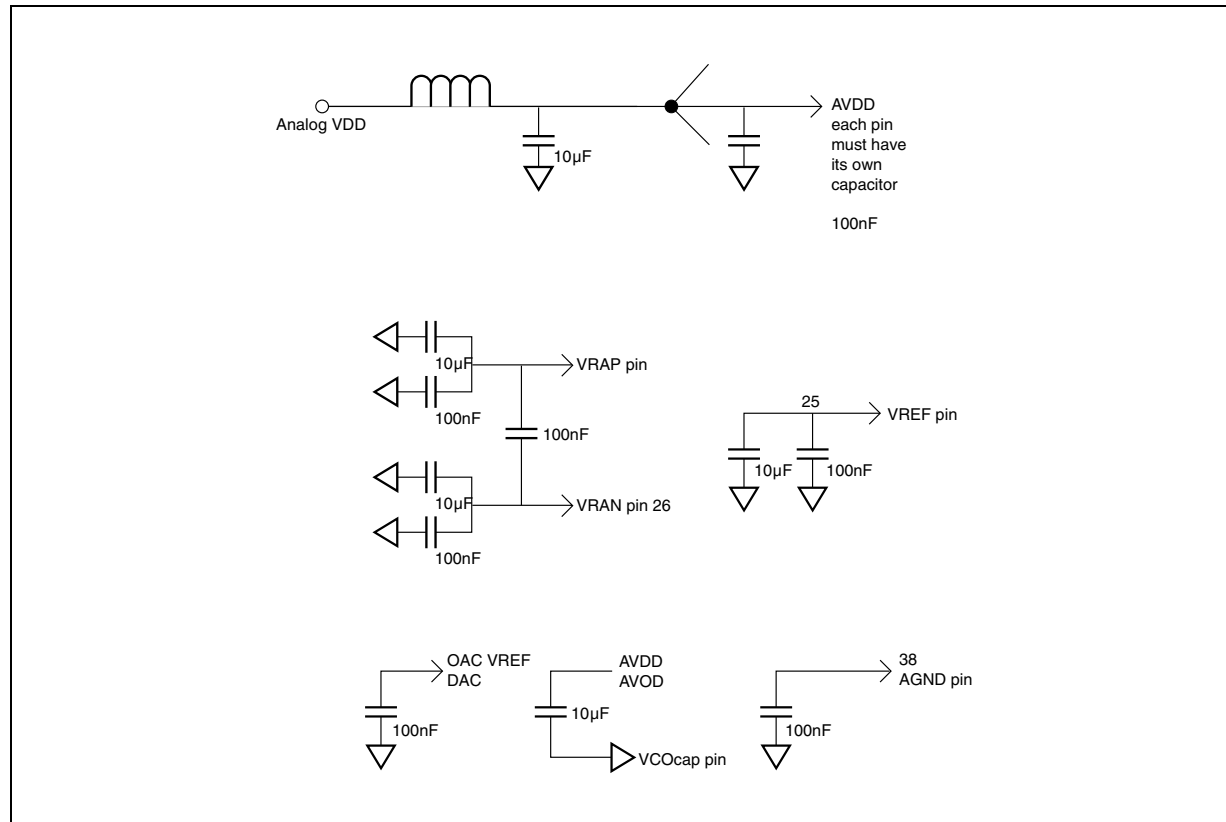
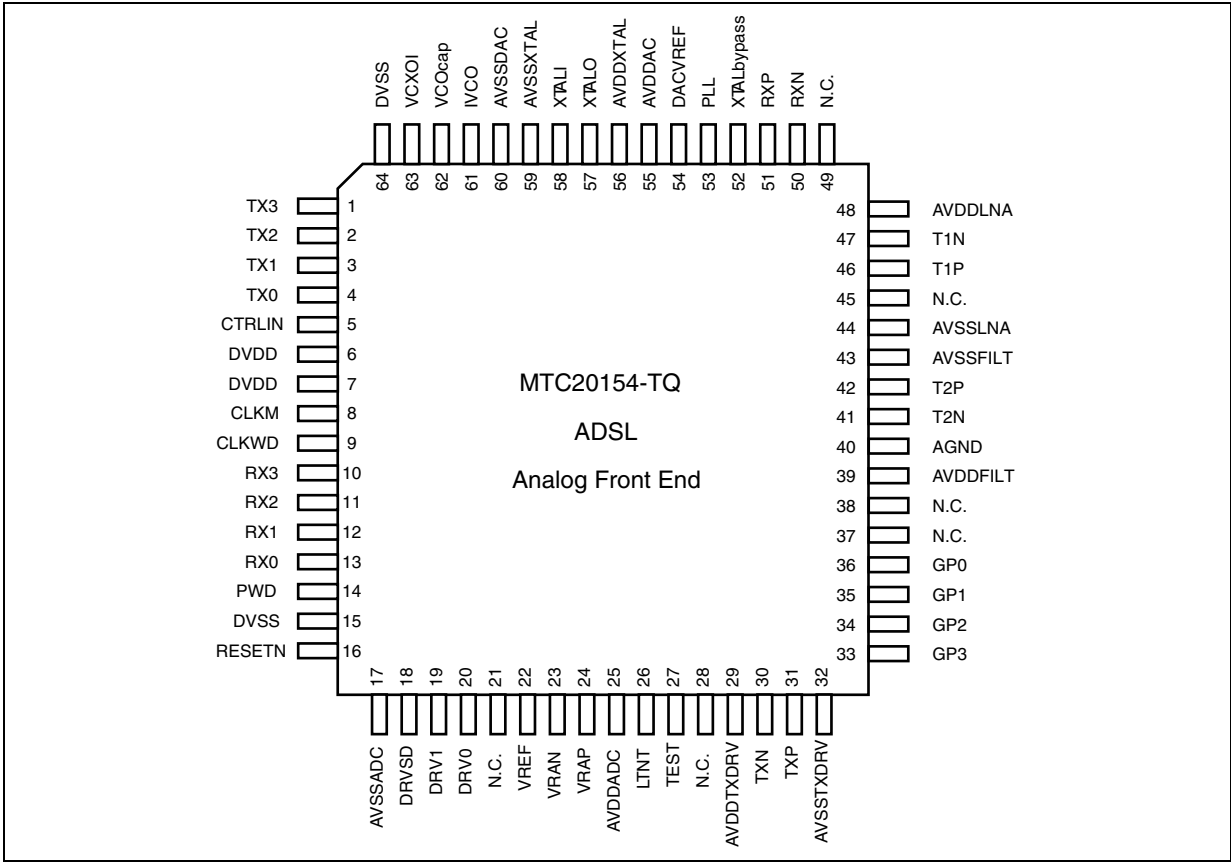


Figure 3. Pin connection (Top view)



## ELECTRICAL RATINGS AND CHARACTERISTICS

### Absolute Maximum Ratings

Operation of the device beyond these limits may cause permanent damage. It is not implied that more than one of these conditions can be applied simultaneously.

Table 2. Electrical Characteristics

| Symbol    | Parameter                                         | Min. | Typ. | Max.           | Unit |
|-----------|---------------------------------------------------|------|------|----------------|------|
| $V_{DD}$  | Any $V_{DD}$ supply voltage, related to substrate | -0,5 |      | 5              | Vhh  |
| $V_{in}$  | Voltage at any input pin                          | -0,5 |      | $V_{DD} + 0.5$ | V    |
| $T_{stg}$ | Storage Temperature                               | -40  |      | 125            | °C   |
| $T_L$     | Lead Temperature (10 second soldering)            |      |      | 300            | °C   |
| $P_d$     | Power Dissipation                                 | 350  | 350  | 500            | mW   |
| $T_j$     | Junction Temperature                              | -40  |      | 110            | °C   |

## Operating Conditions

Unless specified, the characteristic limits of 'Static characteristics' in this document apply for the following operating conditions:

**Table 3. Operating conditions**

| Symbol                             | Parameter                                  | Min. | Max. | Unit |
|------------------------------------|--------------------------------------------|------|------|------|
| AVDD                               | AVDD supply voltages, related to substrate | 3.0  | 3.6  | V    |
| DVDD                               | DVDD supply voltages, related to substrate | 2.7  | 3.6  | V    |
| V <sub>in</sub> , V <sub>out</sub> | Voltage at any input and output pin        | 0    | VDD  | V    |
| T <sub>amb</sub>                   | Ambient Temperature - I version            | -40  | 85   | °C   |
| T <sub>amb</sub>                   | Ambient Temperature - C version            | 0    | 70   | °C   |

## Static Characteristics

### Digital Inputs

Schmitt-trigger inputs: TXi, CTRLIN, PDOWN, LTNT, RESETN, TEST

**Table 4. Digital Inputs**

| Symbol | Parameter                | Min.     | Max.     | Unit |
|--------|--------------------------|----------|----------|------|
| VIL    | Low level input voltage  |          | 0.2*DVDD | V    |
| VIH    | High level input voltage | 0.8*DVDD |          | V    |
| VH     | Hysteresis               | 1.0      | 1.3      | V    |
| Cinp   | Input capacitance        |          | 3        | pF   |

### Digital Outputs

Hard driven outputs: RXi, CLKWD, GPI, DRVI, DRVSD

**Table 5. Digital Outputs**

| Symbol | Parameter                 | Test Condition           | Min.     | Max.     | Unit |
|--------|---------------------------|--------------------------|----------|----------|------|
| VOL    | Low level output voltage  | I <sub>out</sub> = -4 mA |          | .15*DVDD | V    |
| VOH    | High level output voltage | I <sub>out</sub> = 4mA   | .85*DVDD |          | V    |
| Cload  | Load capacitance          |                          |          | 30       | pF   |

Clock Driver output: CLKM

**Table 6. Clock Driver output**

| Symbol | Parameter                 | Test Condition           | Min.     | Max.     | Unit |
|--------|---------------------------|--------------------------|----------|----------|------|
| VOL    | Low level output voltage  | I <sub>out</sub> = -4 mA |          | .15*DVDD | V    |
| VOH    | High level output voltage | I <sub>out</sub> = 4mA   | .85*DVDD |          | V    |
| Cload  | Load capacitance          |                          |          | 30       | pF   |
| Dcycle | Duty cycle                |                          | 45       | 55       | %    |

**Analog TX/RX Signals**

The reference impedance for all power calculations is 100Ω.

**DMT Signal**

A DMT signal is basically the sum of N independently QAM modulated signals, each carried over a distinct carrier. The frequency separation of each carrier is 4.3125 KHz with a total number of 256 carriers (ANSI). For large N, the signal can be modelled by a gaussian process with a certain amplitude probability density function. Since the maximum amplitude is expected to arise very rarely, the signal is clipped to trade-off the resulting SNR loss against AD/DA dynamic range.

A clipping factor ( $V_{peak}/V_{rms}$  = "crest factor") of 5 is used resulting in a maximum SNR of 75 dB. ADSL DMT signals are nominally sent at -40 dBm/Hz +/- 3 dB (-3.65 dBm/carrier) with a maximal power of 100 mW for downlink transmitter and 4.5 mW for uplink transmitter.

The minimum SNR+D needed for DMT carrier demodulation is about  $(3 \cdot N + 20)$  dB with a minimum of 38 dB where N is the constellation size of a carrier (in bits).

**Table 7. Signal Levels (on the line)**

| Description   | LT side    |            | NT side    |            |
|---------------|------------|------------|------------|------------|
|               | RX         | TX         | RX         | TX         |
| Max level     | 839 mVpdif | 15.8 Vpdif | 3.95 Vpdif | 3.4 Vpdif  |
| Max RMS level | 168 Vrms   | 3.16 Vrms  | 791 mVrms  | 671 mVrms  |
| Min level     | 54 mVpdif  | 3.95 Vpdif | 42 mVpdif  | 839 mVpdif |
| Min RMS level | 11 mVrms   | 791 mVrms  | 8 mVrms    | 168 mVrms  |

**Table 8. Total Signal Level (on the line)**

| Description            | LT side             | NT side                |
|------------------------|---------------------|------------------------|
|                        | RX                  | RX                     |
| Max level for receiver | 4 Vpdif (Long line) | 4.2 Vpdif (Short line) |

### ATU-C Side Block Diagram

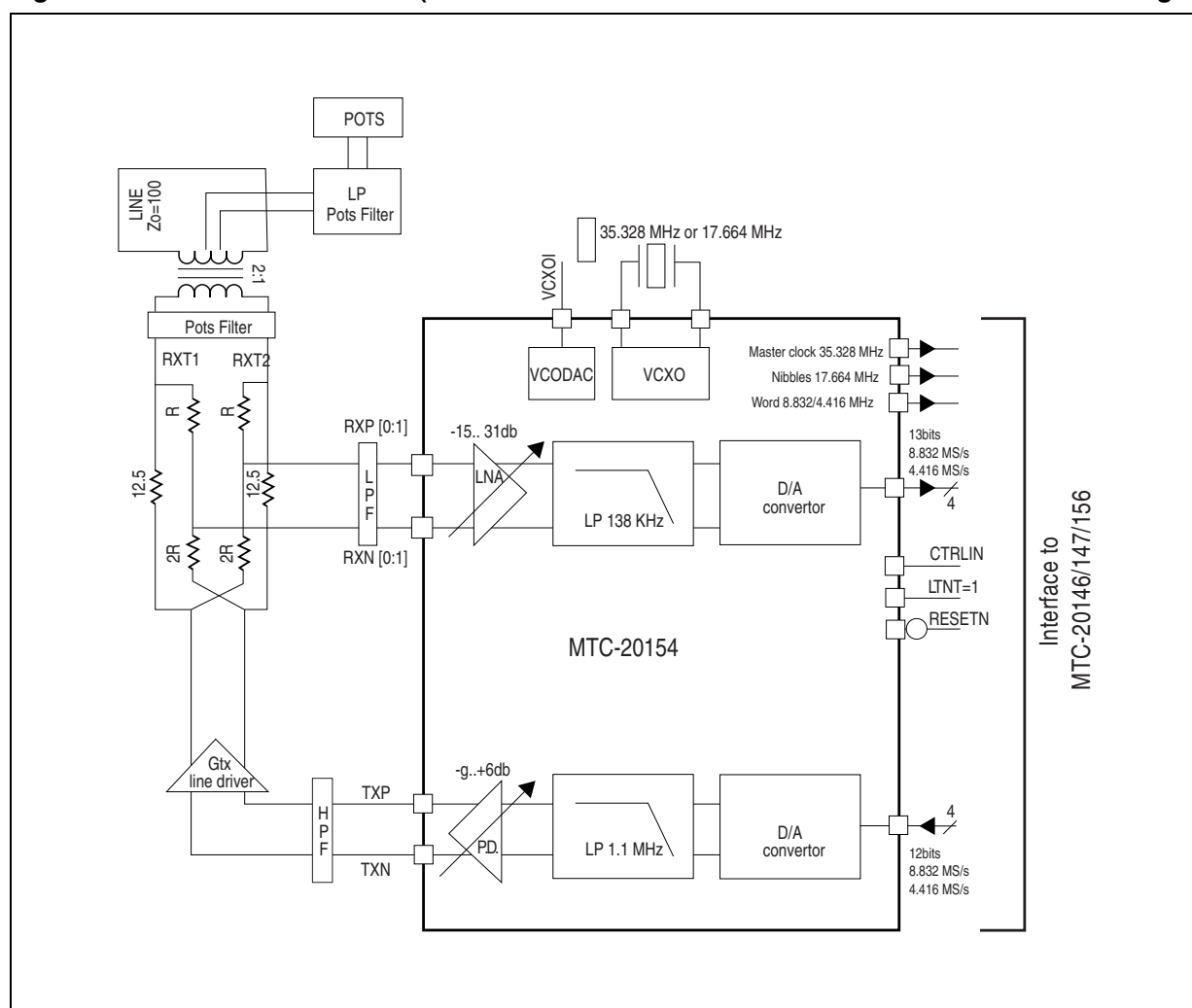
The transformer at the ATU-C side has a 1:2 ratio. The termination resistors are  $12.5\Omega$  in case of  $100\Omega$  lines. The hybrid bridge resistors should be  $< 2.5\text{ k}\Omega$  for low-noise.

An HP filter must be used on the TX path to reduce DMT sidelobes and out-of-band noise influence on the receiver.

On the RX path, a LP filter must be used in order to reduce the echo signal level and to avoid saturation of the input stage of the receiver.

The POTS filter is used in both directions to reduce crosstalk between ADSL signals and POTS speech and signalling.

**Figure 4. ATU-C AFE Schematics (For detailed schematics see MTB-20150-EBC reference design.)**



### ATU-R Side Block Diagram

The ATU-R side block diagram is equal to the ATU-C side block diagram with the following differences:

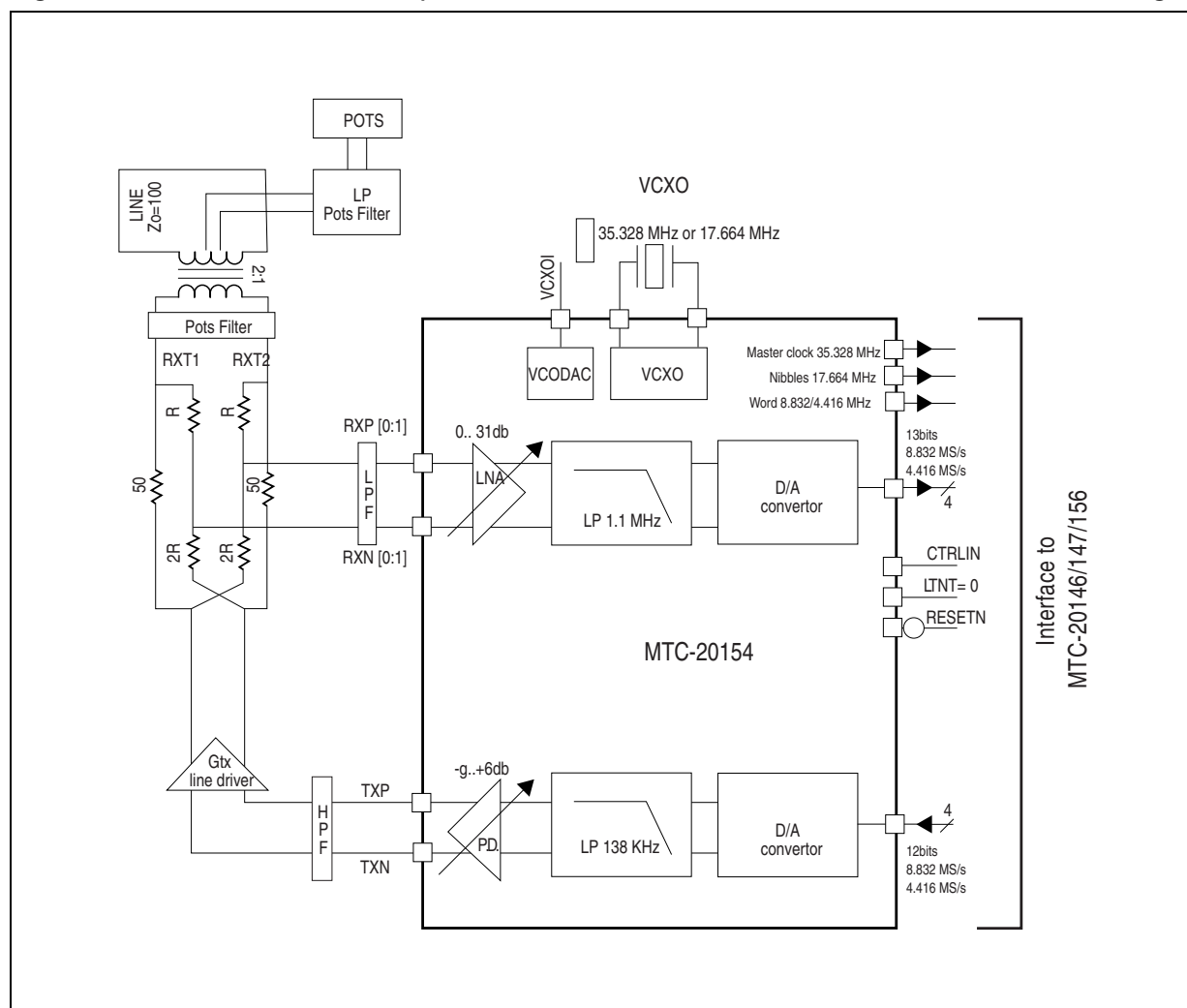
- The transformer ratio is 1:1
- Termination resistors are 50Ω for 100Ω lines.

An LP filter may be used on the TX path to reduce DMT sidelobes and out-of-band noise influence on the receiver.

On the RX path, a HP filter must be used in order to reduce the echo signal level and to avoid saturation of the input stage of the receiver.

The POTS filter is used in both directions to reduce crosstalk between ADSL signals and POTS speech and signalling.

**Figure 5. ATU-R AFE Schematics (For detailed schematics see MTB-20141-EBR reference design.)**



## MTC20154 RX PATH

### Speech Filter

An external bidirectional LP filter for up and downstream POTS service splits out the speech signal to the analog telephone circuit on both the NT and LT sides of the line. The ADSL analog front end integrated circuit does not contain any circuitry for the POTS service but guarantees that the POTS bandwidth is not disturbed by spurious signals from the ADSL spectrum.

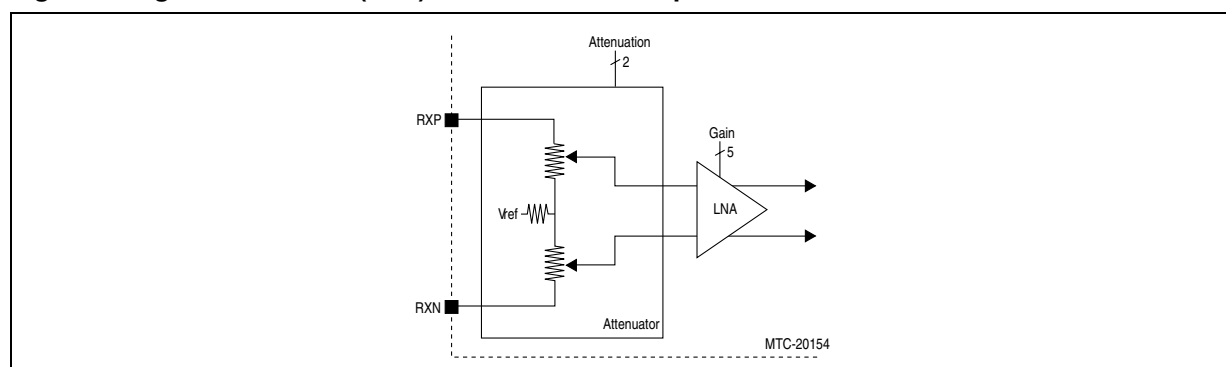
### Channel Filters

The purpose of these external analog circuits is to provide partial echo cancellation by analog filtering of the receive signal for both ATU-R (reception of downstream channel) and ATU-C (reception of upstream channel). This is feasible because the upstream and the downstream data can be modulated on separate carriers (FDM).

### Signal Attenuator (ATT) and Low Noise Amplifier

The attenuator needs to be DC decoupled from the external circuitry. In fact, it is also used to internally fix the LNA input common mode voltage at the nominal value:  $AVDD/2$ . This is done by the use of an internal biasing circuit. It is therefore mandatory to decouple the MTC20154 input from any external DC biasing system. The Low Noise Amplifier (LNA) placed after the ATT will be used in combination with the attenuation block. The goal is to obtain a range of RX path input level varying from  $-15$  dB to  $31$  dB, while maintaining the noise contribution negligible.

**Figure 6. Signal Attenuator (ATT) and Low Noise Amplifier**



The input attenuator will have the following characteristics

**Table 9. Attenuator Characteristics**

| Data                               | Min                         | Typical | Max       | Unity       |
|------------------------------------|-----------------------------|---------|-----------|-------------|
| Input type                         | AC only, DC decoupled       | –       |           |             |
| Common mode voltage (forced)       | –                           | $VDD/2$ | –         | V           |
| Maximum input differential voltage | –                           | VDD     | $VDD+1Vd$ | $V_{pdiff}$ |
| Input impedance                    | 10                          | 14.47   | 19        | KOhms       |
| Attenuation step                   | –                           | 5       | –         | dB          |
| Attenuation range                  | 0                           | –       | $-15$     | dB          |
| Maximum attenuation error          | –                           | .05     | –         | dB          |
| Digital interface                  | –                           | 2       | –         | bits        |
| Digital code                       | '11' → 0 dB attenuation     |         |           |             |
|                                    | '00' → $-15$ dB attenuation |         |           |             |

**Table 10. LNA characteristics**

| Data                                                                            | Min                                | Typical                              | Max | Unity  |
|---------------------------------------------------------------------------------|------------------------------------|--------------------------------------|-----|--------|
| Input common mode voltage                                                       | –                                  | AVDD/2                               | –   | V      |
| Input differential voltage                                                      | –                                  | 1                                    | –   | Vpdiff |
| Maximum peak input differential voltage                                         | –                                  | 1                                    | –   | Vpdiff |
| Output common mode voltage                                                      | –                                  | AVDD/2                               | –   | V      |
| Maximum peak output differential voltage                                        | –                                  | 1                                    | –   | Vpdiff |
| Amplification step                                                              | 0.7                                | 1                                    | 1.3 | dB     |
| Amplification range                                                             | 0                                  | –                                    | +31 | dB     |
| Input referred noise at max gain,<br>min atten. (over a 36 kHz to 1.1 MHz band) | 5.5                                | 6.5                                  | 8   | nV/√Hz |
| Power consumption                                                               | –                                  | 32                                   | –   | mW     |
| Digital interface                                                               | –                                  | 5                                    | –   | bits   |
| Digital code                                                                    | '00000'<br>→ 0 dB<br>amplification | '11111'<br>→ +31 dB<br>amplification |     |        |

**RX Filters**

The combination of the external filter (an LC ladder filter typically) with the integrated lowpass filter provides:

- echo reduction to improve dynamic range
- DMT sidelobe and out of band (anti-aliasing) attenuation.
- Anti alias filter (60 dB rejection @ image freq.)

**ATU-R-RX filters**

The integrated filter characteristics are shown in table 6.

**ATU-C-RX Filter**

This filter is the same as the one used for ATU-R\_TX.

**Linearity of RX**

Linearity of the RX analog path is defined by the IM3 product of two sinusoidal signals with frequencies f1 and f2 and each with 0.5 Vpd amplitude (total 1 Vpd) at the output of the RX-AGC amplifier (i.e: before the ADC) for the case of minimal AGC setting.

**Table 11. Integrated filter characteristics ATU-R-RX**

| Description         | Value/Units           |
|---------------------|-----------------------|
| Type                | 4th order butterworth |
| Cut-off frequency   | 1.104 MHz (f0)        |
| Max. in-band ripple | 0-2 dB                |

**Table 12. Linearity of ATU-R-RX**

|                              |                                                                                  |                                        |                                        |
|------------------------------|----------------------------------------------------------------------------------|----------------------------------------|----------------------------------------|
| f1 (0.5 Vpd)<br>f2 (0.5 Vpd) | 300 kHz<br>200 kHz                                                               | 500 kHz<br>400 kHz                     | 700 kHz<br>600 kHz                     |
| S/IM3<br>(AGC = 0 dB)        | 59.5 dB @ 100 kHz<br>53.5 dB @ 400 kHz<br>43.5 dB @ 700 kHz<br>42.5 dB @ 800 kHz | 59.5 dB @ 300 kHz<br>48.0 dB @ 600 kHz | 48.0 dB @ 500 kHz<br>42.5 dB @ 800 kHz |

**Table 13. Linearity of ATU-C-RX**

|               |                 |
|---------------|-----------------|
| f1 (0,5 Vpd)  | 80 kHz          |
| f2 (0,5 Vpd)  | 70 kHz          |
| S/IM3         | 56.5 dB @60 kHz |
| (AGC = 20 dB) | 56.5 dB @90 kHz |

**A/D Converter**

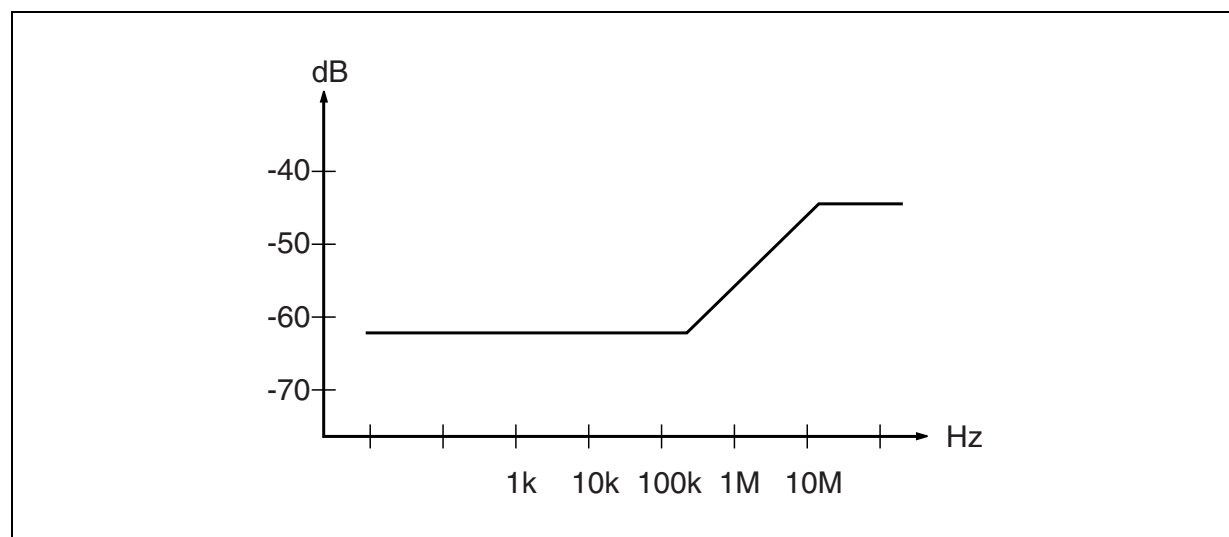
A pipeline architecture is used for the A/D converter.

**Table 14. A/D Converter specifications**

|                                                        |                                 |
|--------------------------------------------------------|---------------------------------|
| Number of bits:                                        | 13 bits                         |
| Minimum resolution of the A/D converter                | 11 bits                         |
| Linearity error of the A/D converter (range: -6 dB FS) | < 4 LSB (out of 13 bits)        |
| Full scale input range:                                | 1.1 Vpdif (+- 5 % @ 3.3 V)      |
| Sampling rate:                                         | 8.832 MHz                       |
| Maximum attenuation at 1.1 MHz:                        | < 0.5 dB without in-band ripple |
| Latency:                                               | 5 sampling clock periods        |

**Power Supply Rejection**

The noise on the power supplies for the RX-path must be lower than the following: < 50 mVrms in-band white noise for any AVDD.

**Figure 7. Power Supply Rejection**

### TX Pre-driver Capability

The pre-driver drives an external line power amplifier which transmits the required power to the line.

**Table 15. Pre-driver characteristics**

|                                                                |                               |                     |
|----------------------------------------------------------------|-------------------------------|---------------------|
| TX drive level to the external line driver for max AGC setting |                               | 2 V <sub>pdif</sub> |
| External line driver input impedance:                          | resistive                     | > 200 $\Omega$      |
|                                                                | capacitive                    | < 30 pF             |
| Pre-driver characteristics:                                    |                               |                     |
| gain range:                                                    | -9 dB...6 dB with step = 1 dB |                     |
| common mode voltage:                                           | AV <sub>DB</sub> /2           |                     |
| output common mode voltage:                                    | 30 nV/Hz                      |                     |

### TX Filter

The TX filters act not only to suppress the DMT sidebands but also as smoothing filters on the D/A converter's output to suppress the image spectrum. For this reason they are realised in a time continuous approach.

### ATU-R-TX Filter

The purpose of this filter is to remove out-of-band noise of the ATU-R-TX path echoed to the ATU-R-RX path. In order to meet the transmitter spectral response, additional filtering is (digitally) performed. The integrated filter has nominal characteristics shown in table 11:

**Table 16. ATU-R-TX filter characteristics**

| Description          | Value/Units               |
|----------------------|---------------------------|
| Input referred noise | 94 nV/ $\sqrt{\text{Hz}}$ |
| Max. input level     | 1 V <sub>pd</sub>         |
| Max. output level    | 1 V <sub>pd</sub>         |
| Type                 | 4th order chebychef       |
| Cut-off frequency    | 138 KHz (f <sub>0</sub> ) |
| Max. in-band ripple  | 0.5 dB                    |

### ATU-C-TX Filter

Same filter as ATU-R-RX. Its purpose is now is to remove image frequency of the transmitted signal according the ANSI definition.

**Table 17. D/A Converter**

| Description                             | Value/Units                              |
|-----------------------------------------|------------------------------------------|
| Number of bits:                         | 12 bits                                  |
| Minimum resolution of the D/A converter | 11 bits                                  |
| Linearity error of the D/A converter    | < 1 LSB (out of 12 bits)                 |
| Full scale output range:                | 1 V <sub>pdif</sub> +- 5%                |
| Sampling Rate:                          | 8.832 MHz (or 4.416 in alternative mode) |
| Latency:                                | 1 sampling clock period                  |

### Linearity of ATU-C-TX

Linearity of the TX is defined by the IM3 product of two sinusoidal signals with frequencies  $f_1$  and  $f_2$  and each with 0.25 V<sub>pd</sub> amplitude (-6 dB FS) at the output of the pre-driver for the case of a total AGC = 0 dB.

**Table 18. Linearity of ATU-C-TX**

| f1 (0.25 V <sub>pd</sub> )<br>f2 (0.25 V <sub>pd</sub> ) | 300 kHz<br>200 kHz                                                               | 500 kHz<br>400 kHz                     | 700 kHz<br>600 kHz                     |
|----------------------------------------------------------|----------------------------------------------------------------------------------|----------------------------------------|----------------------------------------|
| S/IM3<br>(AGC = 0 dB)                                    | 59.5 dB @ 100 kHz<br>53.5 dB @ 400 kHz<br>43.5 dB @ 700 kHz<br>42.5 dB @ 800 kHz | 59.5 dB @ 300 kHz<br>45.0 dB @ 600 kHz | 48.0 dB @ 500 kHz<br>42.5 dB @ 800 kHz |

**Table 19. Linearity of ATU-R-TX**

|                            |                     |
|----------------------------|---------------------|
| f1 (0.25 V <sub>pd</sub> ) | 80 k                |
| f2 (0.25 V <sub>pd</sub> ) | 70 k                |
| S/IM3 (AGC = 0 dB)         | 59.5 dB (60 k/90 k) |

### Power Supply Rejection

The noise on the power supplies for the TX-path must be lower than the following: < 50 mV<sub>rms</sub> in band white noise for AVDD.

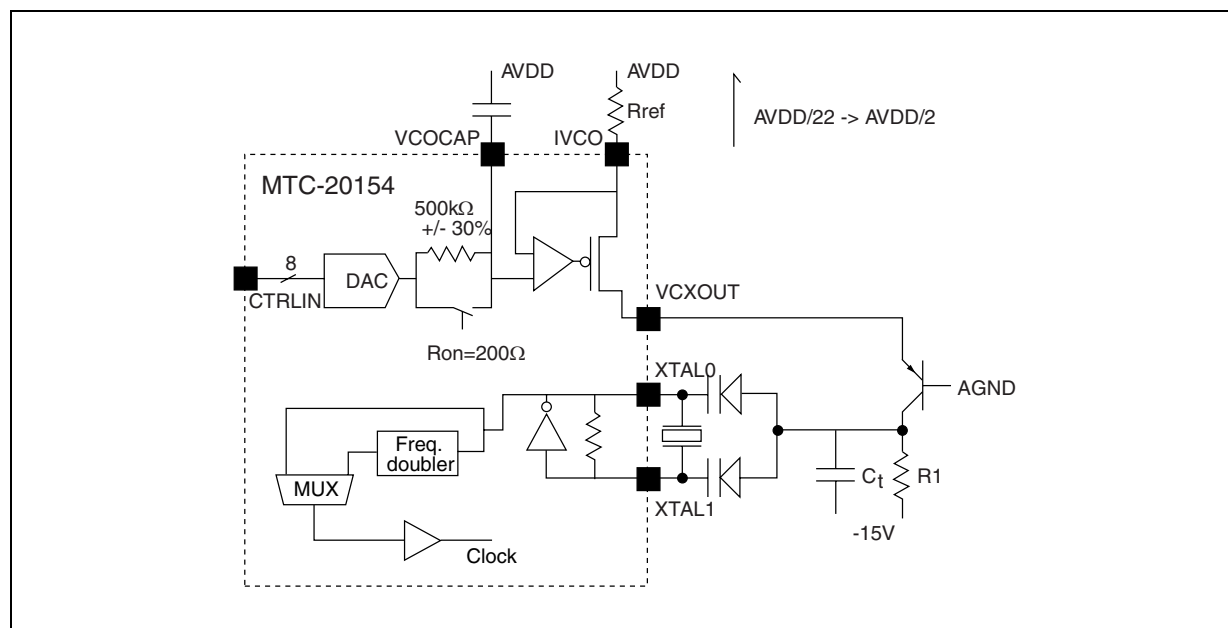
< 15 mV<sub>rms</sub> in band white noise for Pre-driver AVDD.

### Voltage Controlled Crystal Oscillator

A voltage controlled crystal oscillator driver is integrated in the MTC20154. Two nominal frequencies can be used: 35.328 MHz or 17.664 MHz. The quartz crystal is connected between the pins XTAL1 and XTAL0.

The principle of the VCXO control is depicted on the figure beside.

**Figure 8. Principle of the VCXO control (ATU-R)**



The crystal's exact oscillation frequency can be tuned around the nominal frequency. This is needed in order to allow the system to minimize the clock phase shift between the LT and the NT modems. The information coming from the digital processor via the CTRLIN path is used to drive a 8 bits DAC (resistor ladder architecture) which generates a control current. This current is externally converted and filtered to generate the required control voltage for the varicap. The VCXO characteristics are given in the following table.

**Table 20. VCXO characteristics**

| Data                                                        | Min | Typical | Max | Unity |
|-------------------------------------------------------------|-----|---------|-----|-------|
| Needed crystal accuracy                                     | 50  | –       | –   | ppm   |
| Needed crystal frequency tuning range                       | 100 | –       | –   | ppm   |
| DAC resolution                                              | -   | 8       | -   | bit   |
| DAC output voltage range                                    | –   | AVDD/2  | –   | V     |
| DAC differential non linearity error                        | –   | –       | 1.5 | LSB   |
| DAC integrated non linearity error                          | –   | –       | 4   | LSB   |
| VCXO nominal output current<br>(Rref = 16.5 K AVDD = 3.3 V) | 95  | 100     | 105 | mA    |
| Power consumption                                           | –   | .225    | –   | mW    |

### PLL Based Frequency Doubler

Dual crystal frequency can now be used needed when a 17.644 MHz crystal with the MTC20154 on-board crystal is used. A frequency doubler, build driver. However, a master clock up around a Phase Locked Loop (PLL), frequency of 35.328 MHz is still will then be used.

## Digital Interface

### Control Interface

The digital code setting for the MTC20154 configuration is sent over a serial line (CTRLIN) using the word clock (CLKWD). The data burst is composed of 16 bits from which the first bit is used as start bit ('0'), the three LSBs being used to identify the data contained in the 12 remaining bits. Test related data are latched but they are overruled by the normal settings if the TEST pin is low.

### Control Interface Timing

The control interface bits are considered valid on each positive edge of the master clock (CLKM). They will be sampled at this moment. The stop bit will trigger the internal data validation. The timing requirements are depicted in the following figure and table:

**Figure 9. Control Interface Timing diagram**

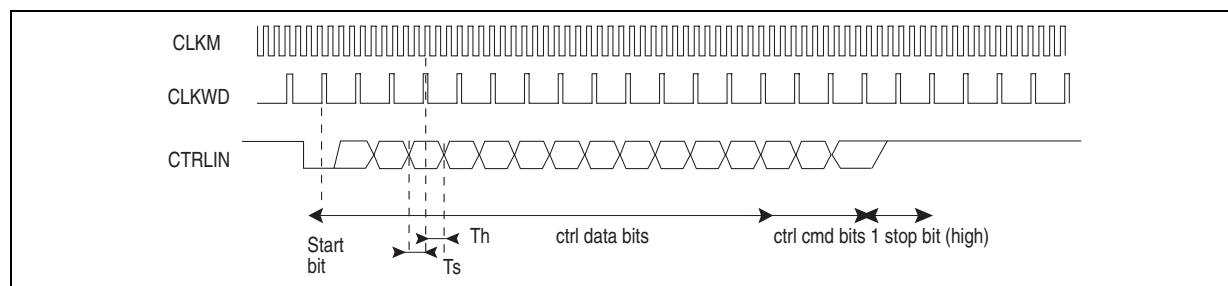


**Table 21. Receive / Transmit Protocol**

| Symbol | Parameters | min    | typ | max  | Remarks |
|--------|------------|--------|-----|------|---------|
| Ts     | Setup Time | 7 ns   | –   | –    |         |
| Th     | Hold time  | 0.2 ns | –   | –    |         |
| TDv    | Data Valid | 0.5 ns | –   | 4 ns |         |

Data set up and hold time are specified versus rising edge of CLKM

### Receive / Transmit Interface

The digital interface is based on a 4 \* 8.832 MHz (35.328 MHz) clock. The 8.832MHz 12 bits A/D output signal or the D/A input signal are SIPO multiplexed over 4 parallel 35.328 MHz data lines in the following table.

If OSR = 2 bit is selected, CLKNIB is used as nibble clock (17.664 MHz, disabled in normal mode), and all the RXi, TXi, CLKWD periods are twice as long as in normal mode.

**Table 22. Receive / Transmit Protocol**

|                          | N0 | N1 | N2  | N3  |
|--------------------------|----|----|-----|-----|
| RXD0 / TXD0 will contain | b0 | b4 | b8  | b12 |
| RXD1 / TXD1 will contain | b1 | b5 | b9  | b13 |
| RXD2 / TXD2 will contain | b2 | b6 | b10 | b14 |
| RXD3 / TXD3 will contain | b3 | b7 | b11 | b15 |

### TX / TXE Signal Dynamic Range

The dynamic range of the signal for both DACs is 12 bits extracted from the available signed 16 bit representation coming from the digital processor. The maximal positive number is  $2^{14}-1$ , the most negative number is  $-2^{14}$ , the 3 LSBs are ignored. Any signal exceeding these limits is clamped to the maximal value.

**Figure 10. TX/TXE Bit Map**

|      |      |     |    |    |    |    |    |    |    |    |    |    |      |      |      |
|------|------|-----|----|----|----|----|----|----|----|----|----|----|------|------|------|
| sign | sign | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | n.u. | n.u. | n.u. |
|------|------|-----|----|----|----|----|----|----|----|----|----|----|------|------|------|

### RX Signal Dynamic Range

The dynamic range of the signal from the ADC is limited to 13 bits. Those bits are converted to a signed representation with a maximal positive number of  $2^{14}-1$  and a most negative number of  $2^{14}$ . The 2 LSBs are filled with '0'.

**Figure 11. RX Bit Map**

|      |     |     |     |    |    |    |    |    |    |    |    |    |    |   |   |
|------|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---|---|
| sign | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | 0 | 0 |
|------|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---|---|

### Receive / Transmit Interface Timing

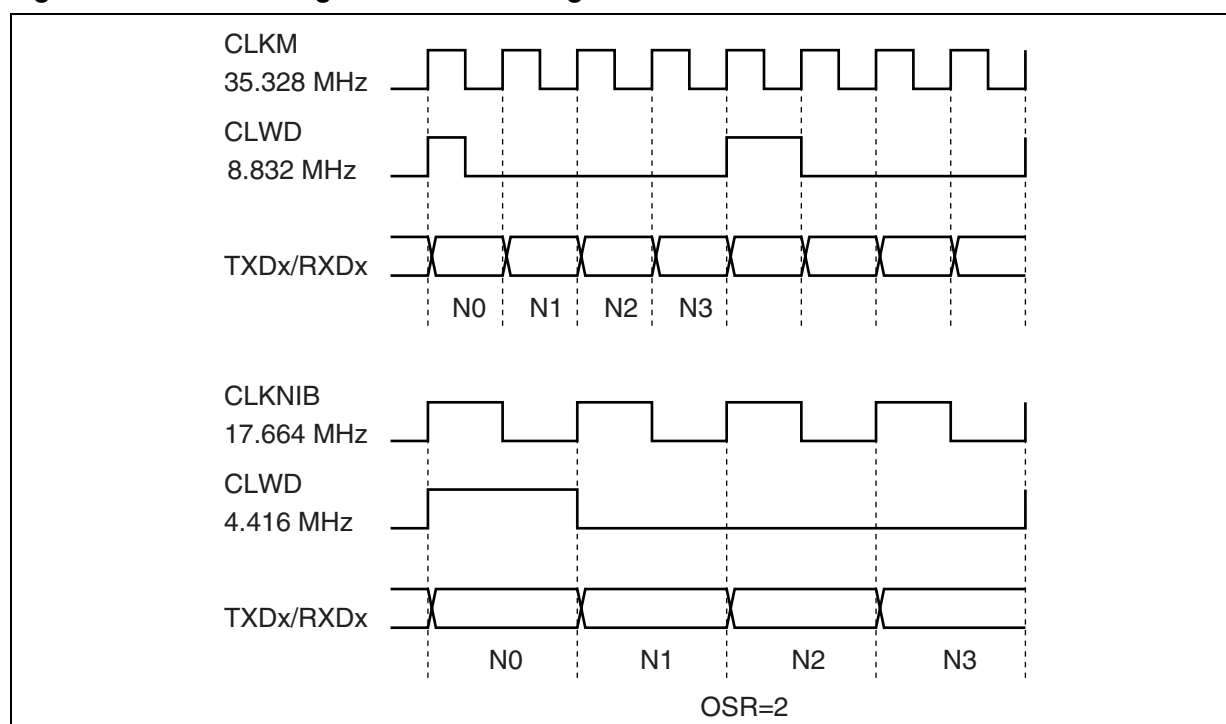
This interface is a triple (RX, TX, TXE) nibble-serial interface running at 8.8 MHz sampling (normal mode). The data are represented in 16 bits format, and transferred in groups of 4 bits (nibbles). The LSBs are transferred first. The MTC20154 generates a nibble clock (= master clock in normal mode, CLKNIB in OSR = 2 mode) and word signals shared by the three interfaces.

Data is transmitted on the rising edge of the master clock (CLKM/CLKNIB) and sampled on the low going edge of CLKM/CLKNIB. This holds for the data stream from MTC20154 and from the digital processor.

Data, CLWD setup and hold times are 5 ns with reference to the falling edge of CLKM/CLKNIB.

RXD is sampled with CLKM rising edge.

**Figure 12. TX/TXE/RX Digital Interface Timing**



### Power Down

The MTC20154 is placed in power-down mode when the PD pin is high. The system specifications are requiring different behavior of the MTC20154 under power down mode according to the fact that the MTC20154 is used at the LT or the NT side. The chip status is depicted in the following table:

**Table 23. Power Down**

| Power down LT side                                                                                                                                                                                                            | Power down NT side                                                                                                                                                                                            |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLKM pin is replicating the XTALO input clock (no crystal used at LT side). System clock available<br>CLKWD is generated.<br>Digital blocks active<br>Analog TX path is in powerdown<br>External driver is forced to power UP | Crystal driver + VCODAC are active<br>CLKWD is generated.<br>Digital blocks active, except for RX-I/O's – they are at low level<br>Analog RX & TX are in powerdown<br>External driver is forced to power DOWN |

## Reset Function

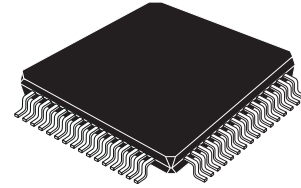
The MTC20154 is placed in reset mode when the RESETN pin is pulled to ground (active low signal). The system specifications are requiring different behavior of the MTC20154 under reset mode according to the fact that the MTC20154 is used at the LT or the NT side. The chip status is depicted in the following table:

**Table 24. Reset Function** (N.B. The reset signal is dominant over the powerdown signal.)

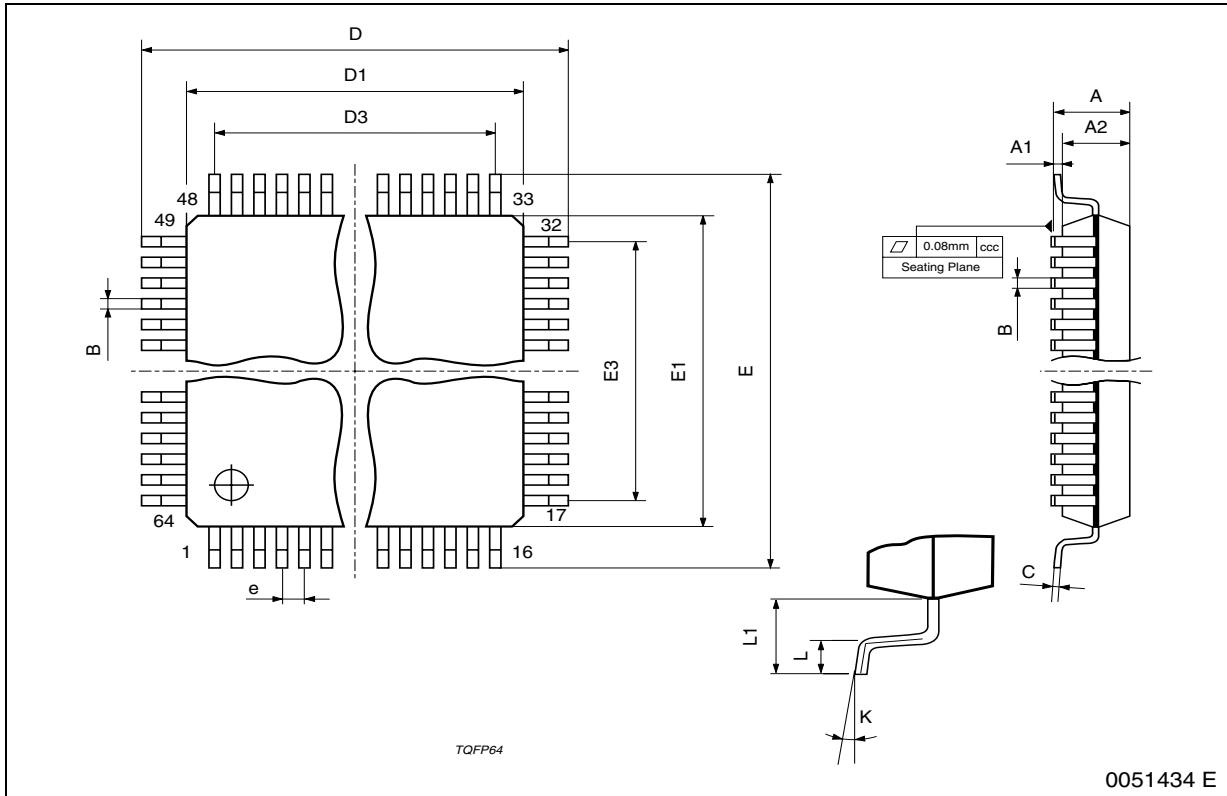
|                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reset LT side<br>CLKM pin is replicating the XTALO input clock<br>(no crystal used at LT side). System clock available<br>CLKWD is not generated. The pin stays at high level.<br>Digital blocks are in reset: no activity<br>Analog blocks are in powerdown<br>External driver is forced to powerdown | Reset NT side<br>Crystal driver in power down: no CLKM signal available.<br>No system clock avail-able.<br>CLKWD is not generated. The pin stays at high level<br>Digital blocks are in reset: no activity<br>Analog blocks are in powerdown<br>External driver is forced to powerdown |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

| DIM. | mm                                |       |       | inch   |        |        |
|------|-----------------------------------|-------|-------|--------|--------|--------|
|      | MIN.                              | TYP.  | MAX.  | MIN.   | TYP.   | MAX.   |
| A    |                                   |       | 1.60  |        |        | 0.063  |
| A1   | 0.05                              |       | 0.15  | 0.002  |        | 0.006  |
| A2   | 1.35                              | 1.40  | 1.45  | 0.053  | 0.055  | 0.057  |
| B    | 0.17                              | 0.22  | 0.27  | 0.0066 | 0.0086 | 0.0086 |
| C    | 0.09                              |       |       | 0.0035 |        |        |
| D    | 11.80                             | 12.00 | 12.20 | 0.464  | 0.472  | 0.480  |
| D1   | 9.80                              | 10.00 | 10.20 | 0.386  | 0.394  | 0.401  |
| D3   |                                   | 7.50  |       |        | 0.295  |        |
| e    |                                   | 0.50  |       |        | 0.0197 |        |
| E    | 11.80                             | 12.00 | 12.20 | 0.464  | 0.472  | 0.480  |
| E1   | 9.80                              | 10.00 | 10.20 | 0.386  | 0.394  | 0.401  |
| E3   |                                   | 7.50  |       |        | 0.295  |        |
| L    | 0.45                              | 0.60  | 0.75  | 0.0177 | 0.0236 | 0.0295 |
| L1   |                                   | 1.00  |       |        | 0.0393 |        |
| K    | 0° (min.), 3.5° (min.), 7° (max.) |       |       |        |        |        |
| ccc  |                                   |       | 0.080 |        |        | 0.0031 |

**OUTLINE AND  
MECHANICAL DATA**



**TQFP64 (10 x 10 x 1.4mm)**



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