DATA SHEET

SKY13299-321LF: 20 MHz-5 GHz, 7 W SPDT Switch

Applications

- WiMAX and WLAN systems

Features

- Positive voltage operation: 0/3 to 0/5 V
- Low insertion loss: 0.5 dB typical @ 3.5 GHz
- High isolation >35 dB @ 3.5 GHz
- High P0.1dB of +38.5 dBm @ 3.3 V
- Low gate lag process for fast settling time applications
- Small, QFN (12-pin, 3 x 3 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

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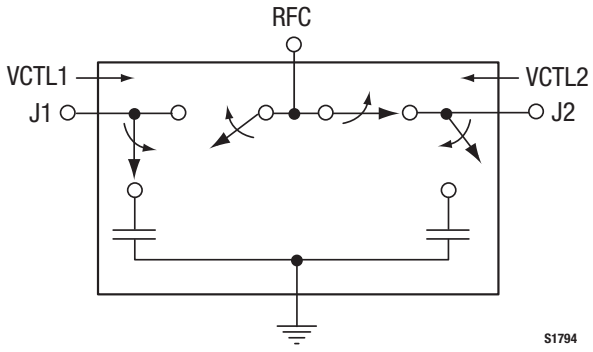


Figure 1. SKY13299-321LF Block Diagram

Description

The SKY13299-321LF is a high-power GaAs pHEMT FET I/C Single-Pole, Double-Throw (SPDT) switch. The device is provided in a 3 x 3 mm, 12-pin Quad Flat No-Lead (QFN) package.

The SKY13299-321LF is particularly suited for low-cost commercial WiMAX and WLAN applications where low insertion loss, high isolation, and excellent linearity are required.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

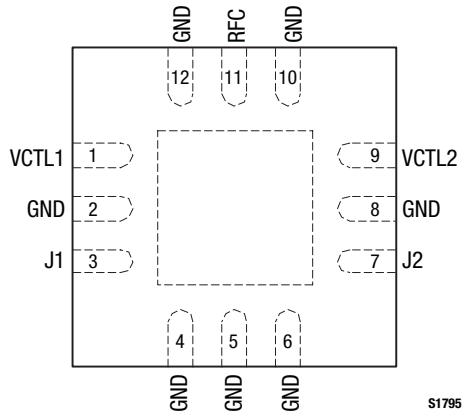


Figure 2. SKY13299-321LF Pinout – 12-Pin QFN (Top View)

Table 1. SKY13299-321LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	VCTL1	DC control voltage.	7	J2	RF port. Must be DC blocked.
2	GND	Ground	8	GND	Ground
3	J1	RF port. Must be DC blocked.	9	VCTL2	DC control voltage.
4	GND	Ground	10	GND	Ground
5	GND	Ground	11	RFC	RF common port. Must be DC blocked.
6	GND	Ground	12	GND	Ground

Note: Exposed pad must be grounded.

Table 2. SKY13299-321LF Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Control voltage range	V_{CTL}	2.75	7	V
RF input power @ 3.3 V, @ 25 °C (f > 700 MHz) (Note 2)	P_{IN}		+39.5	dBm
RF input power @ 5.0 V, @ 25 °C (f > 700 MHz) (Note 2)	P_{IN}		+40.0	dBm
Operating temperature	T_{OP}	–40	+85	°C
Storage temperature	T_{STG}	–65	+150	°C

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Note 2: Input power under matched conditions (50 Ω). Defined as peak or CW. For high Peak-to-Average Ratio (PAR) signals, the highest peak should be below the maximum value shown here.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13299-321LF are provided in Table 2. Electrical specifications are provided in Table 3.

The state of the SKY13299-321LF is determined by the logic provided in Table 4.

Typical performance characteristics are illustrated in Figures 3 to 8.

Table 3. SKY13299-321LF Electrical Specifications (Note 1)
(V_{CTL} = 0 to 3 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, , Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Insertion loss	IL	0.02 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz 4.0 to 5.0 GHz		0.30 0.40 0.45 0.65 0.75	0.50 0.60 0.65 0.85 1.00	dB dB dB dB dB
Isolation	Iso	0.02 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz 4.0 to 5.0 GHz	26 26 26 27 19	29 29 29 30 22		dB dB dB dB dB
Return loss (insertion loss state) (Note 2)		0.02 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz 4.0 to 5.0 GHz		20 17 20 17 17		dB dB dB dB dB
Switching characteristics: Rise/fall time On/off time		 10/90% or 90/10% RF 50% V_{CTL} to 90/10% RF		 200 300		 ns ns
Settling time		50% V_{CTL} to 0.1 dB final value		2		µs
Harmonics	H2, H3	P_{IN} = +34 dBm, CW, @ 900 MHz P_{IN} = +31 dBm, CW, @ 5000 MHz		–80 –78		dBc dBc
0.1 dB Input Compression Point	IP0.1dB	0.7 to 4.0 GHz 48 MHz		+38.5 +38.5		dBm dBm
3rd Order Input Intercept Point	IIP3	V_{CTL} = 3 V For two-tone input power, +27 dBm/tone, 900 and 901 MHz For two-tone input power, +27 dBm/tone, 2400 and 2401 MHz For two-tone input power, +27 dBm/tone, 3500 and 3501 MHz For two-tone input power, +27 dBm/tone, 5000 and 5001 MHz		 +65 +66 +61 +57		 dBm dBm dBm dBm
Control voltage	V_{DD}	V_{CTL} = low V_{CTL} = high	0 2.75		0.2 5.00	V V
Supply current	I_{DD}	V_{CTL} = low V_{CTL} = high @ 3.3 V and <+30 dBm input V_{CTL} = high @ 3.3 V and +30 to +37 dBm input V_{CTL} = high @ 3.3 V and +37 to +38 dBm input		5 50 100 200		µA µA µA µA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Lower frequency return loss is dependent on DC blocks.

Table 4. SKY13299-321LF Truth Table

VCTL1	VCTL2	RFC to J1	RFC to J2
1	0	Insertion loss	Isolation
0	1	Isolation	Insertion loss

Note: 1 = +2.75 to +5.00 V
low = 0 to 0.2 V
Any state other than described in this Table places the switch into an undefined state.

Typical Performance Characteristics

(V_{CTL} = 0 to 3 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_O] = 50 Ω, , Unless Otherwise Noted)

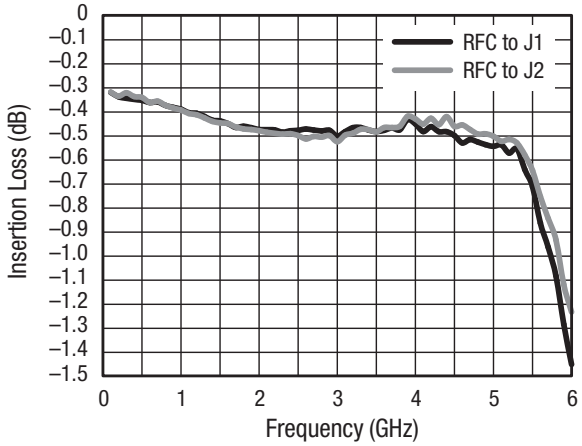


Figure 3. Typical Insertion Loss

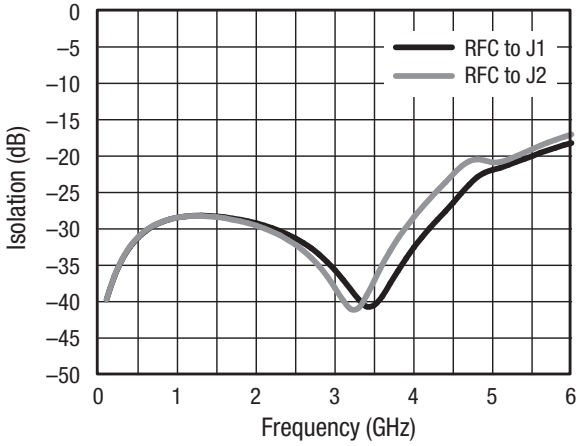


Figure 4. Typical Isolation

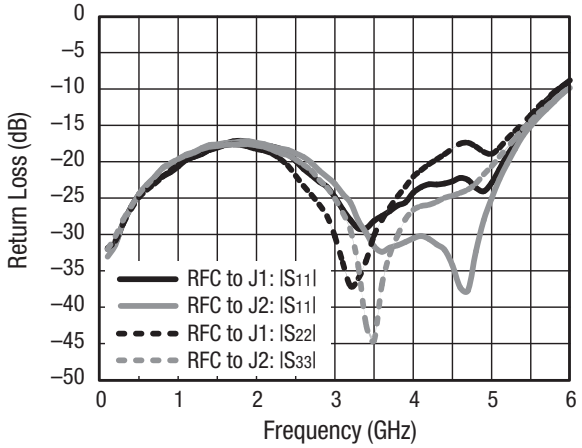


Figure 5. Typical Return Loss

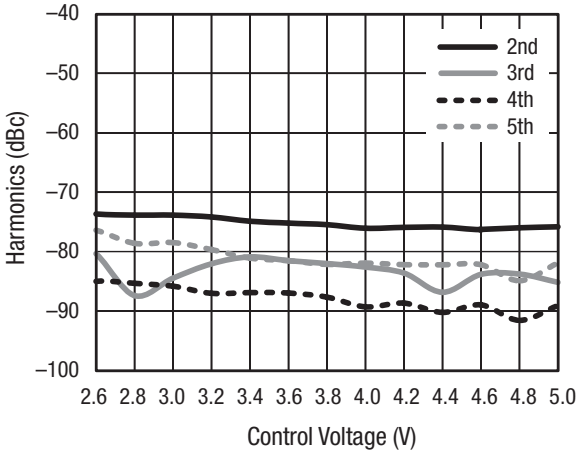


Figure 6. Typical Harmonics
(f = 900 MHz, P_{IN} = +34 dBm, CW)

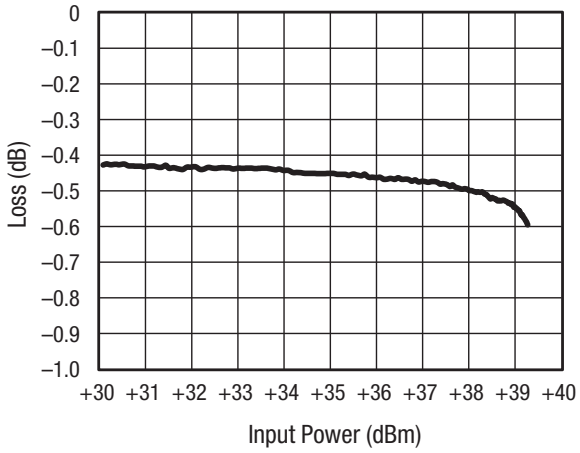


Figure 7. Typical Loss vs Input Power (f = 2500 MHz, V_{CTL} = 3.3 V)

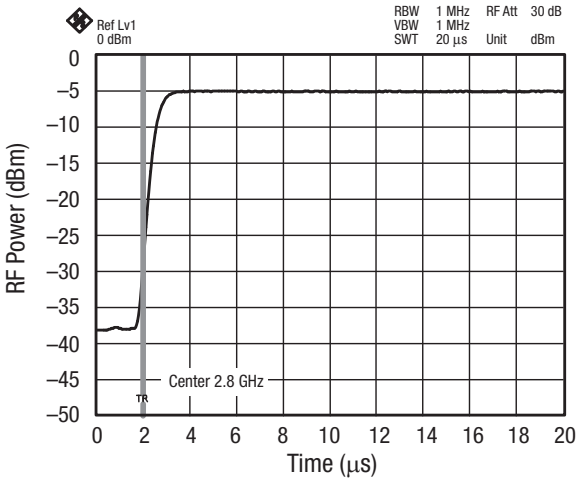


Figure 8. Typical Settling Time

Evaluation Board Description

The SKY13299-321LF Evaluation Board is used to test the performance of the SKY13299-321LF SPDT switch. An assembly drawing for the Evaluation Board is shown in Figure 9 and an Evaluation Board schematic diagram is shown in Figure 10.

Package Dimensions

The PCB layout footprint for the SKY13299-321LF is shown in Figure 11. Typical case markings are noted in Figure 12. Package dimensions for the 12-pin QFN are shown in Figure 13, and tape and reel dimensions are provided in Figure 14.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY13299-321LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

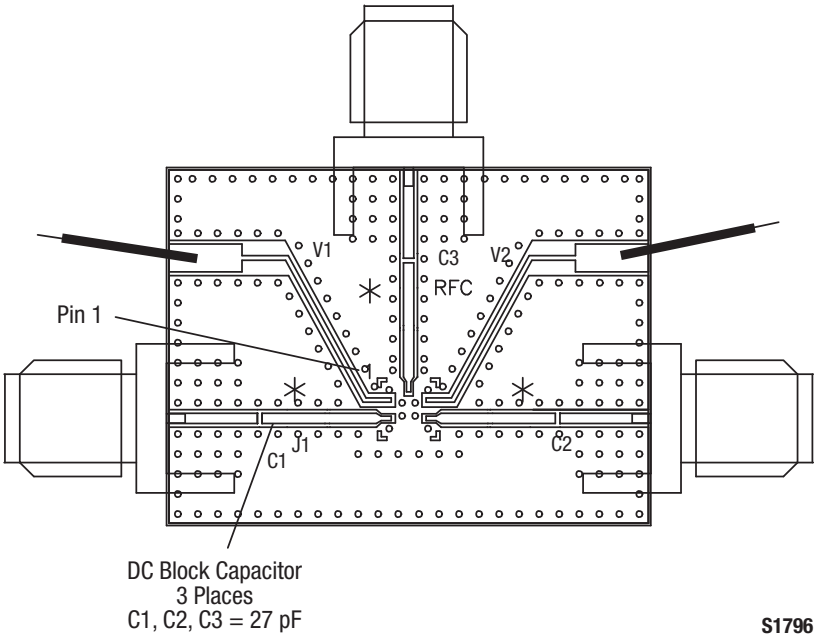


Figure 9. SKY13299-321LF Evaluation Board Assembly Diagram

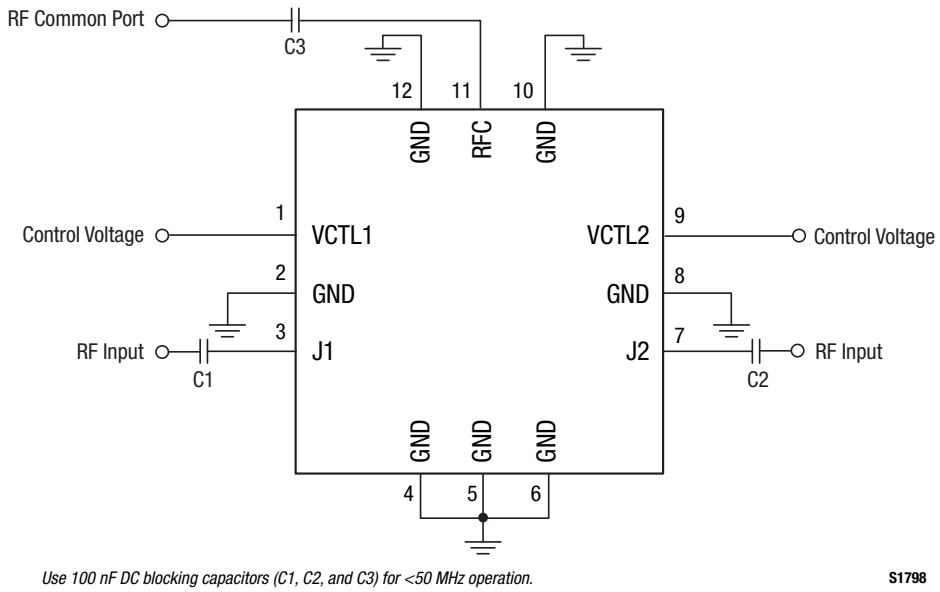


Figure 10. SKY13299-321LF Evaluation Board Schematic Diagram

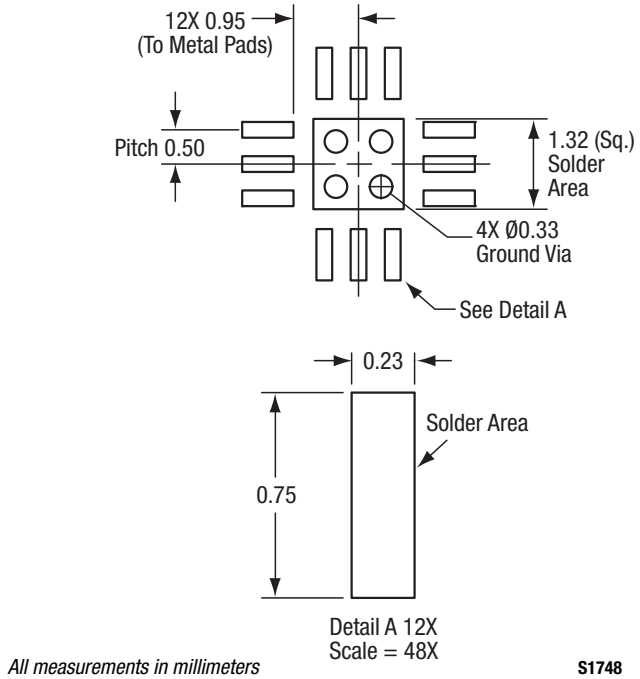


Figure 11. SKY13299-321LF PCB Layout Footprint

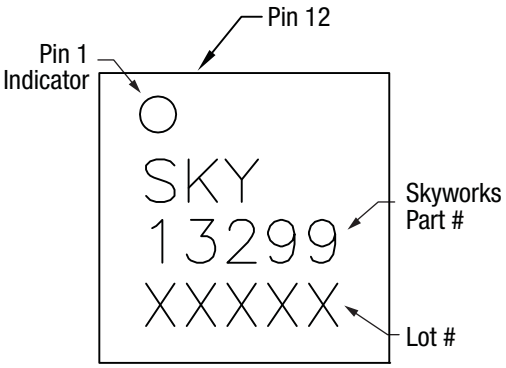
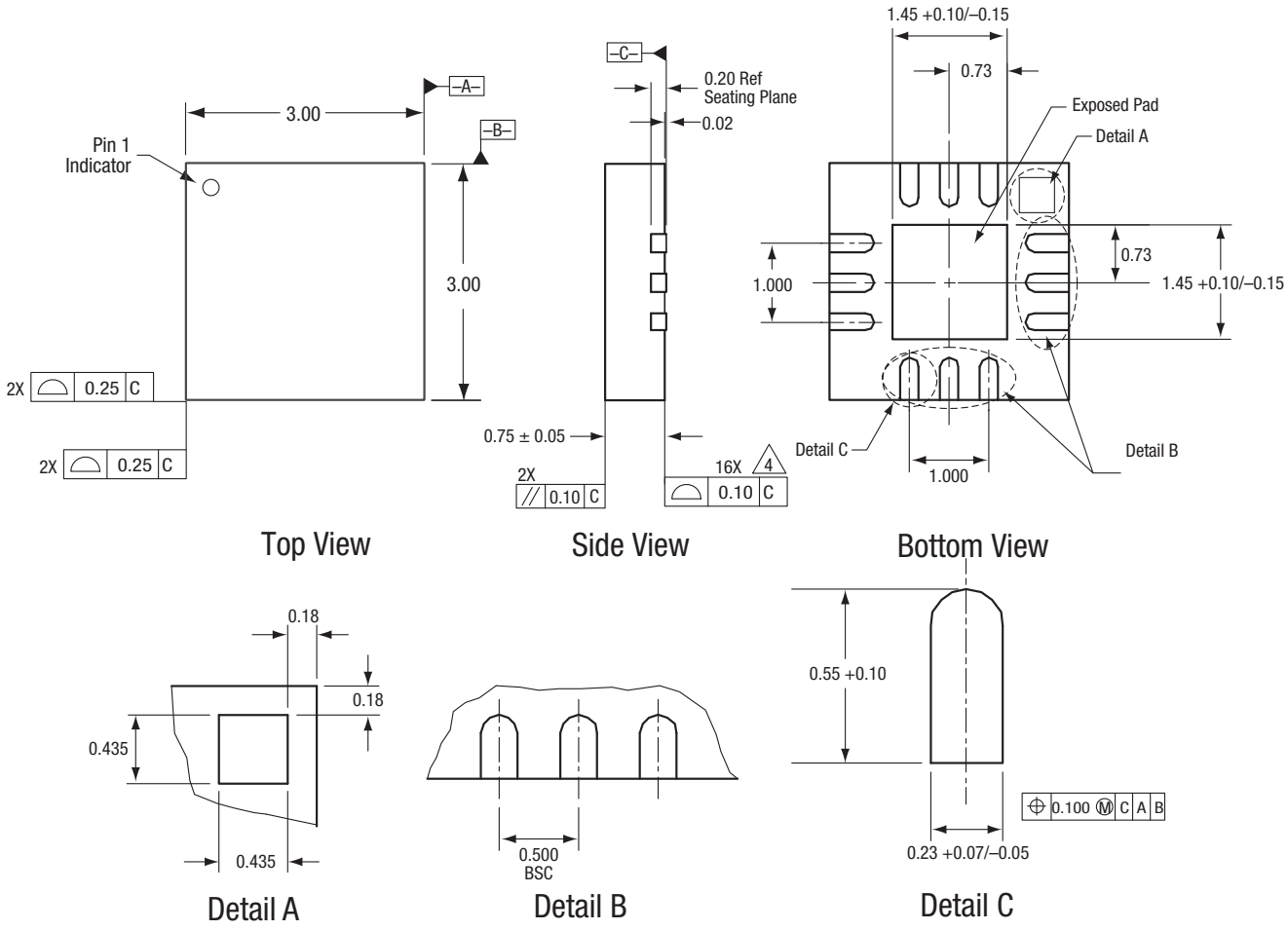


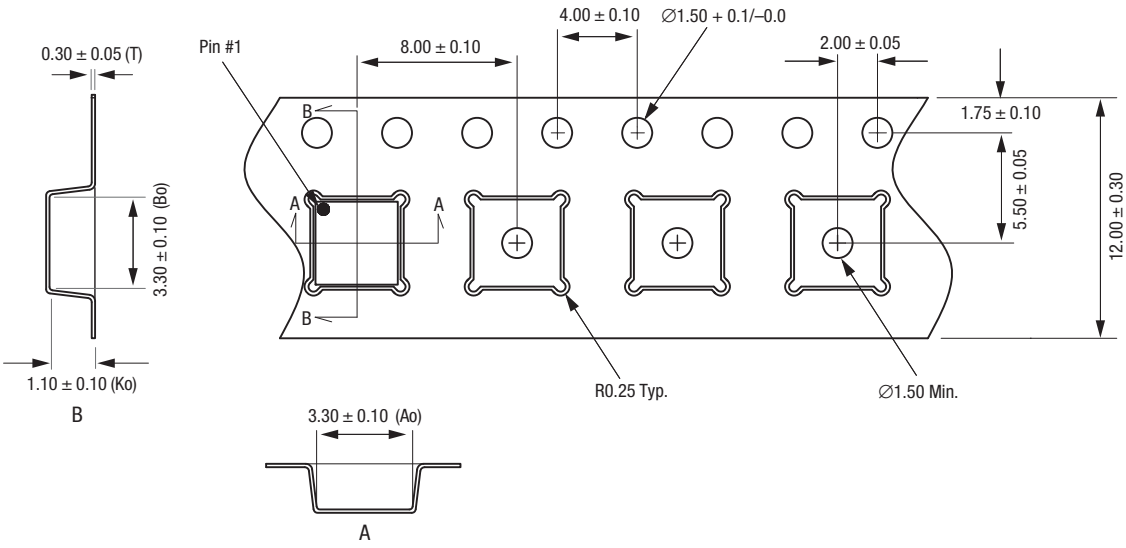
Figure 12. Typical Part Markings (Top View)



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the exposed heat sink slug as well as the terminals..
Plating requirement per source control drawing (SCD) 2504.
All contact points are pure matte tin, Pb-free surfaces.

S1542

Figure 13. SKY13299-321LF 12-Pin QFN Package Dimensions



Notes:
1. Carrier tape: black conductive polystyrene, non-bakeable material.
2. Cover tape material: transparent conductive HSA.
3. Cover tape size: 9.20 mm width.
4. All measurements are in millimeters.

S1698

Figure 14. SKY13299-321LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Numbers
SKY13299-321LF SPDT Switch	SKY13299-321LF	SKY13299-321LF-EVB

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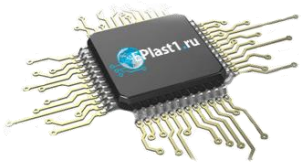

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