RICOH

R3118x SERIES

LOW VOLTAGE DETECTOR with individual SENSE pin and delay function

NO.EA-242-160229

OUTLINE

The R3118x series are CMOS-based voltage detector ICs with individual sense pin, high detector threshold accuracy and delay time, and ultra-low supply current, which can be operated at an extremely low voltage and is used for system reset as an example.

Each of these ICs consists of a voltage reference unit, a hysteresis comparator, resistors net for detector threshold setting, an output driver transistor, and a delay circuit.

V_{DD} supply pin for the IC and voltage supervisory sense pin are individual, therefore the output pin can keep "L" level even if the sense pin voltage is going down to 0V, or there is no indefinite range for the sense pin.

Since a delay circuit is built-in, by connecting an external capacitor, any output delay time can be set. In the R3118x series, detector released delay time can be set, and detector delay time is not influenced by the external capacitor for the delay time.

The detector threshold is fixed with high accuracy internally and does not require any adjustment.

The tolerance of the detector threshold is ±22.5mV ($-V_{DET_S}$<1.6V) or ±1.5% ($-V_{DET_S}$≥1.6V).

Minimum detector threshold voltage is 0.6V, ultra low voltage detector threshold can be set.

Output delay time for the detector release can be set with high accuracy. The tolerance of the IC side is ±30%.

Two output types, Nch open drain type and CMOS type are available. If the sense pin voltage becomes to equal or lower than the detector threshold voltage, the output voltage becomes "L", and if the sense pin voltage becomes to released voltage, the output voltage becomes "H" after the set delay time.

Three types of packages, SOT-23-5, SC-88A, and DFN(PLP)1212-6 are available.

FEATURES*

- Supply Current ..... Typ. 0.4μA (V_{SENSE}≥+V_{DET}, V_{DD}=6V)
  Consumption current through SENSE pin is not included.
- Operating Voltage Range ..... 1.0V to 6.0V (-40°C≤T_{opt}≤85°C)
- Detector Threshold Range ..... 0.6V to 5.0V (0.1V steps)
  (For other voltages, please refer to MARK INFORMATIONS.)
- Accuracy Detector Threshold ..... ±1.5% ($-V_{DET_S}$≥1.6V), ±22.5mV ($-V_{DET_S}$<1.6V)
- Temperature-Drift Coefficient of Detector Threshold ..... Typ. ±30ppm/°C
- Accuracy Detector Released ..... ±30%
- Temperature-Drift Coefficient of Detector Released ..... Typ. ±0.16ppm/°C
- Output Types ..... Nch Open Drain and CMOS
- Packages ..... DFN(PLP)1212-6, SC-88A , SOT-23-5

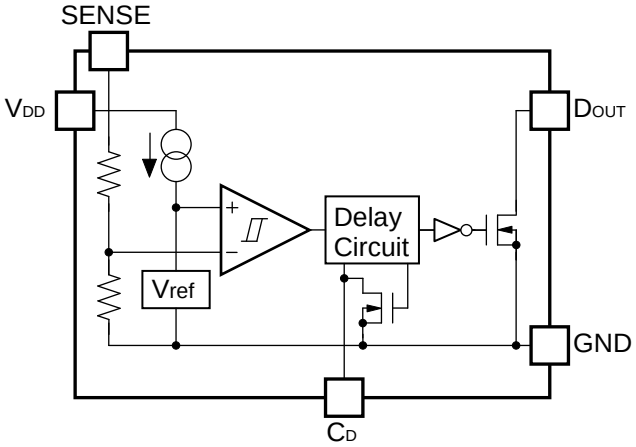
∗ Topt=25°C, unless otherwise noted.

APPLICATIONS

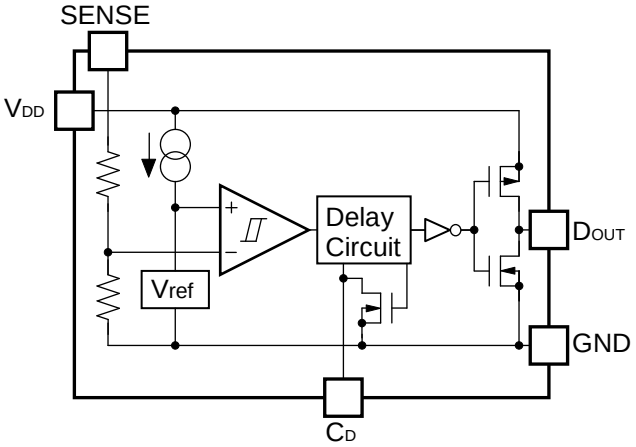
- CPU and Logic Circuit Reset
- Battery Checker
- Window Comparator / Level discrimination
- Battery Back-up Circuit
- Power Failure Detector

BLOCK DIAGRAMS

Nch Open Drain Output (R3118xxxxA)



CMOS Output (R3118xxxxC)



SELECTION GUIDE

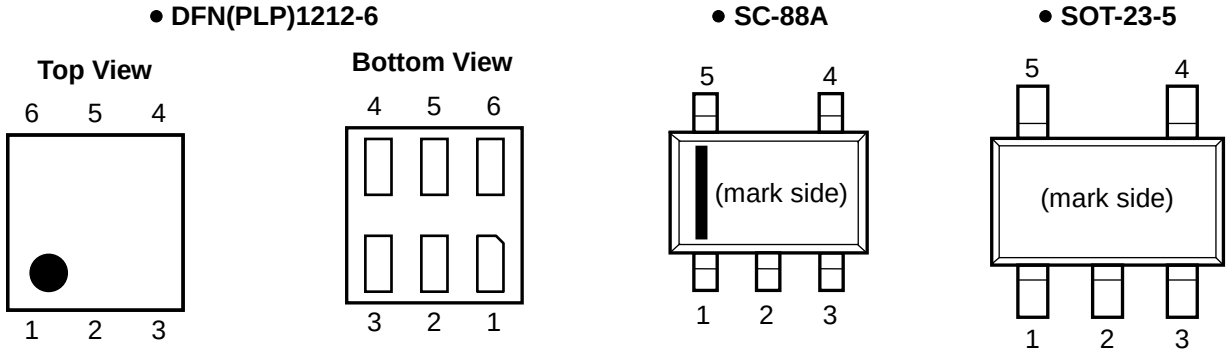
The package type, the detector threshold, the output type and the taping type for the ICs can be selected at the users' request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3118Kxx1∗-TR	DFN(PLP)1212-6	5,000 pcs	Yes	Yes
R3118Qxx2∗-TR-FE	SC-88A	3,000 pcs	Yes	Yes
R3118Nxx1∗-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

xx: The detector threshold can be designated in the range from 0.6V(06) to 5.0V(50) in 0.1V steps.
(For other voltages, please refer to MARK INFORMATIONS.)

∗ : Designation of Output Type
(A) Nch Open Drain
(C) CMOS

PIN CONFIGURATIONS



PIN DESCRIPTIONS

- **DFN(PLP)1212-6**

Pin No.	Symbol	Description
1	SENSE	Voltage Detector Voltage Sense Pin
2	GND	Ground Pin
3	C_D	Pin for External Capacitor (for setting output delay)
4	V_{DD}	Input Pin
5	NC	No Connection
6	D_{OUT}	Output Pin ("L" at detection)

- **SC-88A**

Pin No.	Symbol	Description
1	D_{OUT}	Output Pin ("L" at detection)
2	GND	Ground Pin
3	V_{DD}	Input Pin
4	C_D	Pin for External Capacitor (for setting output delay)
5	SENSE	Voltage Detector Voltage Sense Pin

- **SOT-23-5**

Pin No.	Symbol	Description
1	D_{OUT}	Output Pin ("L" at detection)
2	V_{DD}	Input Pin
3	GND	Ground Pin
4	C_D	Pin for External Capacitor (for setting output delay)
5	SENSE	Voltage Detector Voltage Sense Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{DD}	Supply Voltage	–0.3 to 7.0	V
V_{SENSE}	SENSE Pin Voltage	–0.3 to 7.0	V
V_{DOUT}	Output Voltage (Nch Open Drain Output)	–0.3 to 7.0	V
	Output Voltage (CMOS Output)	–0.3 to V_{DD}+0.3	
I_{DOUT}	Output Current Nch Driver (Sink Current)	20	mA
	Output Current Pch Driver (Source Current)	–5	
P_D	Power Dissipation (DFN(PLP)1212-6) *	400	mW
	Power Dissipation (SC-88A)*	380	
	Power Dissipation (SOT-23-5) *	420	
Topt	Operating Temperature Range	–40 to 85	°C
Tstg	Storage Temperature Range	–55 to 125	°C

*) For Power Dissipation, please refer to PACKAGE INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTRICAL CHARACTERISTICS

- **R3118xxxxA/C**

values indicate –40°C≤Topt≤85°C, -V_{DET_S} means set detector threshold, V_{DD}=1V to 6V, unless otherwise noted.

Topt=25°C

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage			1		6	V
-V_{DET}	Detector Threshold	-V_{DET_S} <1.6V	Topt=25°C	–V_{DET_S} –0.0225	–V_{DET_S}	–V_{DET_S} +0.0225	V
			–40°C≤Topt≤85°C	–V_{DET_S} –0.0375	–V_{DET_S}	–V_{DET_S} +0.0375	
		-V_{DET_S}≥1.6V	Topt=25°C	–V_{DET_S} × 0.985	–V_{DET_S}	–V_{DET_S} × 1.015	
			–40°C≤Topt≤85°C	–V_{DET_S} × 0.975	–V_{DET_S}	–V_{DET_S} × 1.025	
V_{HYS}	Detector threshold Hysteresis	Topt=25°C		–V_{DET_S} × 0.040	–V_{DET_S} × 0.055	–V_{DET_S} × 0.070	V
		–40°C≤Topt≤85°C		–V_{DET_S} × 0.035	–V_{DET_S} × 0.055	–V_{DET_S} × 0.075	

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
I_{SS}	Supply Current *1	V_{SENSE}=0V, V_{DD}=6V			0.480	1.450	μA
		V_{SENSE}=6V, V_{DD}=6V			0.400	1.200	
R_{SENSE}	Sense Resistor	V_{SENSE}=6V, V_{DD}=6V		9	34	58	MΩ
I_{DOUT}	Output Current (Driver Output Pin)	Nch V_{SENSE}=0V	V_{DD}=1V, V_{DOUT}=0.1V	0.150			mA
			V_{DD}=3V, V_{DOUT}=0.1V	0.550			
			V_{DD}=5V, V_{DOUT}=0.1V	0.850			
			V_{DD}=1V, V_{DOUT}=0.4V	0.400			
			V_{DD}=3V, V_{DOUT}=0.4V	2.100			
			V_{DD}=5V, V_{DOUT}=0.4V	3.300			
		Pch*2 V_{SENSE}=6V	V_{DD}=1V, V_{DOUT}=0.9V	6			μA
			V_{DD}=3V, V_{DOUT}=2.9V	30			
			V_{DD}=5V, V_{DOUT}=4.9V	45			
I_{LEAK}	Nch Driver Leakage Current *3	V_{SENSE}=6V, V_{DD}=6V, V_{DOUT}=6V				80	nA
R_{DIS}	C_D pin Discharge Tr. On Resistance	V_{SENSE}=6V, V_{DD}=1V, V_{CD}=0.4V		2.200		6.200	kΩ
		V_{SENSE}=6V, V_{DD}=3V, V_{CD}=0.4V		0.400		1.250	
		V_{SENSE}=6V, V_{DD}=5V, V_{CD}=0.4V		0.250		0.800	
t_{reset}	Detect Output Delay Time *4	Topt=25°C			80		μs
t_{delay}	Release Output Delay Time *5	Topt=25°C		70	100	130	ms
		−40°C≤Topt≤85°C		65	100	145	

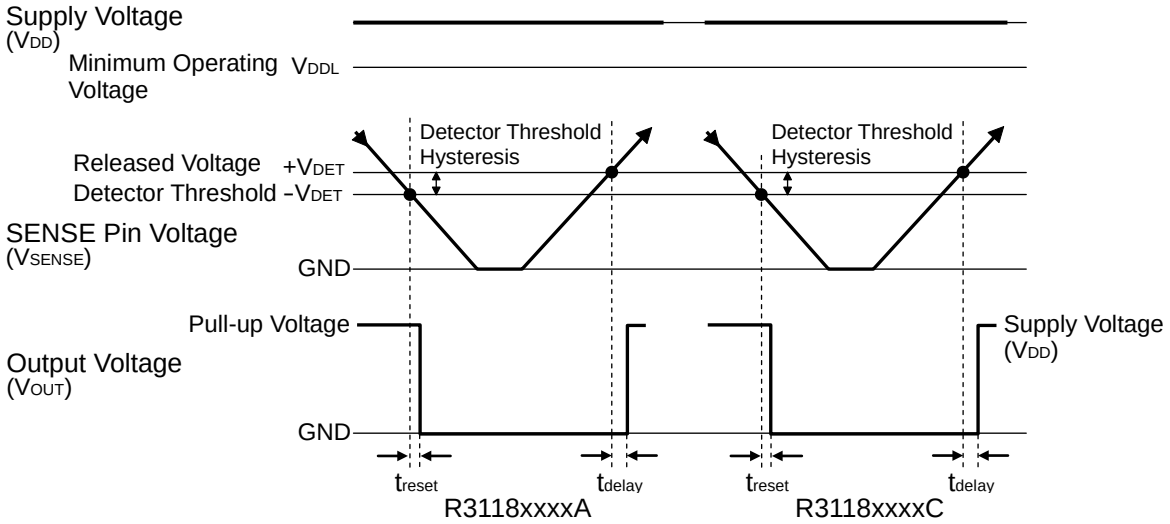
All of unit are tested and specified under load conditions such that Topt=25°C except for Detector Threshold Temperature Coefficient, Detector Output Delay Time and Release Output Delay Time.

∗1: Consumption current through SENSE pin is not included.
∗2: In case of CMOS type
∗3: In case of Nch Open Drain type
∗4: In the case of CMOS output type: In the case that a 0.022μF capacitor is connected to the C_D pin, the time interval from forcing pulsive voltage between -V_{DET_S}×1.155V and -V_{DET_S}×0.9 to SENSE pin, to when the output voltage of the D_{OUT} pin will reach from "H" to V_{DD}/2.
In the case of Nch Open drain output type: In the case that a 0.022μF capacitor is connected to the C_D pin and the D_{OUT} pin is pulled up to 5V with 470kΩ, the time interval from forcing pulsive voltage between -V_{DET_S}×1.155V and -V_{DET_S}×0.9V to SENSE pin, to when the output voltage reaches from "H" to 2.5V.
∗5: In the case of CMOS output type: In the case that a 0.022μF capacitor is connected to the C_D pin, the time interval from forcing pulsive voltage between -V_{DET_S}×0.9 and -V_{DET_S}×1.155V to SENSE pin, to when the output voltage of the D_{OUT} pin will reach from "L" to V_{DD}/2.
In the case of Nch Open drain output type: In the case that a 0.022μF capacitor is connected to the C_D pin and the D_{OUT} pin is pulled up to 5V with 470kΩ, the time interval from forcing pulsive voltage between -V_{DET_S}×0.9V and -V_{DET_S}x1.155V to SENSE pin, to when the output voltage reaches from "L" to 2.5V.

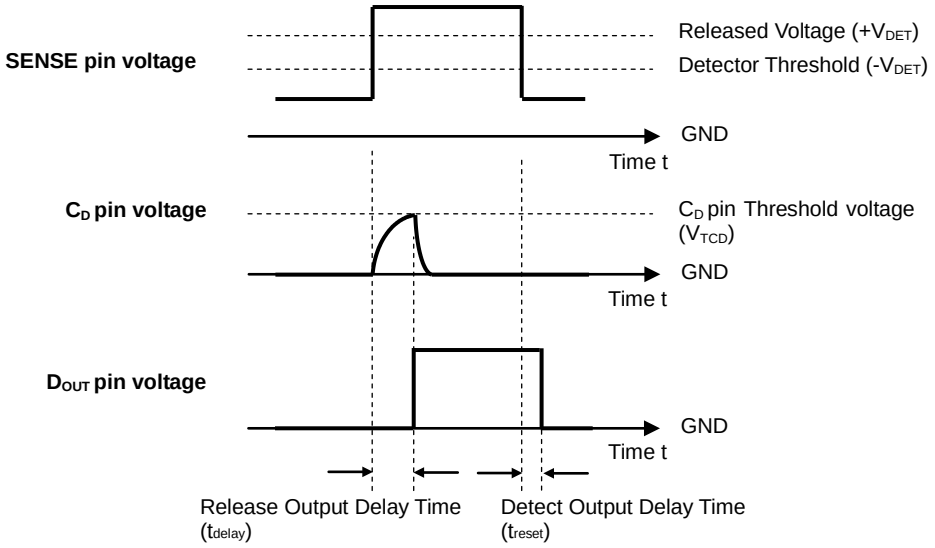
RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

TIMING CHART



DESCRIPTION OF OUTPUT DELAY OPERATION



Output Delay Operation Diagram

DEFINITION OF OUTPUT DELAY TIME

A higher voltage than the released voltage is forced to the SENSE pin, charge to the capacitor connected to C_D pin is started, then the C_D pin voltage increases. Until C_D pin voltage reaches to C_D pin threshold voltage, the output of D_{OUT} pin voltage keeps "L", then when C_D pin voltage is higher than C_D pin threshold voltage, the D_{OUT} pin voltage changes from "L" to "H". The released output delay time means the time interval from when the released voltage threshold or more voltage level is forced to SENSE pin to when D_{OUT} voltage changes from "L" to "H".

When the voltage of D_{OUT} pin reverses from "L" to "H", the discharge of the external capacitor connected to C_D pin starts. Therefore, the time interval from when the voltage lower than the detector threshold is forced to SENSE pin, to when the output voltage reverses from "H" to "L", or detector output delay time is constant and independent from the external capacitance value.

∗1. After the D_{OUT} pin voltage reverses from "L" to "H", if a voltage lower than the detector threshold is forced to SENSE pin before the capacitor connected to C_D pin is discharged, delay time will increase. The time interval (t_{DIS}) from when the capacitor connected to C_D pin is discharged completely to when the capacitor is charged to a certain C_D pin voltage (described as V_{CD} herein) can be calculated by power supply voltage (V_{DD}), external capacitance (C_D), on resistance of the C_D pin discharge transistor (R_{DIS}) as in the next formula:

$$t_{DIS} = -R_{DIS} \times C_D \times \ln(V_{CD}/V_{DD} \times 0.45))$$

∗2. During the released delay operation, only a small current will charge the external capacitor connected to C_D pin. If the leakage current between C_D pin and GND is large, the released delay time may increase or the detector may not be released.

∗3. During the released delay operation, if the V_{DD} pin voltage varies, the released output delay time will be also shift.

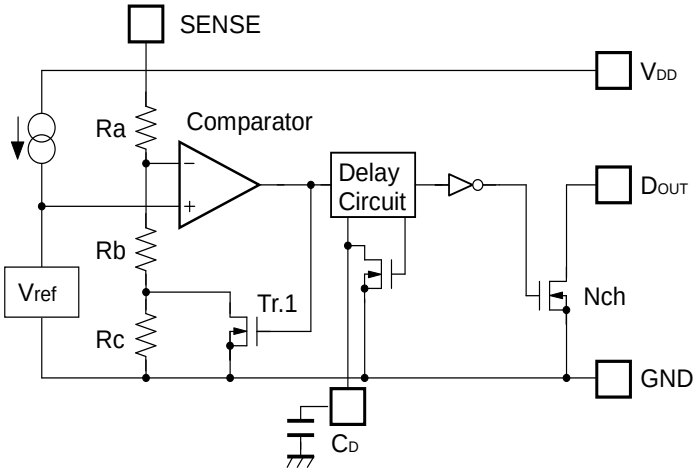
- **How to calculate the released output delay time**

The release output delay time (t_{delay}) can be calculated as in the next formula with an external capacitance value (C_D):

$$t_{delay}(s) = 4.545 \times 10^6 \times C_D(F)$$

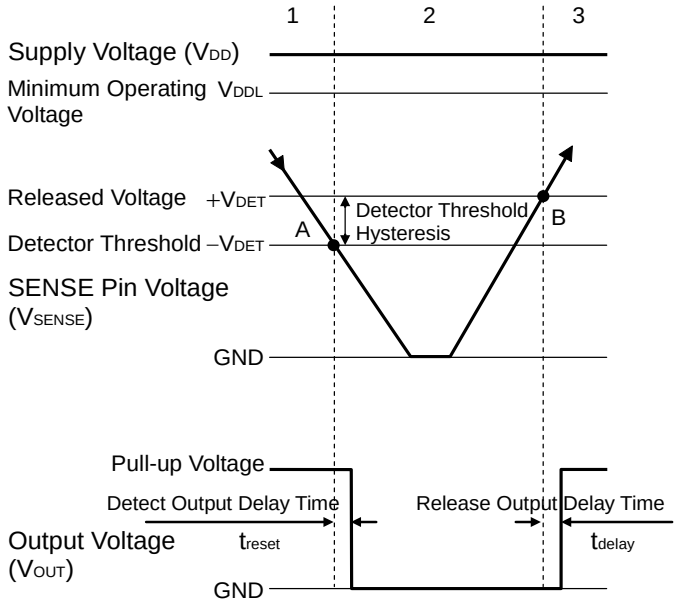
OPERATION

• Operation of R3118xxxxA



∗)DOUT pin should be pulled-up to VDD or an external voltage level.

Block diagram with an external capacitor (R3118xxxxA)



Step		1	2	3
Comparator (−) Pin Input Voltage		I	II	I
Comparator Output		L	H	L
Tr.1		OFF	ON	OFF
Output Tr.	Nch	OFF	ON	OFF

I $\frac{Rb+Rc}{Ra+Rb+Rc} \times V_{SENSE}$

II $\frac{Rb}{Ra+Rb} \times V_{SENSE}$

Operation Diagram

• Explanation of operation

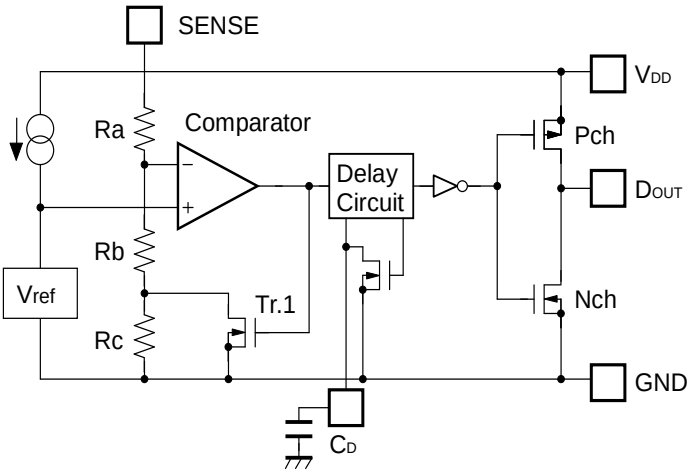
Step 1. The output voltage is equal to the pull-up voltage.

Step 2. At Point "A", Vref ≤ V_{SENSE}×(Rb+Rc)/(Ra+Rb+Rc) is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage (-V_{DET}). (When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the GND level.)

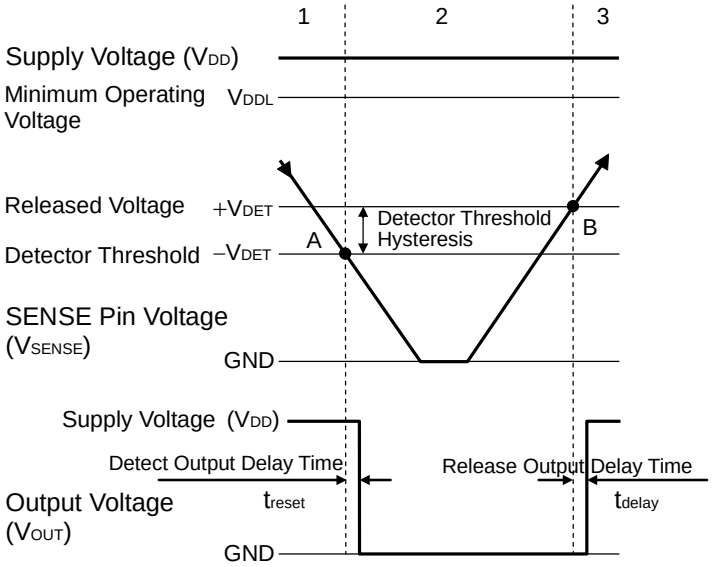
Step 3. At Point "B", V_{ref} ≤ V_{SENSE}×Rb/(Ra+Rb) is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the pull-up voltage. The voltage level of Point B means a released voltage (+V_{DET}).

∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

• Operation of R3118xxxxC



Block diagram with an external capacitor (R3118xxxxC)



Step		1	2	3
Comparator (–) Pin Input Voltage		I	II	I
Comparator Output		L	H	L
Tr.1		OFF	ON	OFF
Output Tr.	Pch	ON	OFF	ON
	Nch	OFF	ON	OFF

I $\frac{Rb+Rc}{Ra+Rb+Rc} \times V_{SENSE}$

II $\frac{Rb}{Ra+Rb} \times V_{SENSE}$

Operation Diagram

• Explanation of operation

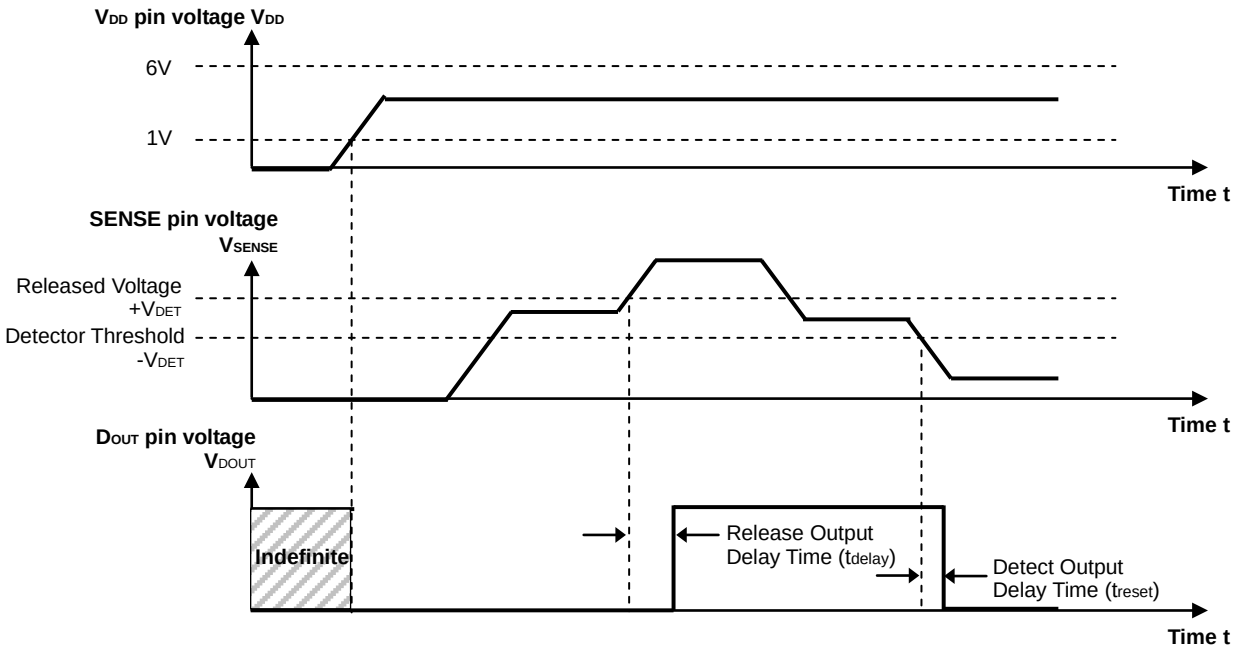
Step 1. The output voltage is equal to the supply voltage (V_{DD}).

Step 2. At Point "A", $V_{ref} \geq V_{SENSE} \times (Rb+Rc)/(Ra+Rb+Rc)$ is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage ($-V_{DET}$). (When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the GND level.)

Step 3. At Point "B", $V_{ref} \leq V_{SENSE} \times Rb/(Ra+Rb)$ is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the supply voltage (V_{DD}). The voltage level of Point B means a released voltage ($+V_{DET}$).

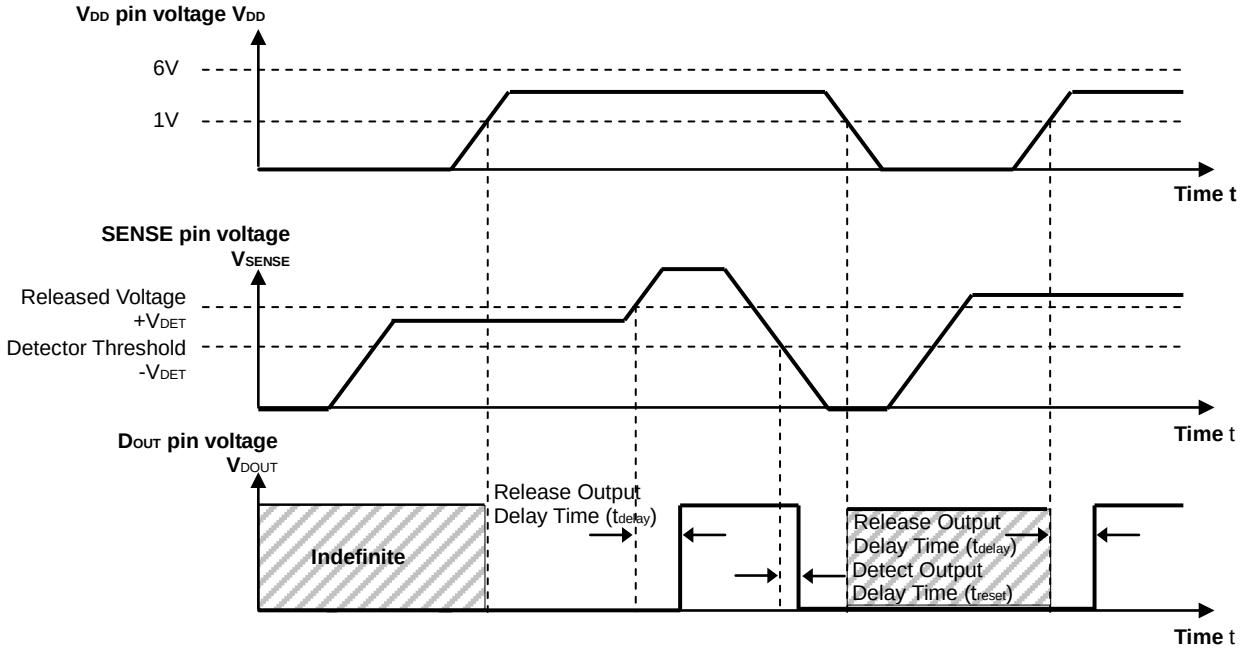
∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

- **In case of the SENSE pin voltage is forced after the V_{DD} pin voltage is forced.**



If a power supply (in the range from 1V to 6V) is forced to V_{DD} pin and a voltage is forced to SENSE pin, when the SENSE pin voltage is less than released voltage $+V_{DET}$, D_{OUT} pin becomes "L". When the SENSE pin voltage is equal or more than the released voltage $+V_{DET}$, D_{OUT} pin becomes "H".

- **In case of the V_{DD} pin voltage is forced after the SENSE pin voltage is forced.**



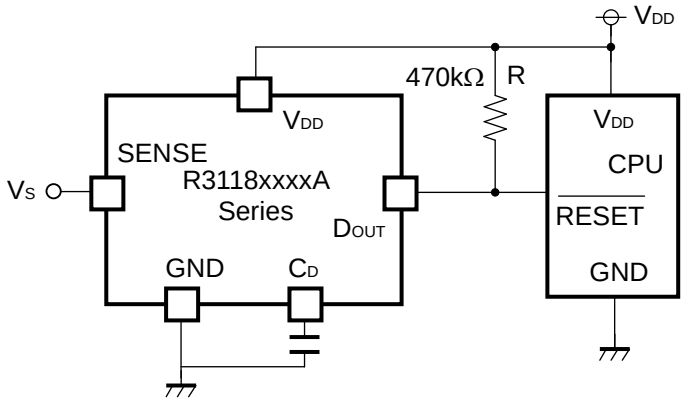
In the case of the SENSE pin voltage is less than released voltage $+V_{DET}$, when the V_{DD} pin voltage becomes to 1V or more, "L" output of D_{OUT} is determined. In case of the SENSE pin voltage is equal or more than the released voltage $+V_{DET}$, when the V_{DD} pin voltage becomes to 1V or more, "H" output of D_{OUT} is determined.

∗) If the turn on speed of the supply voltage of the V_{DD} pin up to 1V is slower than the1V/s, connect 0.001μF or more capacitor to C_D pin, otherwise, the output of D_{OUT} pin may indefinite.

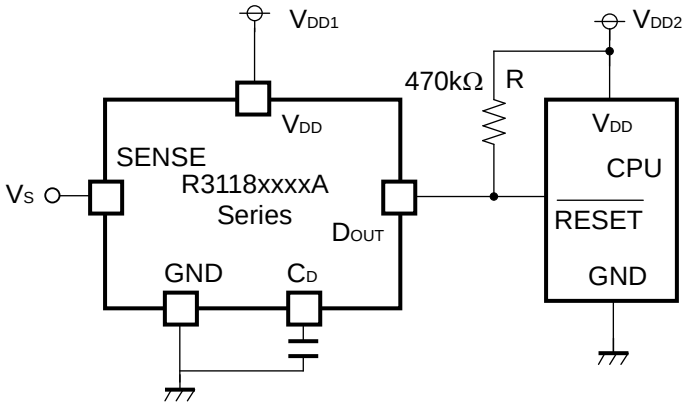
TYPICAL APPLICATION

- **R3118xxxxA CPU Reset Circuit (Nch Open Drain Output)**

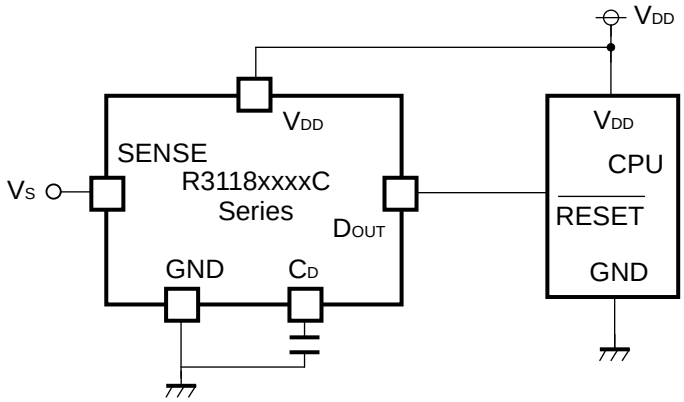
(1) V_{DD} pin Voltage to R3118xxxxA is equal to V_{DD} pin Voltage to CPU



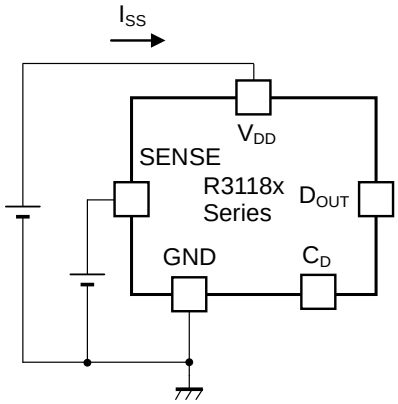
(2) V_{DD} pin Voltage to R3118xxxxA is unequal to V_{DD} pin Voltage to CPU



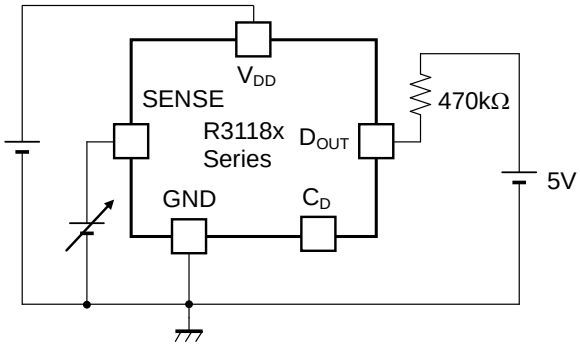
- **R3118xxxxC CPU Reset Circuit (CMOS Output)**



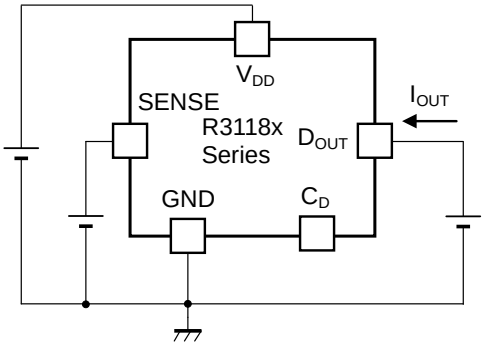
TEST CIRCUITS



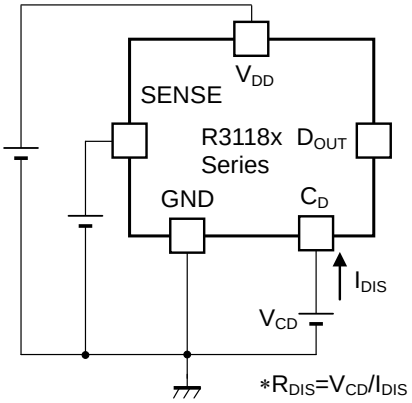
Supply Current Test Circuit



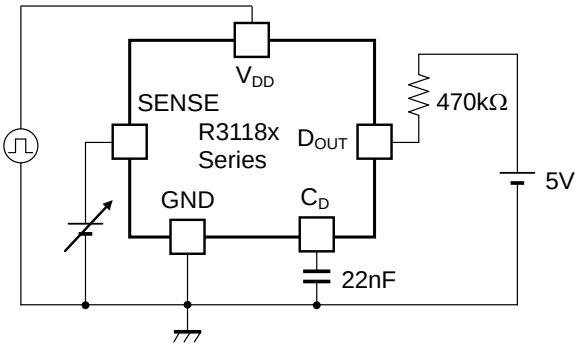
Detector Threshold Test Circuit
(Pull-up circuit is not necessary for CMOS Output type.)



Nch/Pch Driver Output Current Test Circuit



C_D pin Discharge Transistor On resistance Test Circuit

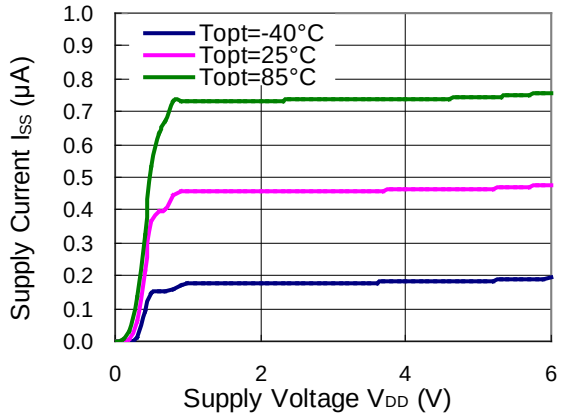


Detect output delay time/Release output delay time Test Circuit
(Pull-up circuit is not necessary for CMOS Output type.)

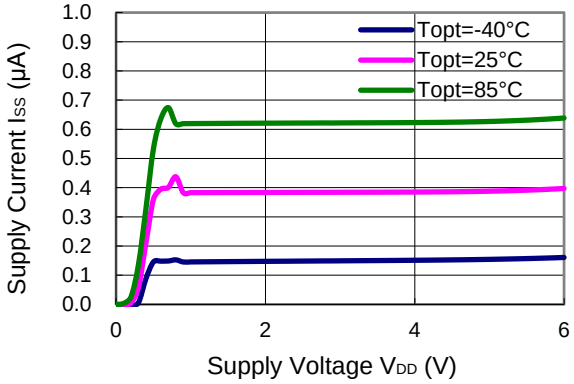
TYPICAL CHARACTERISTICS

1) Supply Current vs. Supply Voltage

R3118xxxxA/C (V_{SENSE}=0V)

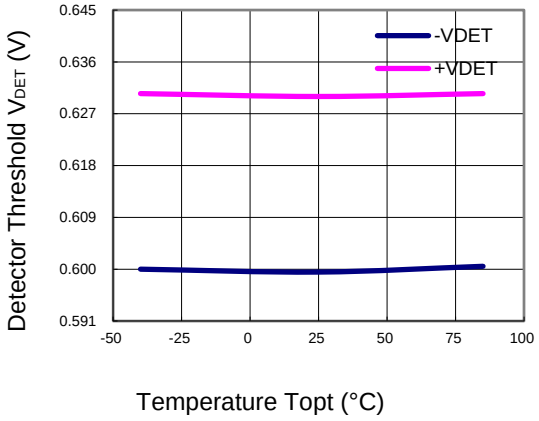


R3118xxxxA/C (V_{SENSE}=6V)

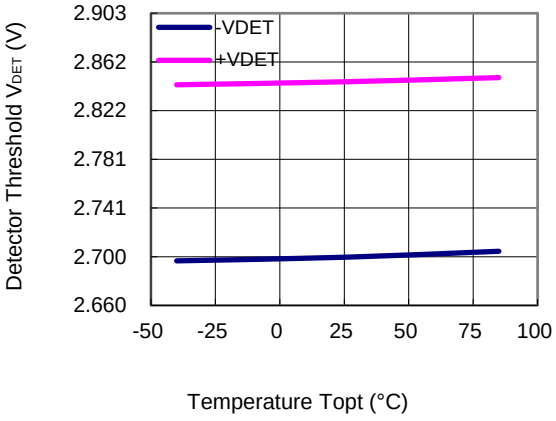


2) Detector Threshold vs. Temperature

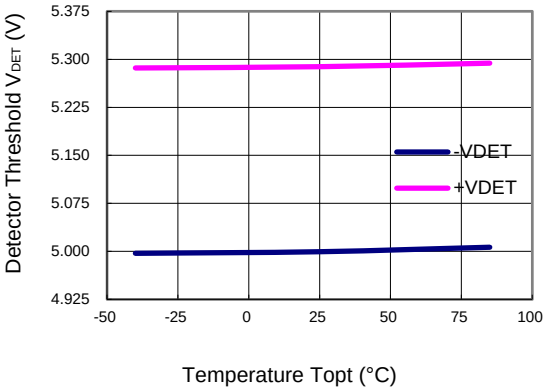
R3118x06xA/C (V_{DD}=5.3V)



R3118x27xA/C (V_{DD}=5.3V)

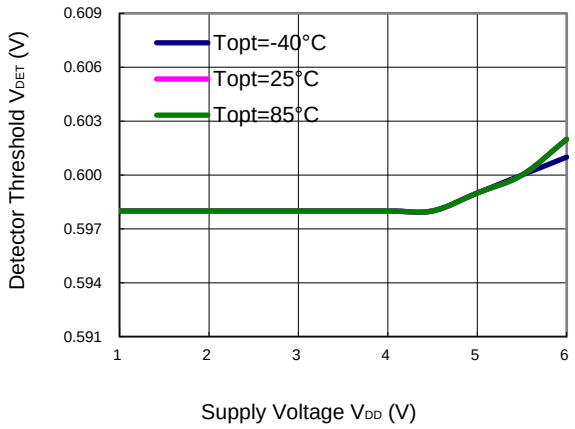


R3118x50xA/C (V_{DD}=5.3V)

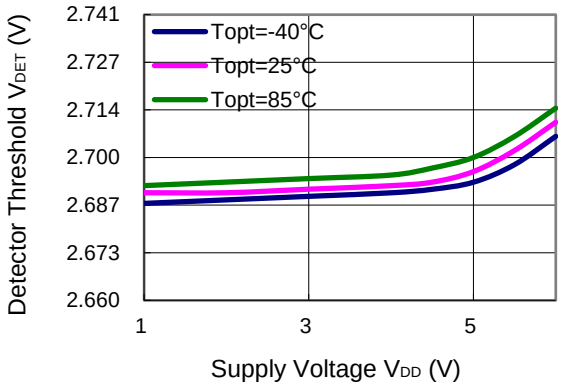


3) Detector Threshold vs. Supply Voltage

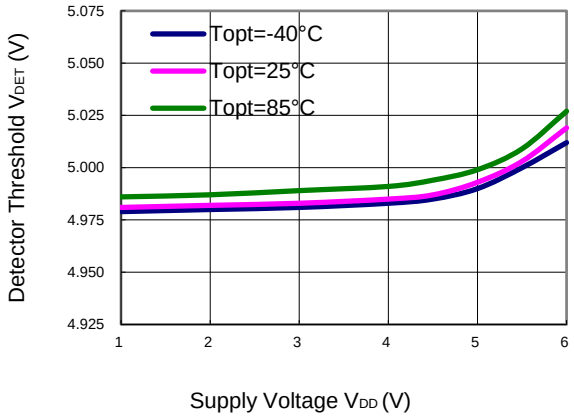
R3118x06xA/C



R3118x27xA/C

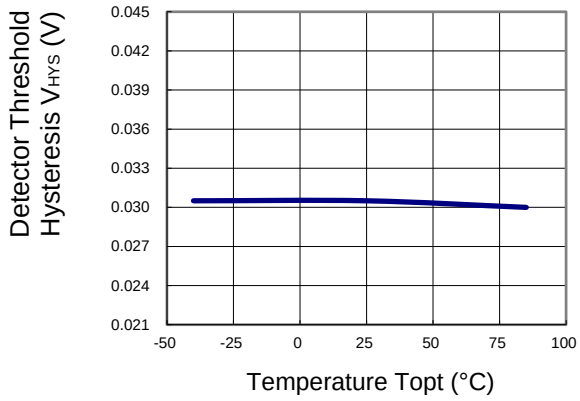


R3118x50xA/C

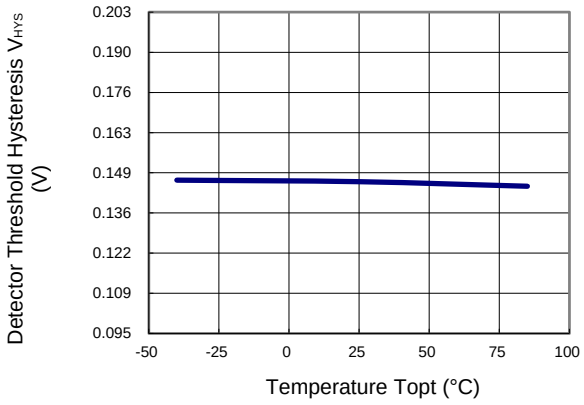


4) Hysteresis vs. Temperature

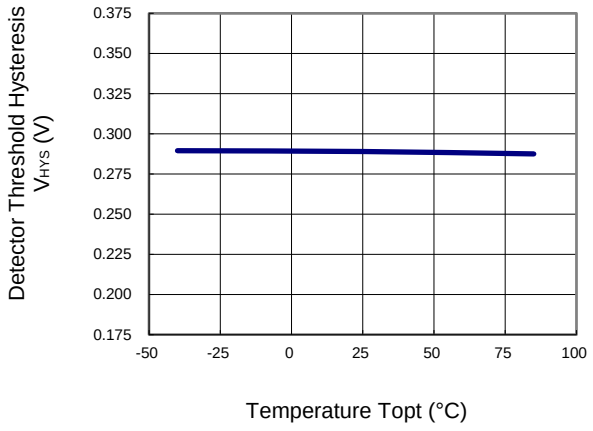
R3118x06xA/C (V_{DD}=5.3V)



R3118x27xA/C (V_{DD}=5.3V)

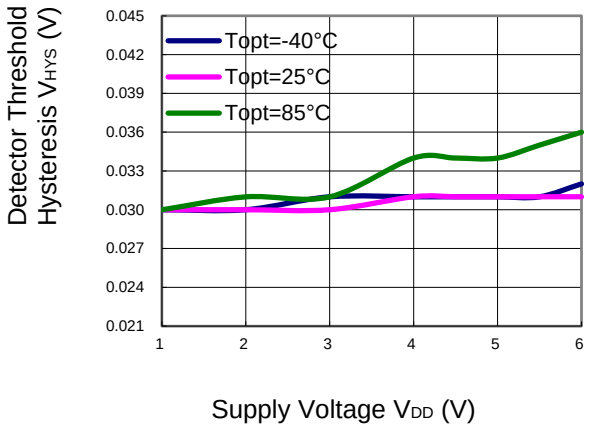


R3118x50xA/C (V_{DD}=5.3V)

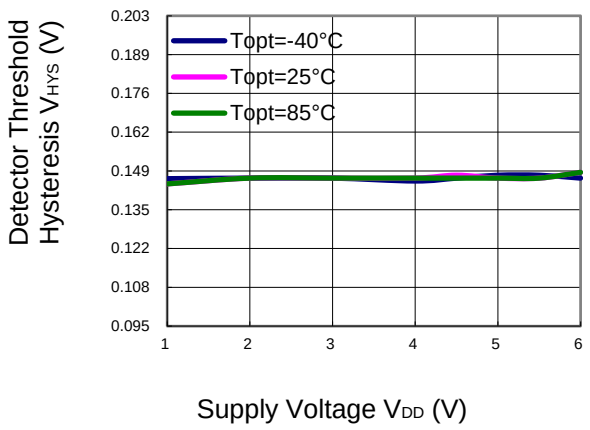


5) Hysteresis vs. Supply Voltage

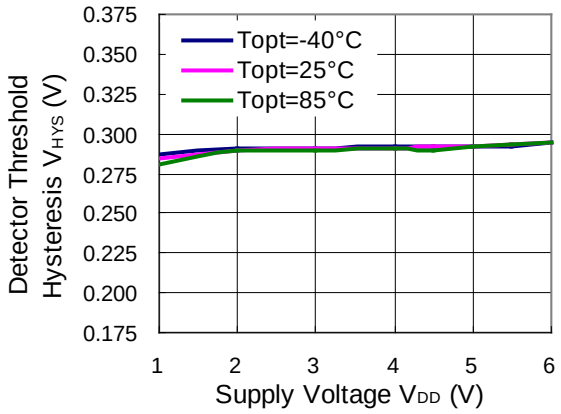
R3118x06xA/C



R3118x27xA/C



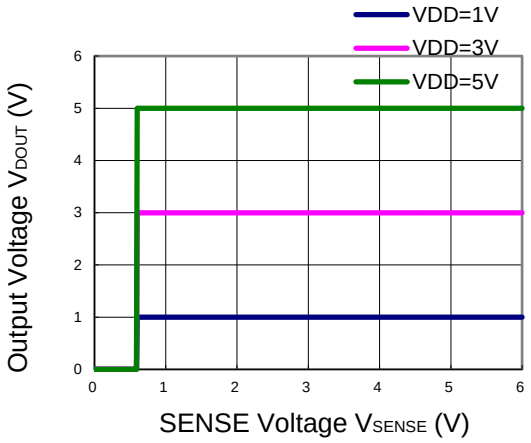
R3118x50xA/C



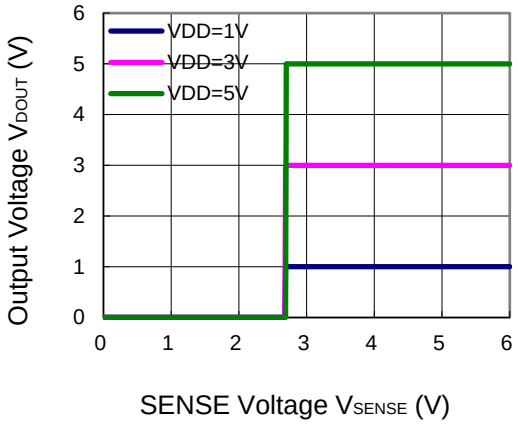
RICOH

6) Output Voltage vs. SENSE Voltage (DOUT pin is pulled up to VDD pin via 470kΩ.)

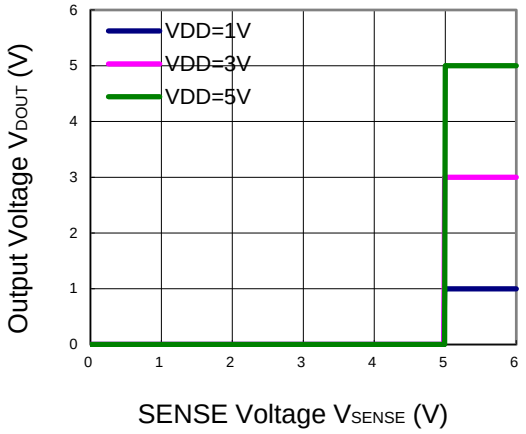
R3118x06xA/C



R3118x27xA/C

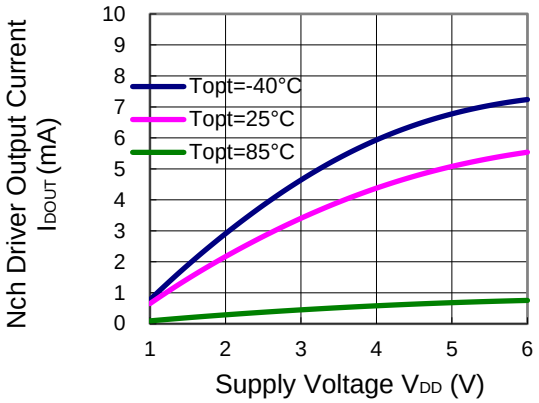


R3118x50xA/C



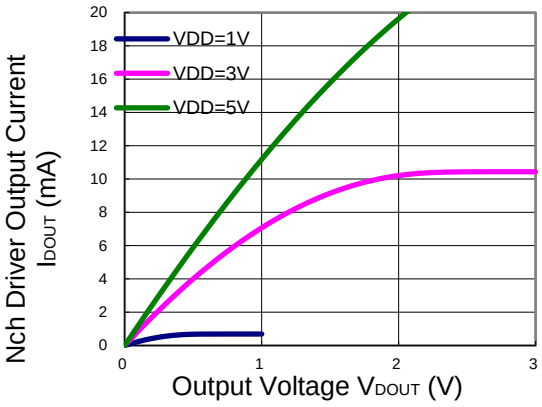
7) Nch Driver Output Current vs. Supply Voltage

R3118xxxxA/C (VDOUT=0.4V)



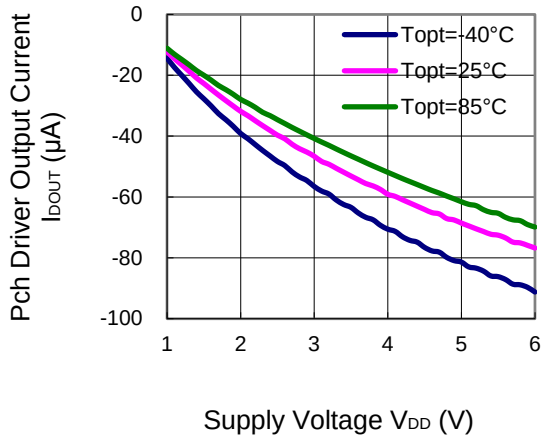
8) Nch Driver Output Current vs. Output Voltage

R3118xxxxA/C



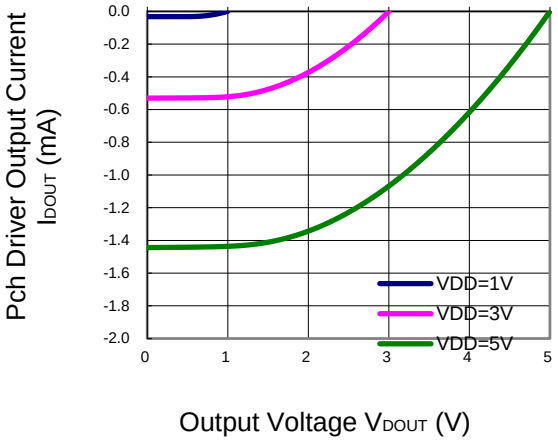
9) Pch Driver Output Current vs. Supply Voltage

R3118xxxxA/C (V_{DOUT}=V_{DD}–0.1V)



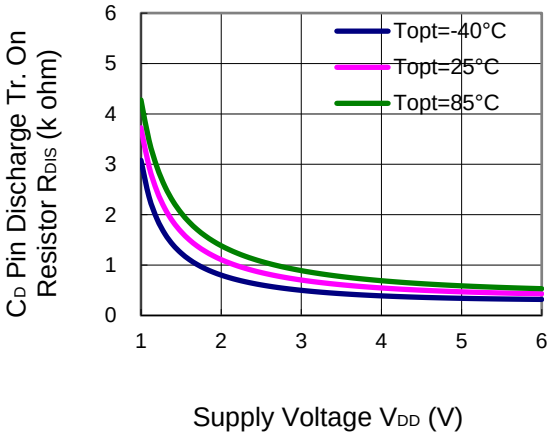
10) Pch Driver Output current vs. Output voltage

R3118xxxxA/C



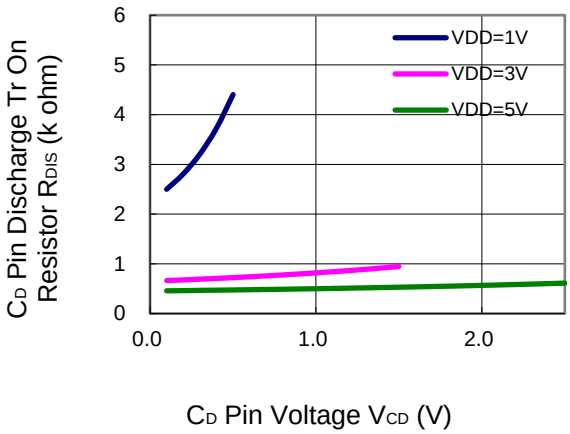
11) C_D pin Discharge Tr. On Resistance vs. Supply Voltage

R3118xxxxA/C (V_{CD}=0.4V)



12) C_D pin Discharge Transistor On Resistance vs. C_D pin voltage

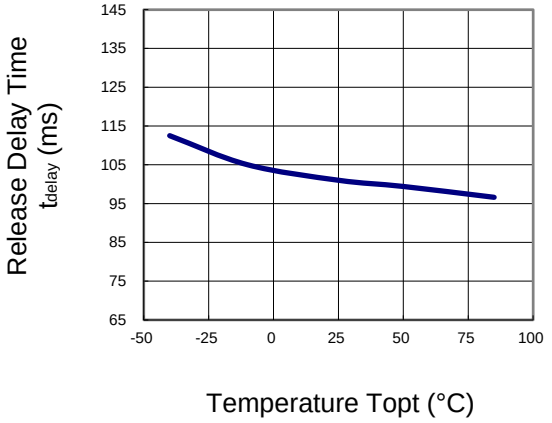
R3118xxxxA/C



RICOH

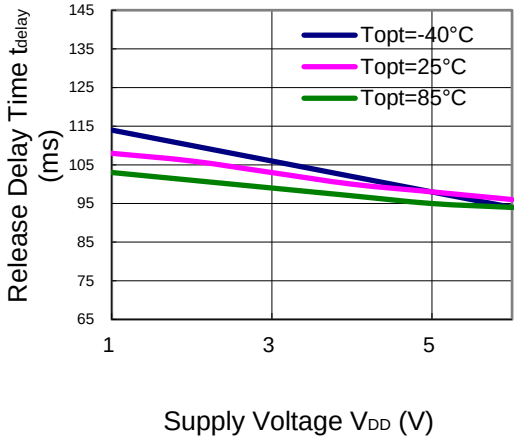
13) Release Output Delay Time vs. Temperature

R3118xxxxA/C (V_{DD}=4V, C_D=0.022μF)



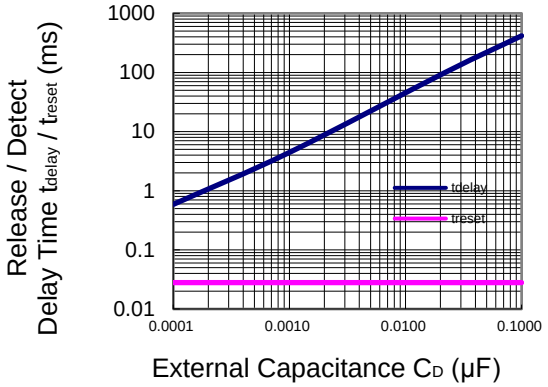
14) Release Output Delay Time vs. Supply Voltage

R3118xxxxA/C (C_D=0.022μF)

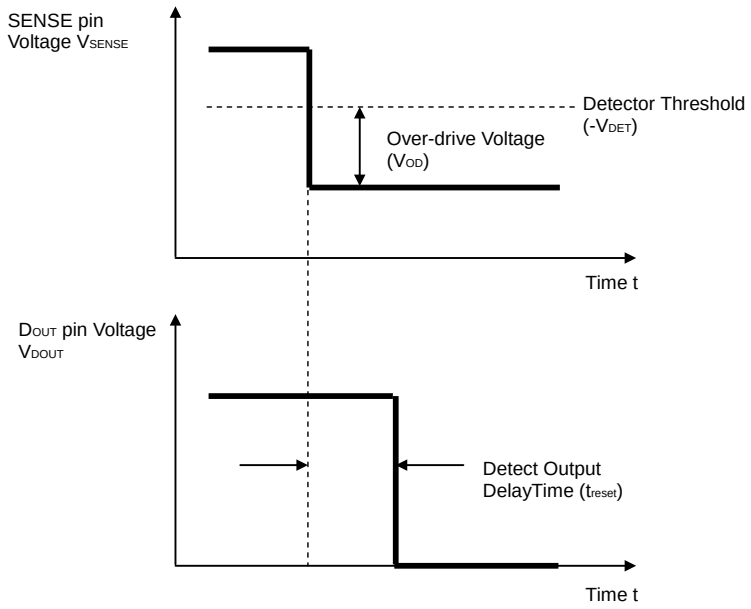


15) Detect Output Delay Time/Release Output Delay Time vs. C_D pin External Capacitance

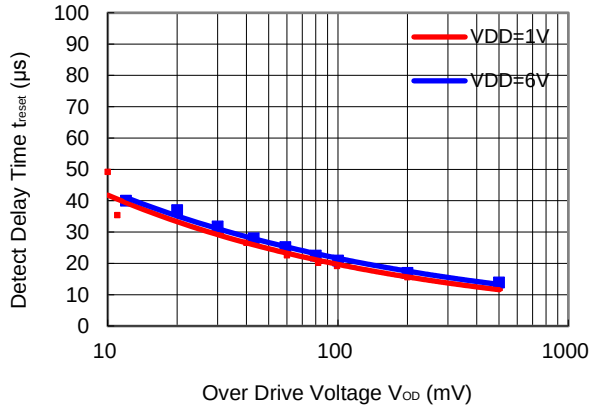
R3118xxxxA/C (V_{DD}=4V)



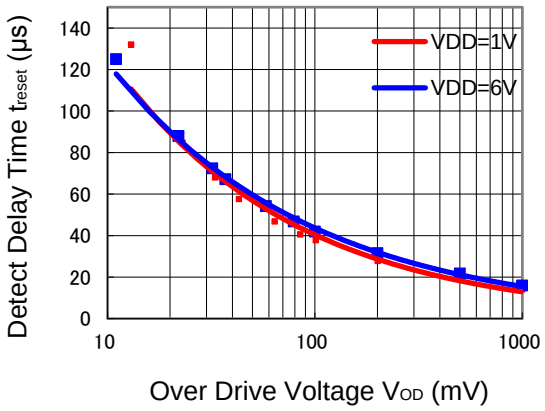
16) Detect Output Delay time vs. Over-drive Voltage



R3118x06xA/C（CD=none）

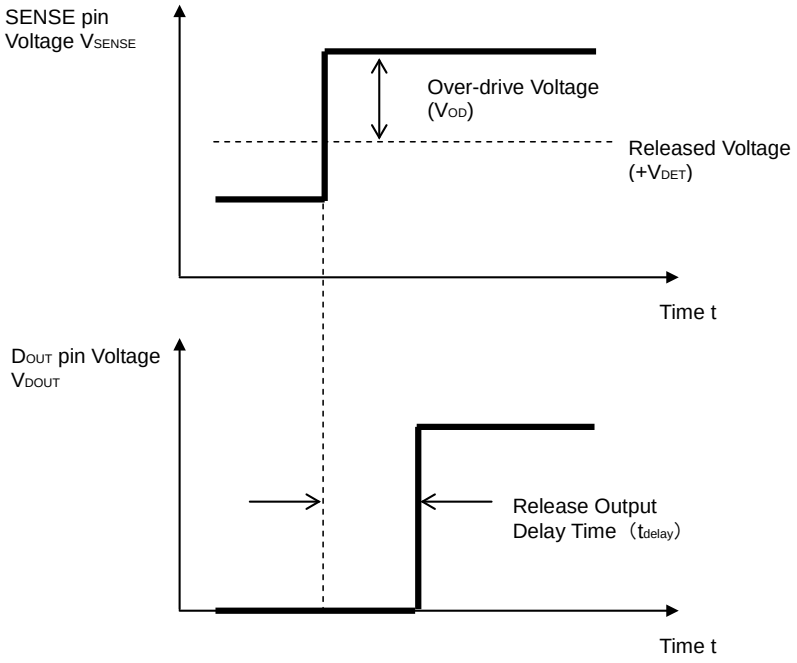


R3118x50xA/C（CD=none）

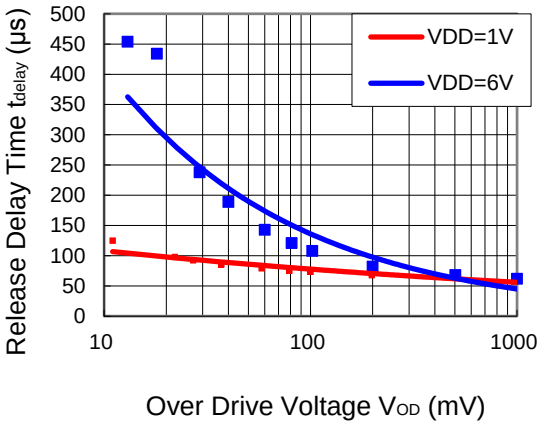


The pulse shorter than the detect output delay time cannot be detected, and "L" does not output from DOUT pin.

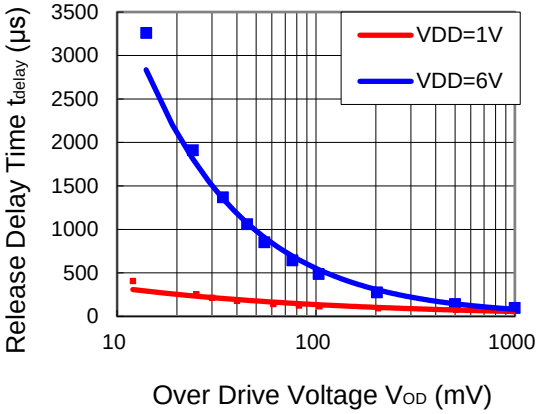
17) Release Output Delay time vs. Over-drive Voltage



R3118x06xA/C（CD=none）



R3118x50xA/C（CD=none）



· If the pulse is shorter than the output release delay time, the R3118 cannot be released and "H" does not output from DOUT pin.

· If the attachment capacitor for CD pin for setting a delay time is too small and the difference between the released voltage threshold and the actual released voltage is too small or the slope for rising voltage of the SENSE pin is too slow, the output delay time tolerance will be worse.

Ex. Attachment capacitor=0.0001µF, Released voltage threshold=4.725V, Actual released voltage=4.75V In this case, the calculated delay time=0.4545ms, however, over-drive voltage is only 25mV. Therefore, the actual delay time will be approximately 2.4545ms. If the attachment capacitor=0.001µF and other conditions are same as above, the calculated delay time=4.545ms, and the actual delay time will be approximately 6.545ms. If the attachment capacitor=0.01µF and other conditions are same as above, the calculated delay time=45.45ms, and the actual delay time will be approximately 47.45ms.

TECHNICAL NOTES

When connecting resistors to the device's input pin

When connecting a resistor (R1) to an input of this device, the input voltage decreases by [Device's Consumption Current] x [Resistance Value] only. And, the cross conduction current*1, which occurs when changing from the detecting state to the release state, is decreased the input voltage by [Cross Conduction Current] x [Resistance Value] only. And then, this device will enter the re-detecting state if the input voltage reduction is larger than the difference between the detector voltage and the released voltage.

When the input resistance value is large and the VDD is gone up at mildly in the vicinity of the released voltage, repeating the above operation may result in the occurrence of output.

As shown in Figure A/B, set R1 to become 100 kΩ or less as a guide, and connect C_{IN} of 0.1 μF and more to between the input pin and GND. Besides, make evaluations including temperature properties under the actual usage condition, with using the evaluation board like this way. As a result, make sure that the cross conduction current has no problem.

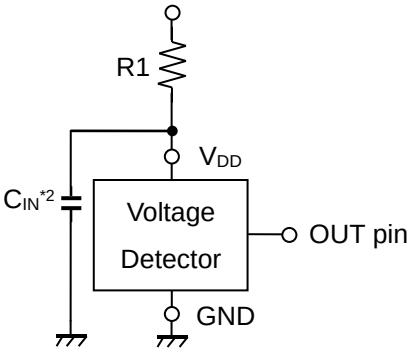


Figure A

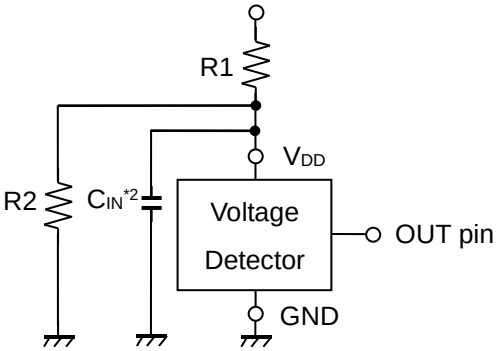


Figure B

*1 In the CMOS output type, a charging current for OUT pin is included.
*2 Note the bias dependence of capacitors.

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