

Description

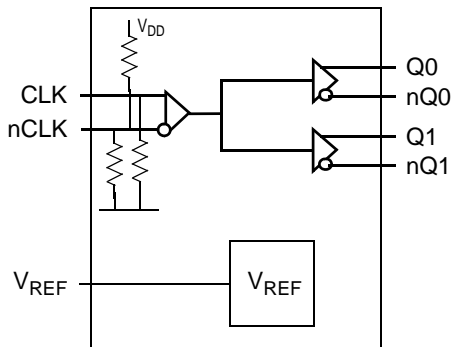
The IDT8P34S1102I is a high-performance differential LVDS fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals.

The IDT8P34S1102I is characterized to operate from a 1.8V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the IDT8P34S1102I ideal for those clock distribution applications demanding well-defined performance and repeatability. One differential input and two low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the differential device input. The device is optimized for low power consumption and low additive phase noise.

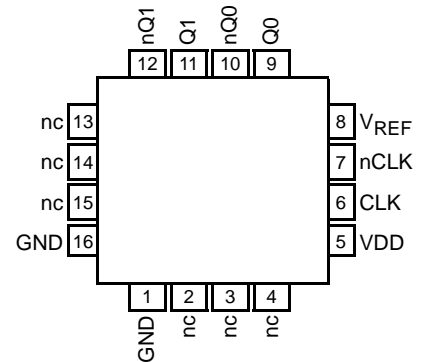
Features

- Two low skew, low additive jitter LVDS output pairs
- One differential clock input pair
- Differential CLK, nCLK pairs can accept the following differential input levels: LVDS, CML
- Maximum input clock frequency: 1.2GHz
- Output skew: 3ps (typical)
- Propagation delay: 400ps (maximum)
- Low additive phase jitter, RMS; $f_{REF} = 156.25\text{MHz}$, 12kHz- 20MHz: 42fs (typical)
- Maximum device current consumption (I_{EE}): 48mA
- Full 1.8V supply voltage
- Lead-free (RoHS 6), 16-Lead VFQFN packaging
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



IDT8P34S1102I
16-lead VFQFN

3mm x 3mm x 0.925mm package body
1.7mm x 1.7mm ePad Size
NL Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions^{Note 1.}

| Number | Name | Type | | Description |
|---------------------|------------------|--------|---------------------|---|
| 1, 16 | GND | Power | | Power supply ground. |
| 2, 3, 4, 13, 14, 15 | nc | Unused | | Do not connect. |
| 5 | V _{DD} | Power | | Power supply pins. |
| 6 | CLK | Input | Pulldown | Non-inverting differential clock/data input. |
| 7 | nCLK | Input | Pulldown/ Pullup | Inverting differential clock input. |
| 8 | V _{REF} | Output | | Bias voltage reference. Provides an input bias voltage for the CLK, nCLK input pair in AC-coupled applications. Refer to <i>Figures 2B and 2C</i> for applicable AC-coupled input interfaces. |
| 9, 10 | Q0, nQ0 | Output | | Differential output pair 0. LVDS interface levels. |
| 11, 12 | Q1, nQ1 | Output | | Differential output pair 1. LVDS interface levels. |

1. *Pulldown and Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 2 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|---------------------------------|
| Supply Voltage, V _{DD} | 4.6V |
| Inputs, V _I | -0.5V to V _{DD} + 0.5V |
| Outputs, I _O Continuous Current Surge Current | 10mA 15mA |
| Input Sink/Source, I _{REF} | ±2mA |
| Maximum Junction Temperature, T _{J,MAX} | 125°C |
| Storage Temperature, T _{STG} | -65°C to 150°C |
| ESD - Human Body Model ^{Note 1.} | 2000V |
| ESD - Charged Device Model ^{Note 1.} | 1500V |

1. According to JEDEC JS-001-2012/JESD22-C101E.

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|---|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| I_{DD} | Power Supply Current | Q0 to Q1 terminated 100Ω between nQx, Qx | | 40 | 48 | mA |

Table 3B. Differential Input Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|--|---------|---------|-----------------------|---------------|
| I_{IH} | Input High Current | CLK, nCLK $V_{IN} = V_{DD} = 1.89V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK $V_{IN} = 0V, V_{DD} = 1.89V$ | -10 | | | μA |
| | | nCLK $V_{IN} = 0V, V_{DD} = 1.89V$ | -150 | | | μA |
| V_{REF} | Reference Voltage for Input Bias ^{Note 1.} | $I_{REF} = +100\mu\text{A}, V_{DD} = 1.8V$ | 0.9 | | 1.30 | V |
| V_{PP} | Peak-to-Peak Voltage ^{Note3.} | $V_{DD} = 1.89V$ | 0.2 | | 1.0 | V |
| V_{CMR} | Common Mode Input Voltage ^{Note 2.} Note 3. | | 0.9 | | $V_{DD} - (V_{PP}/2)$ | V |

- V_{REF} specification is applicable to the AC-coupled input interfaces shown in *Figures 2B and 2C*.
- Common mode input voltage is defined as crosspoint voltage.
- V_{IL} should not be less than $-0.3V$ and V_{IH} should not be higher than V_{DD} .

Table 3C. LVDS DC Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C ^{Note 1.}

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|---------------------------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | outputs loaded with 100Ω | 247 | | 454 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.0 | | 1.40 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

- Output drive current must be sufficient to drive up to 30cm of PCB trace (assume nominal 50Ω impedance)

AC Electrical Characteristics

Table 4. AC Electrical Characteristics, $V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85° Note 1.

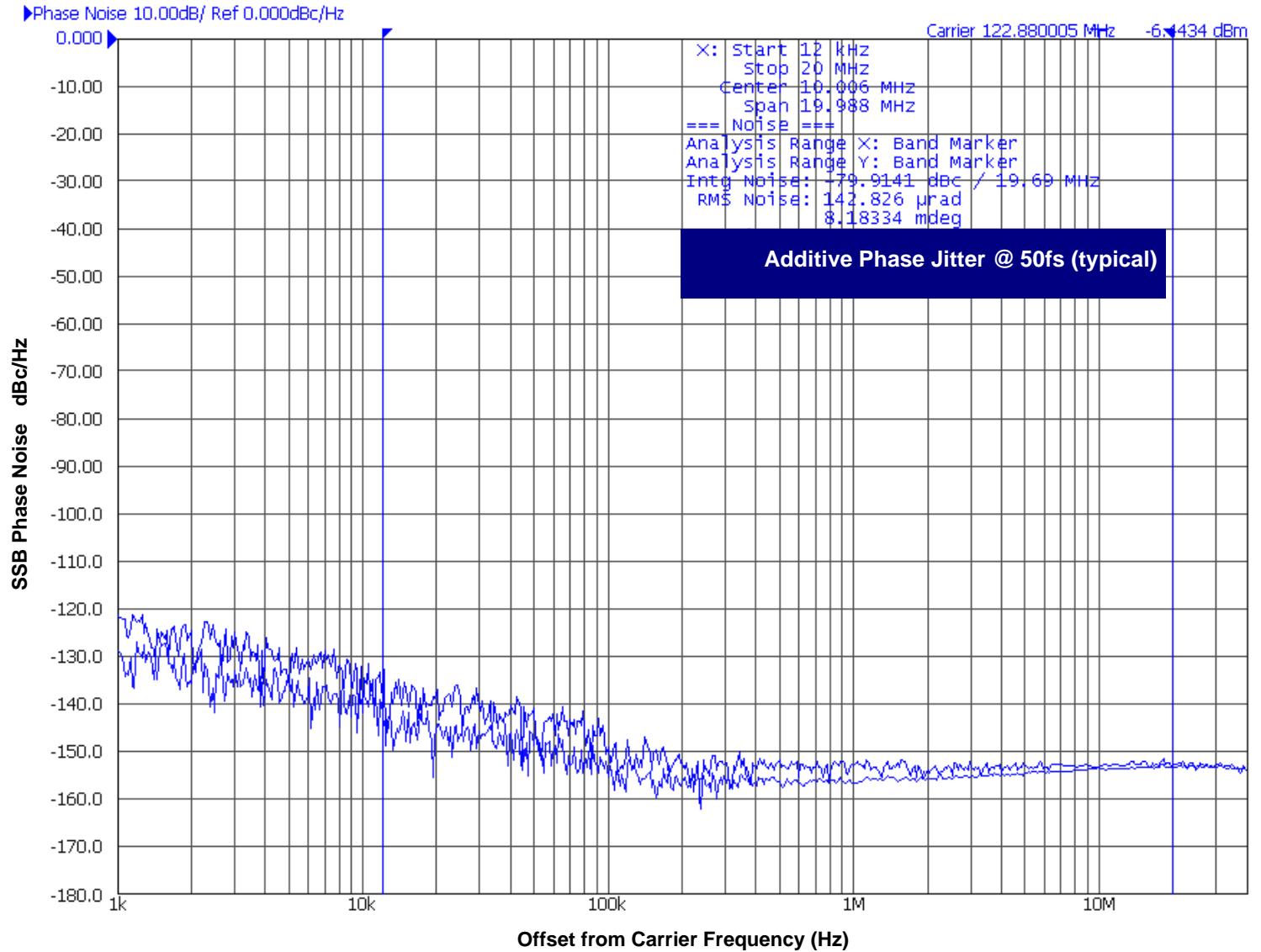
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|---|---|---------|---------|---------|-------|
| f_{REF} | Input Frequency CLK, nCLK | | | | 1.2 | GHz |
| $\Delta V/\Delta t$ | Input Edge Rate CLK, nCLK | | 1.5 | | | V/ns |
| t_{PD} | Propagation Delay ^{Note 2. Note 3.} | CLK, nCLK to any Qx, nQx | 150 | | 400 | ps |
| $t_{sk(o)}$ | Output Skew ^{Note 4. Note 5.} | | | 3 | 15 | ps |
| $t_{sk(p)}$ | Pulse Skew | $f_{REF} = 100\text{MHz}$ | | | 20 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew ^{Note 6.} | | | | 250 | ps |
| t_{JIT} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | $f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 1kHz – 40MHz | | 61 | 85 | fs |
| | | $f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 10kHz – 20MHz | | 50 | 62 | fs |
| | | $f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 12kHz – 20MHz | | 50 | 62 | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 1kHz – 40MHz | | 63 | 85 | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 10kHz – 20MHz | | 42 | 61 | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$, Integration Range: 12kHz – 20MHz | | 42 | 61 | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 1kHz – 40MHz | | 76 | 100 | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 10kHz – 20MHz | | 55 | 74 | fs |
| | | $f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$, Integration Range: 12kHz – 20MHz | | 55 | 74 | fs |
| t_R / t_F | Output Rise/ Fall Time | 10% to 90%, outputs loaded with 100 Ω | | 200 | 400 | ps |
| | | 20% to 80%, outputs loaded with 100 Ω | | 115 | 260 | ps |

- Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- Measured from the differential input crossing point to the differential output crossing point.
- Input V_{PP} is 0.4V.
- Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
- This parameter is defined in accordance with JEDEC Standard 65.
- Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



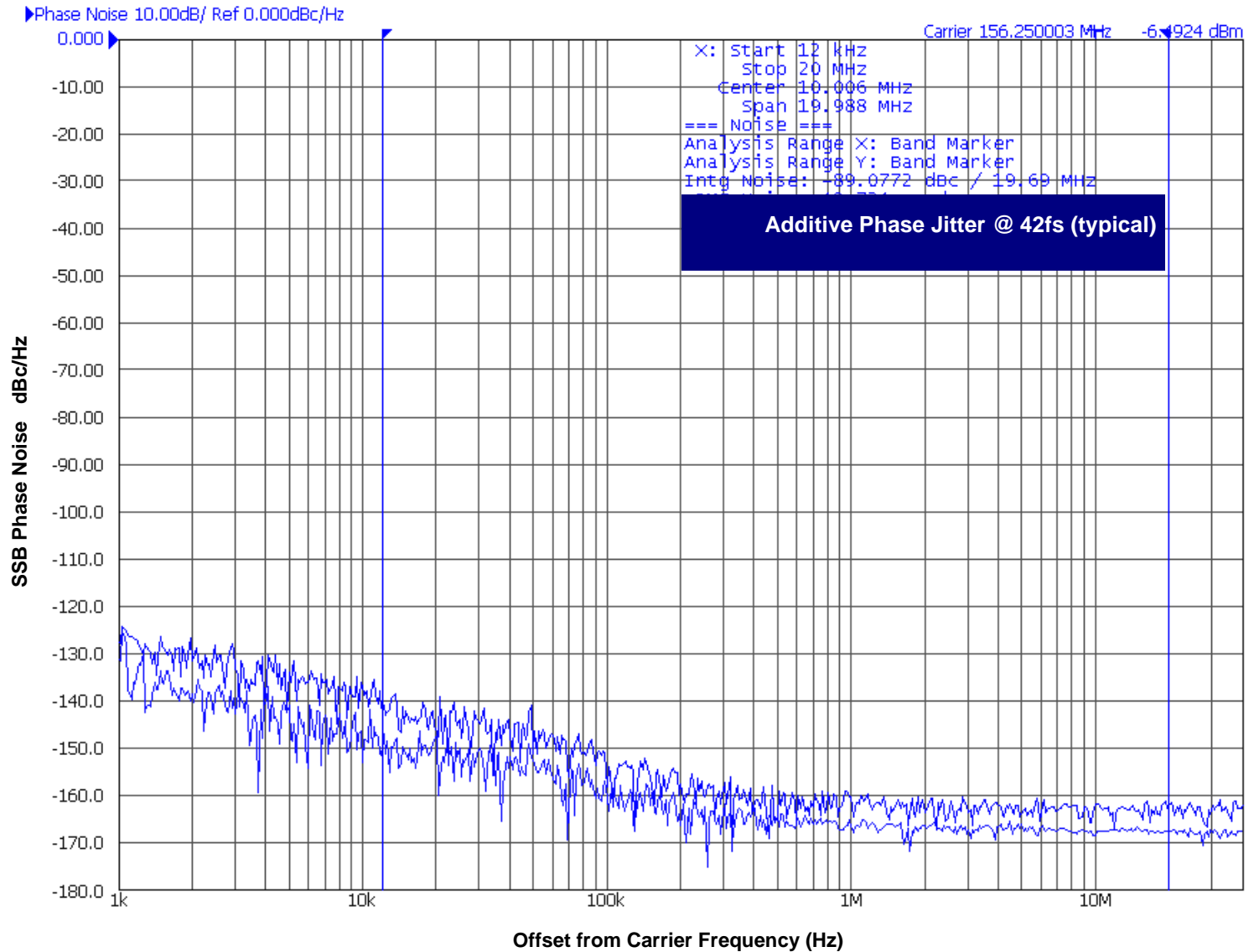
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzel Oscillator as the input source.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

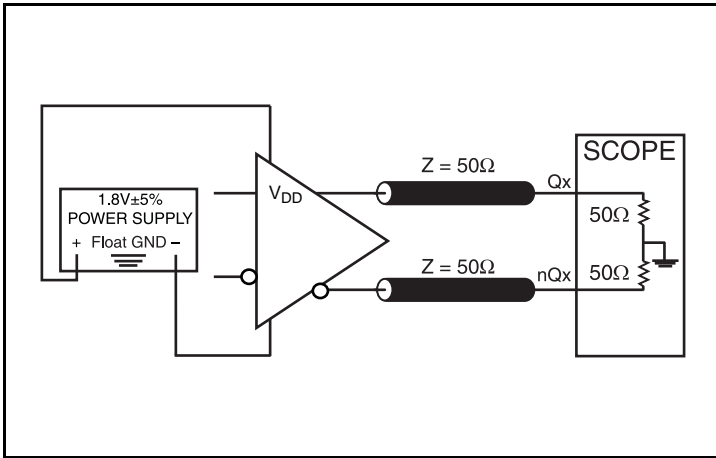
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



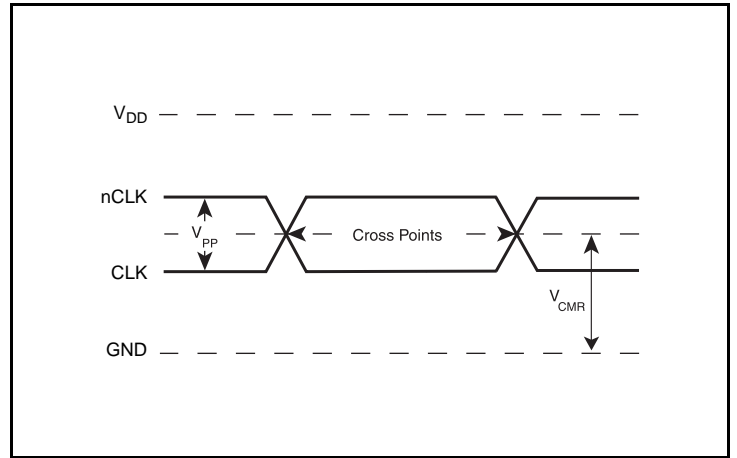
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzel Oscillator as the input source.

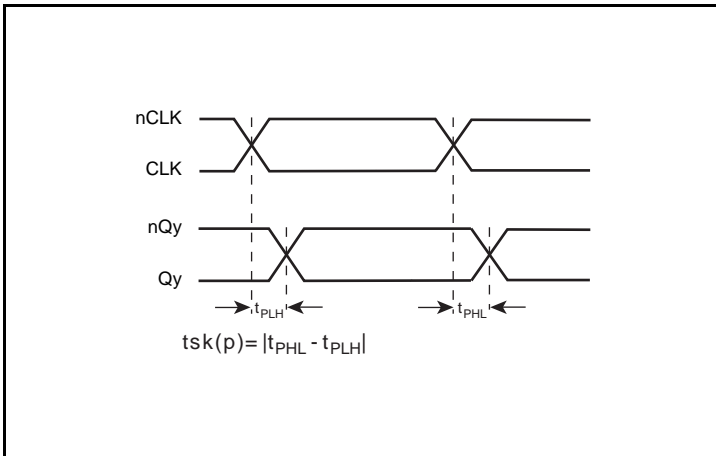
Parameter Measurement Information



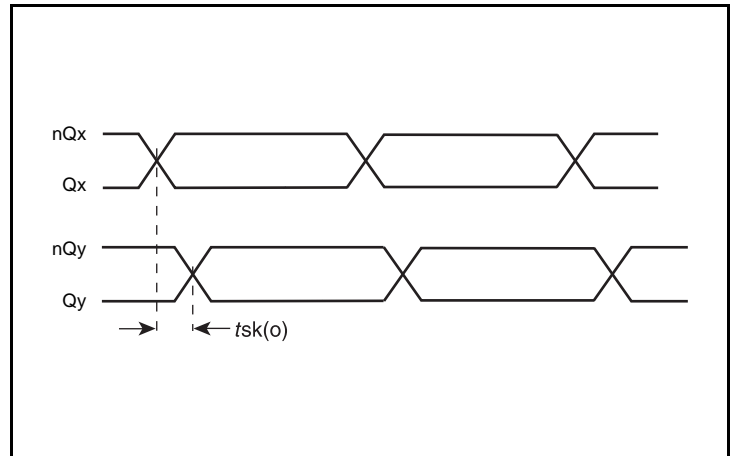
1.8V LVDS Output Load Test Circuit



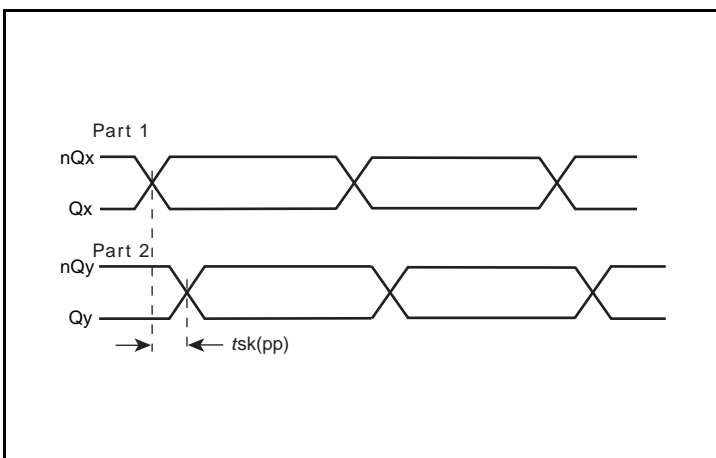
Differential Input Level



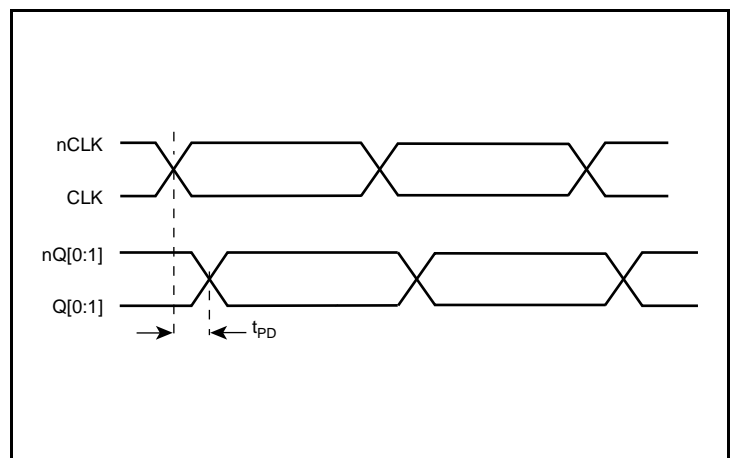
Pulse Skew



Output Skew

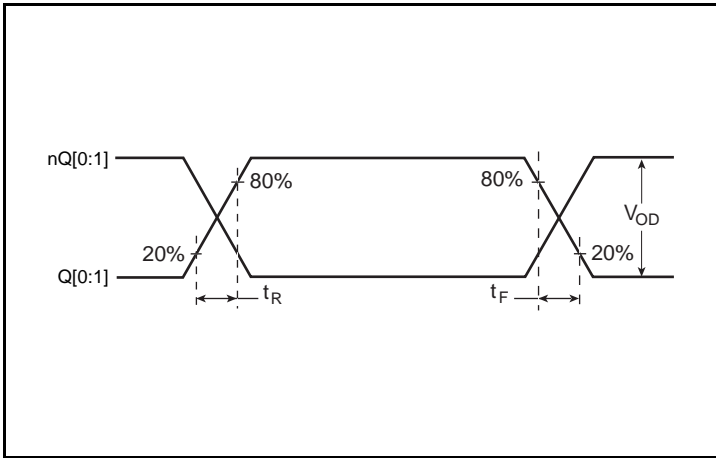


Part-to-Part Skew

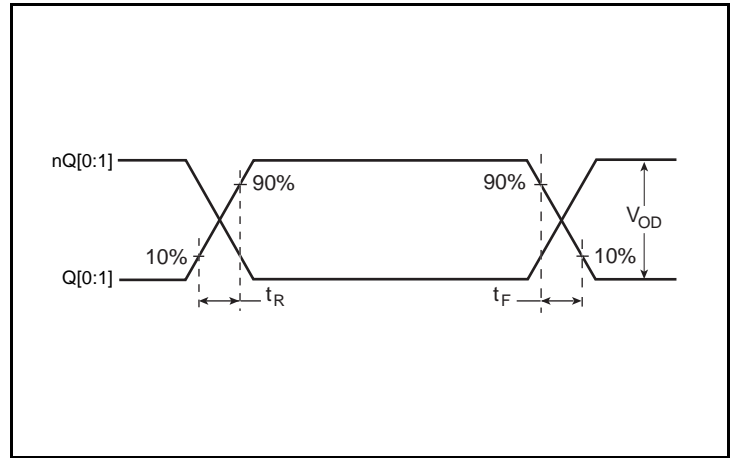


Propagation Delay

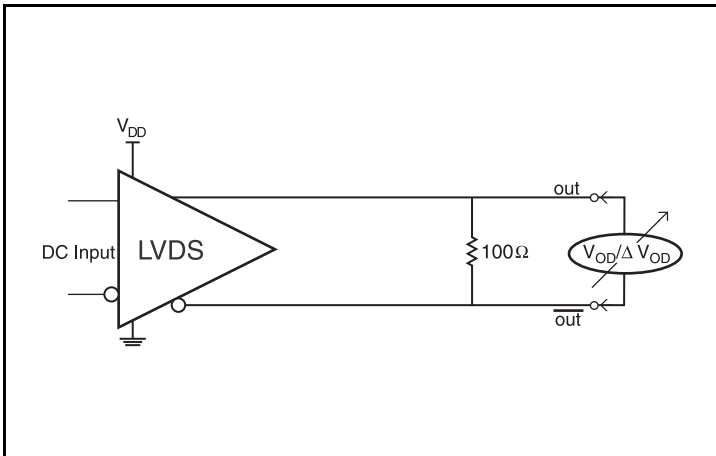
Parameter Measurement Information, continued



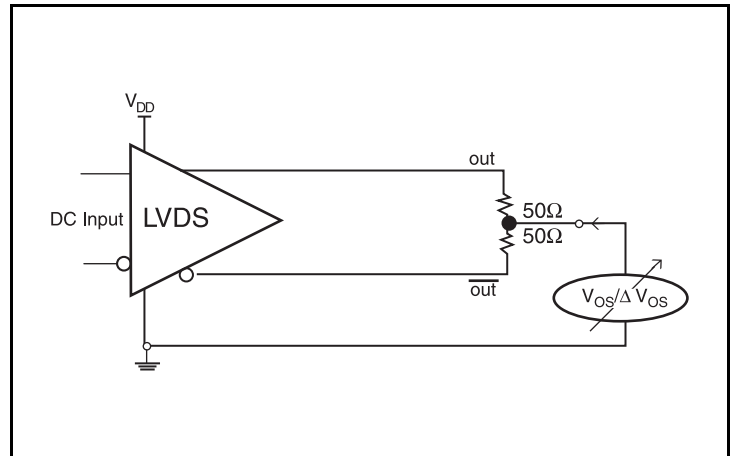
Output Rise/Fall Time, 20% – 80%



Output Rise/Fall Time, 10% – 90%



Differential Output Voltage Setup



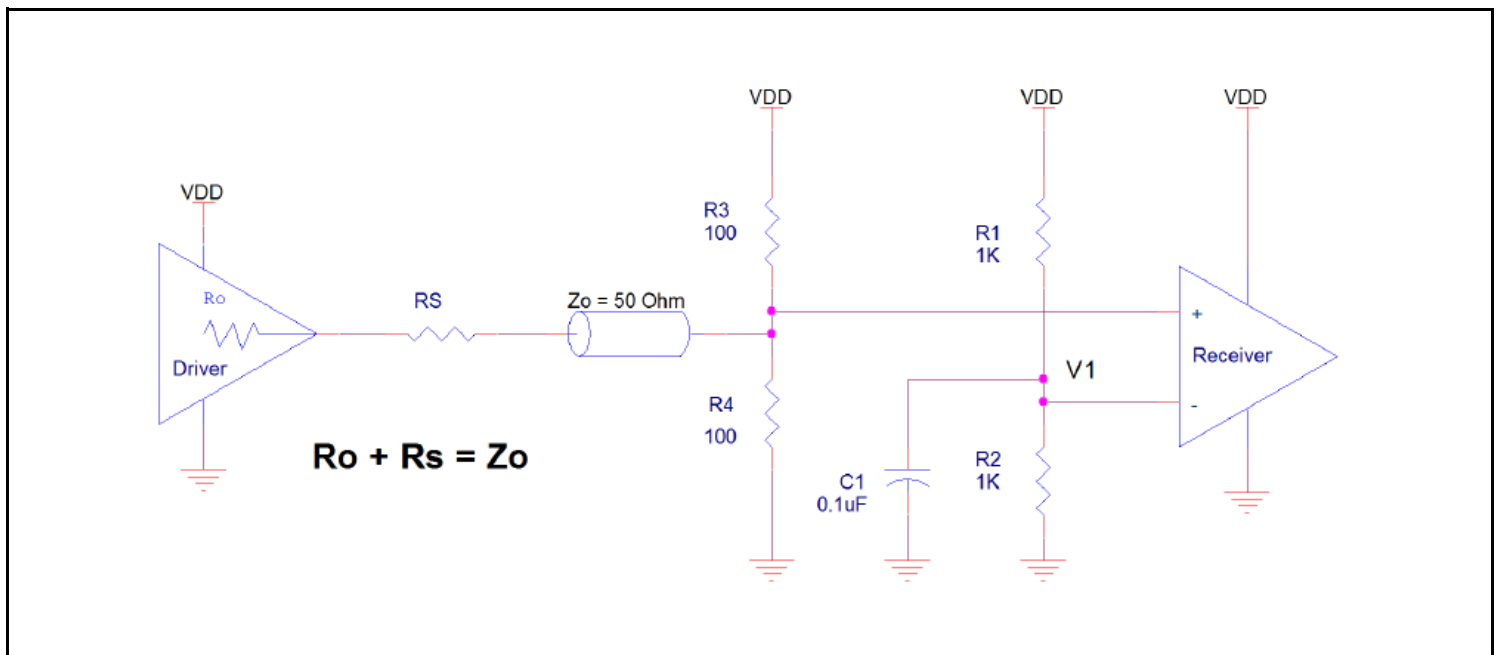
Offset Voltage Setup

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 1.8V and $V_{DD} = 1.8V$, R1 and R2 value should be adjusted to set V_1 at 0.9V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than $V_{DD} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.



Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. Figures 2A to 2D show interface examples for the CLK /nCLK input driven by the most common driver types. The input

interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



Figure 2A. Differential Input Driven by an LVDS Driver - DC Coupling

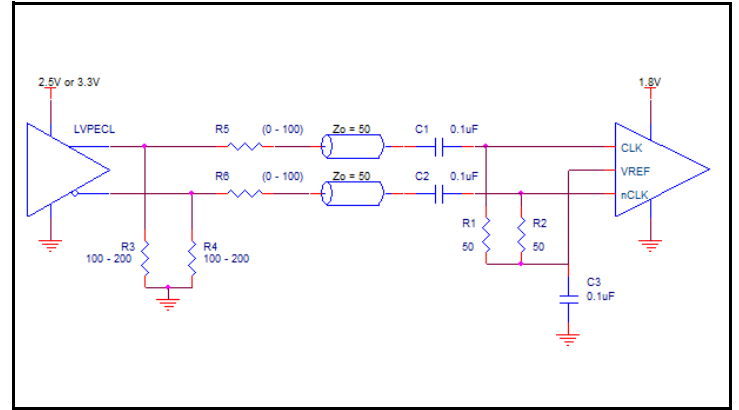


Figure 2B. Differential Input Driven by an LVPECL Driver - AC Coupling

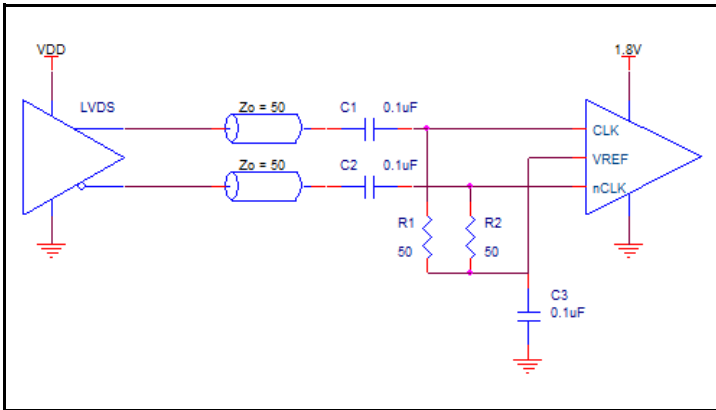


Figure 2C. Differential Input Driven by an LVDS Driver - AC Coupling

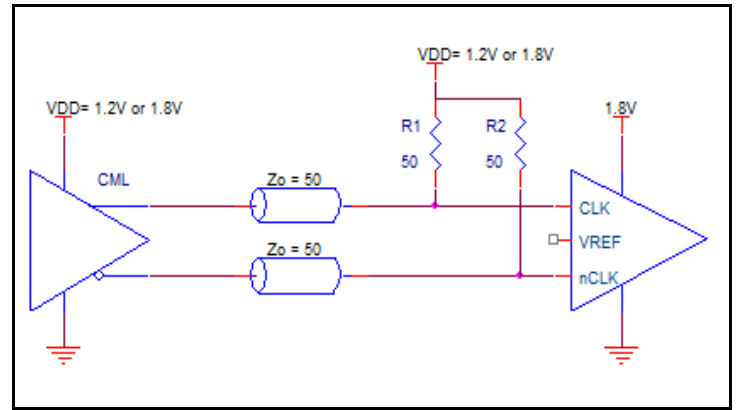


Figure 2D. Differential Input Driven by a CML Driver

Recommendations for Unused Output Pins

Outputs:

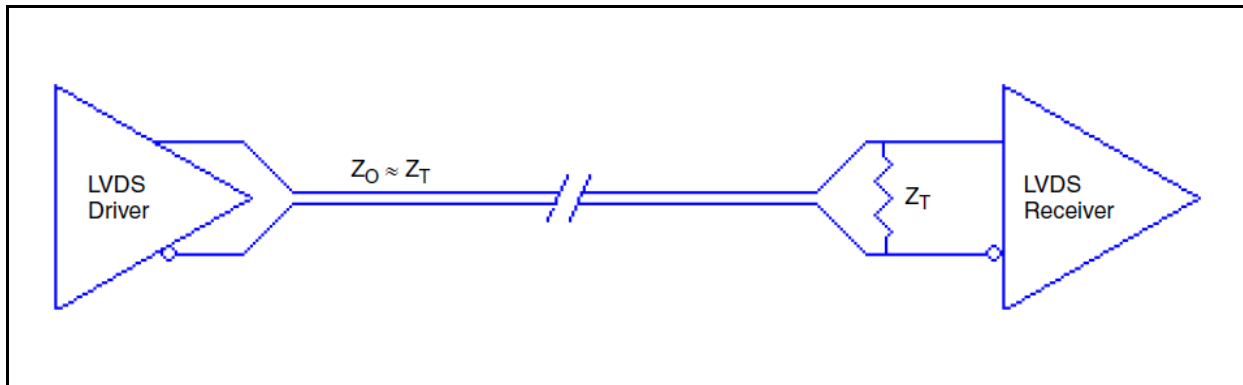
LVDS Outputs

Unused LVDS outputs must either have a 100Ω differential termination or have a 100Ω pull-up resistor to V_{DD} in order to ensure proper device operation.

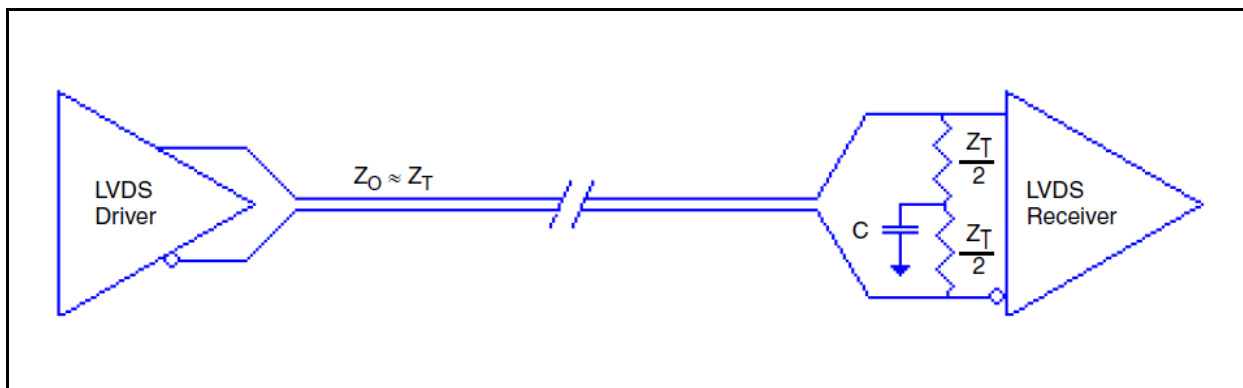
LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in the first figure can be

used with either type of output structure. The second figure, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



Standard LVDS Termination



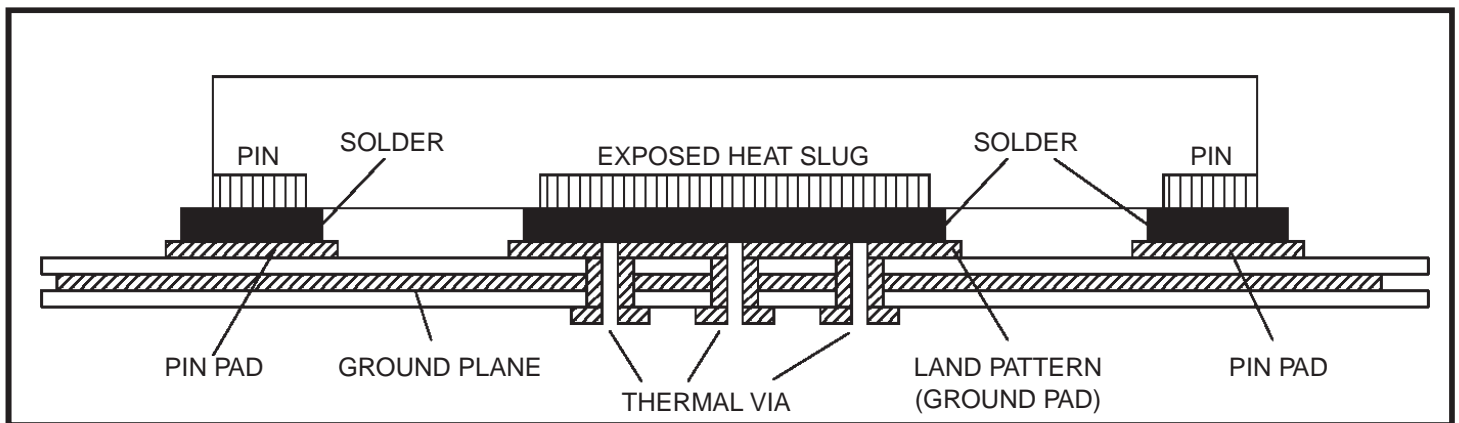
Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8P34S1102I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8P34S1102I is the sum of the core power plus the output power dissipation due to the load. The following is the power dissipation for $V_{DD} = 1.8V + 5\% = 1.89V$, which gives worst case results.

The maximum current at 85°C is as follows:

$$I_{DD_MAX} = 48mA$$

$$Power_{(core)MAX} = V_{DD_MAX} * I_{DD_MAX} = 1.89V * 48mA = \mathbf{90.72mW}$$

$$\mathbf{Total Power_MAX = 90.72mW}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 5 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.091W * 74.7^\circ C/W = 91.8^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 16-lead VFQFN

| θ_{JA} vs. Air Flow (m/s) | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W | 65.3°C/W | 58.5°C/W |

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16-lead VFQFN

| θ_{JA} vs. Air Flow (m/s) | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W | 65.3°C/W | 58.5°C/W |

Transistor Count

The transistor count for the IDT8P34S1102I is: 935

Package Outline Drawings

The package outline drawings are located in the last section of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 7. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------|---------------------------|--------------------|---------------|
| 8P34S1102NLGI | S102I | "Lead-Free" 16-lead VFQFN | Tube | -40°C to 85°C |
| 8P34S1102NLGI8 | S102I | "Lead-Free" 16-lead VFQFN | Tape & Reel | -40°C to 85°C |

Revision History

| Revision Date | Description of Change |
|--------------------|--|
| September 20, 2017 | Updated the package outline drawings; however, no mechanical changes Completed other minor improvements |
| February 26, 2014 | Ordering Info: Changed Tray to Tube. |



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

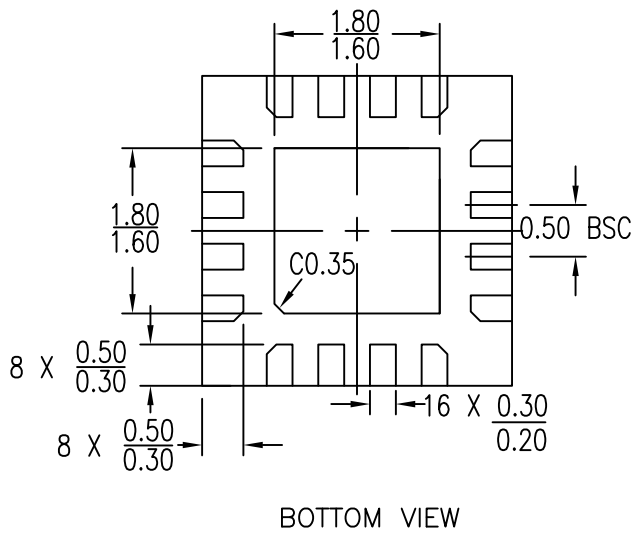
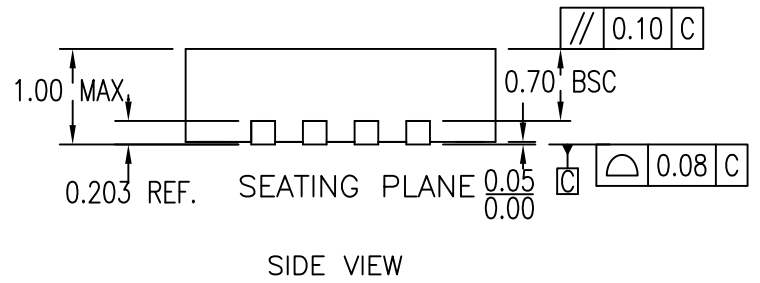
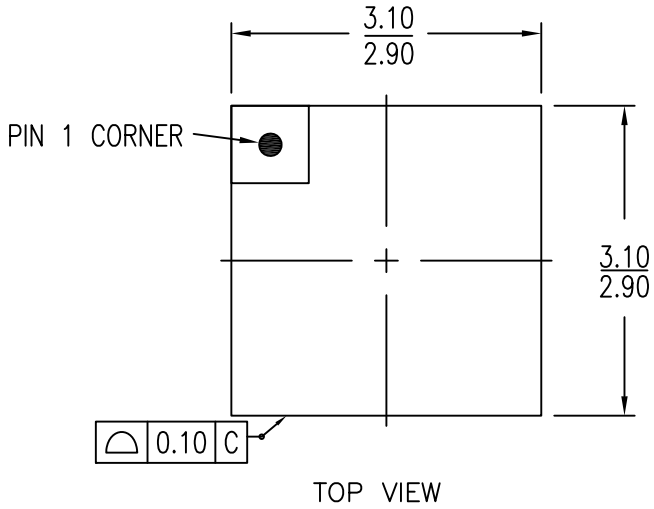
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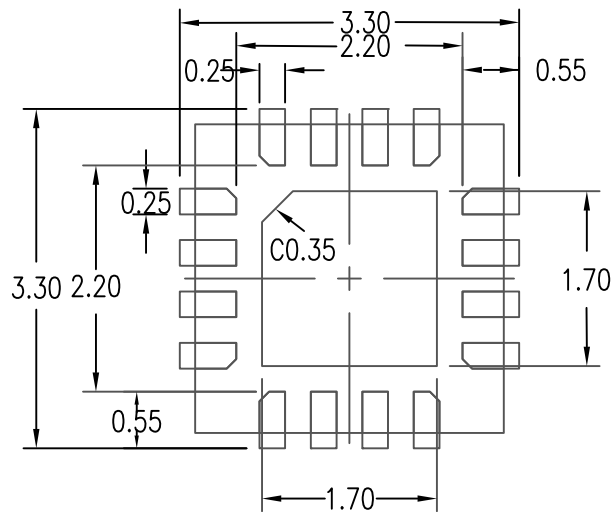
16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad
 NL/NLG16P2, PSC-4169-02, Rev 03, Page 1



NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES



RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES
2. TOP DOWN VIEW—AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

| Package Revision History | | |
|--------------------------|---------|-------------------|
| Date Created | Rev No. | Description |
| Aug 15, 2017 | Rev 03 | Update Epad Range |
| Jul 28, 2017 | Rev 02 | New format |



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.