

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT HC563 INVERTING - HC573 NON INVERTING

- HIGH SPEED
 $t_{PD} = 13 \text{ ns (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) AT } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $I_{OL} = |I_{OH}| = 6 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS563/573

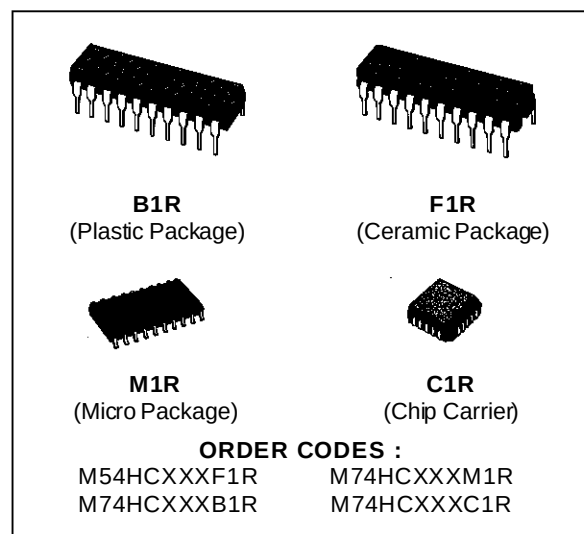
DESCRIPTION

The M54/74HC563 and M54HC573 are high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2 MOS technology.

These ICs archive the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8 bit D-Type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level



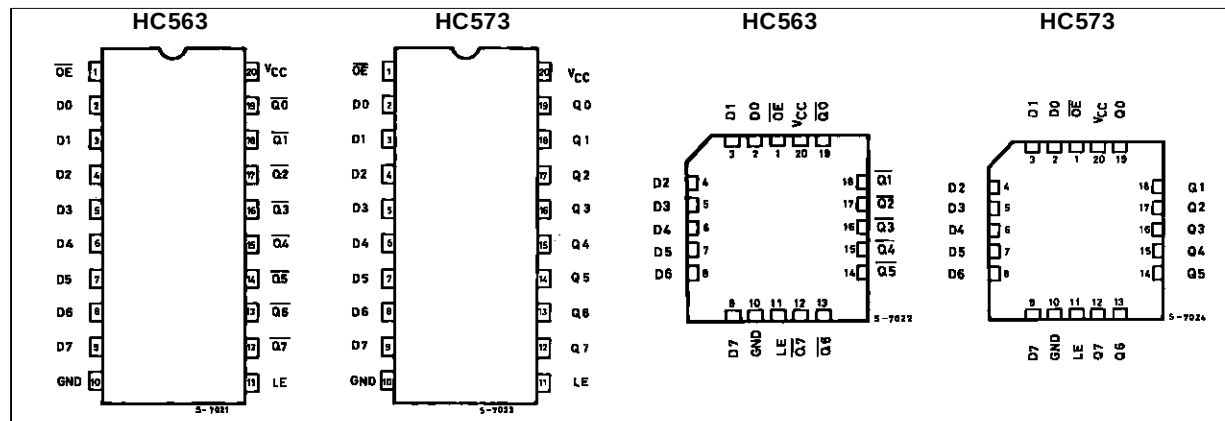
of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The application designer has a choice of combination of inverting and non inverting outputs.

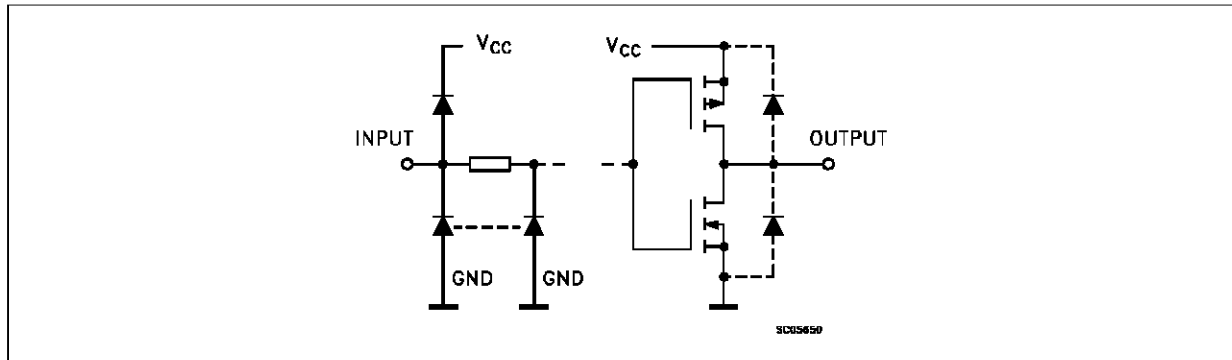
The three state output configuration and the wide choice of outline make bus organized system simple.

All inputs are equipped with protection circuits against discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



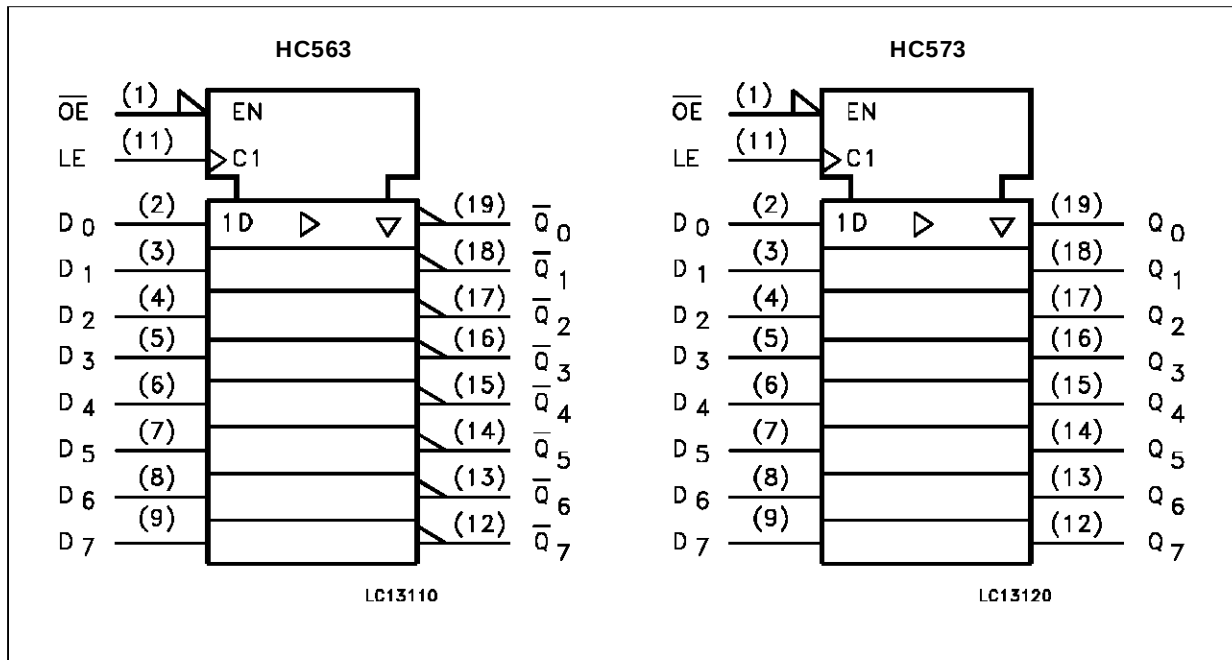
PIN DESCRIPTION (HC563)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC573)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

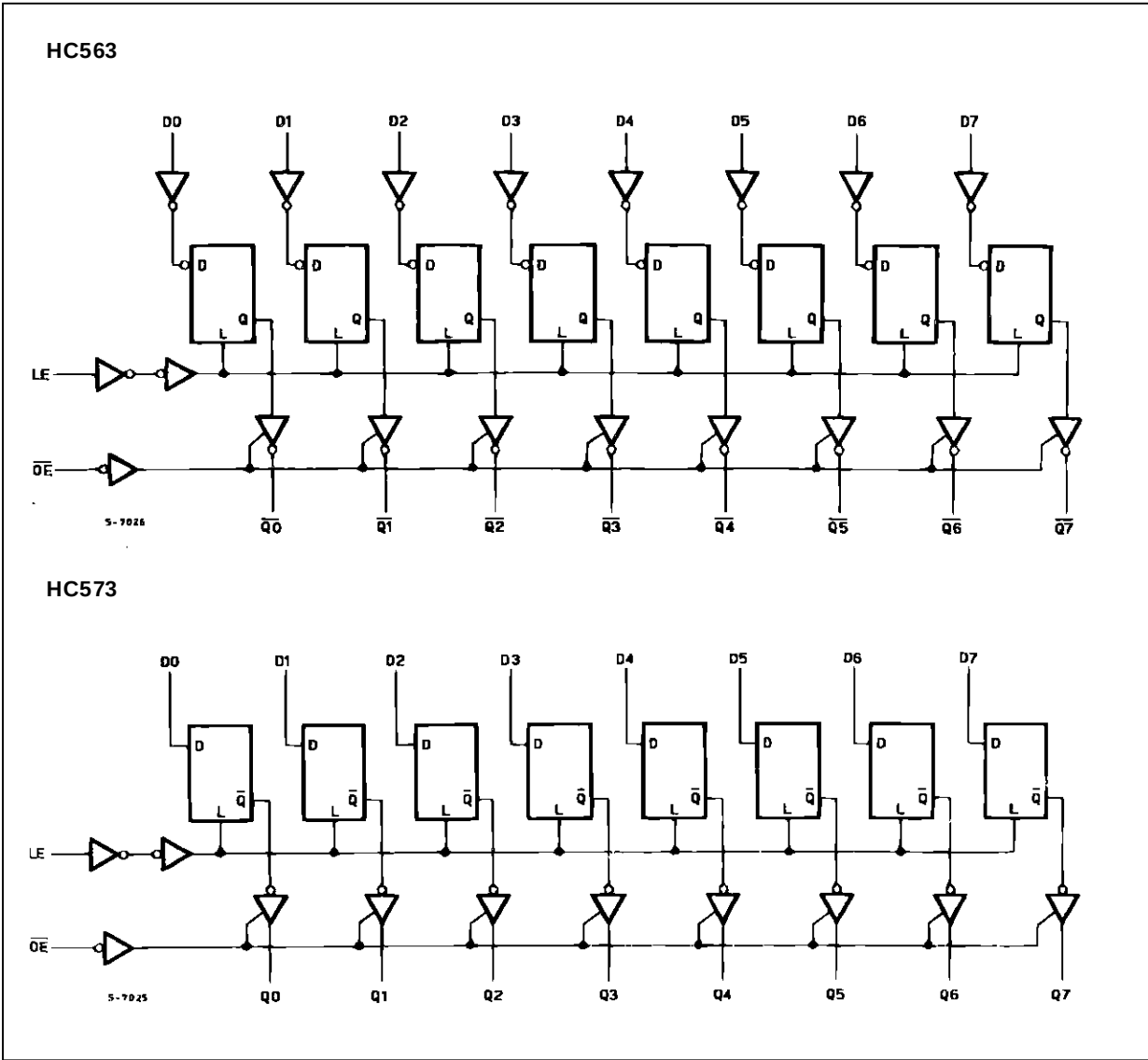


TRUTH TABLE

INPUTS			OUTPUTS	
OE	LE	D	Q (HC573)	$\bar{Q}$ (HC563)
H	X	X	Z	Z
L	L	X	NO CHANGE *	NO CHANGE *
L	H	L	L	H
L	H	H	H	L

X: DON'T CARE
 Z: HIGH IMPEDANCE
 *: Q/Q OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(*) 500 mW: $\equiv 65^\circ\text{C}$ derate to 300 mW by 10mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6\text{ V}$	0 to 1000 0 to 500 0 to 400
			ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value						Unit		
		V _{CC} (V)			T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V	
		4.5			3.15			3.15		3.15			
		6.0			4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V	
		4.5					1.35		1.35		1.35		
		6.0					1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O =-20 μA	1.9	2.0		1.9		1.9		V	
		4.5			4.4	4.5		4.4		4.4			
		6.0			5.9	6.0		5.9		5.9			
		4.5		I _O =-6.0 mA		4.18	4.31		4.13		4.10		
		6.0		I _O =-7.8 mA		5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V	
		4.5				0.0	0.1		0.1		0.1		
		6.0				0.0	0.1		0.1		0.1		
		4.5		I _O = 6.0 mA			0.17	0.26		0.33			0.40
		6.0		I _O = 7.8 mA			0.18	0.26		0.33			0.40
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND				±0.1		±1		±1	μA	
I _{OZ}	3 State Output Off State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND				±0.5		±5.0		±10	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND				4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

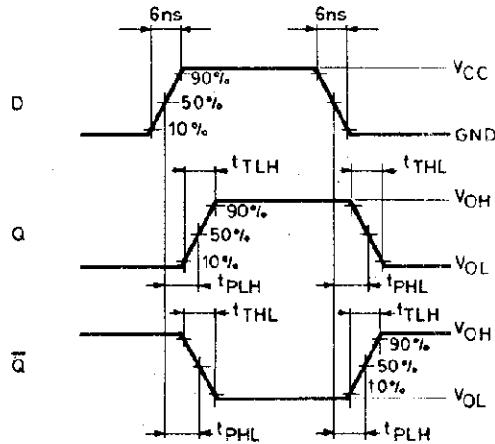
Symbol	Parameter	Test Conditions			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t _{PLH} t _{PHL}	Propagation Delay Time (LE - Q, Q̅)	2.0	50			50	115		145		175	ns
		4.5				15	23		29		35	
		6.0				13	20		25		30	
		2.0	150			60	155		195		235	ns
		4.5				20	31		39		47	
		6.0				17	26		33		40	
t _{PLH} t _{PHL}	Propagation Delay Time (D - Q, Q)	2.0	50			42	110		140		165	ns
		4.5				14	22		28		33	
		6.0				12	19		24		28	
		2.0	150			57	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
t _{PZL} t _{PZH}	3 State Output Enable Time	2.0	50	R _L = 1 KΩ		55	140		175		210	ns
		4.5				17	28		35		42	
		6.0				14	24		30		36	
		2.0	150	R _L = 1 KΩ		66	180		225		270	ns
		4.5				22	36		45		54	
		6.0				19	31		38		46	
t _{PLZ} t _{PHZ}	3 State Output Disable Time	2.0	50	R _L = 1 KΩ		40	125		155		190	ns
		4.5				17	25		31		38	
		6.0				15	21		26		32	
t _{W(L)} t _{W(H)}	Minimum Pulse Width	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t _s	Minimum Set-up Time	2.0	50			16	50		65		75	ns
		4.5				5	10		13		15	
		6.0				3	9		11		13	
t _h	Minimum Hold Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C _{IN}	Input Capacitance					5	10		10		10	pF
C _{OUT}	Output Capacitance					10						pF
C _{PD} (*)	Power Dissipation Capacitance			for HC563 for HC573		49 51						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate)

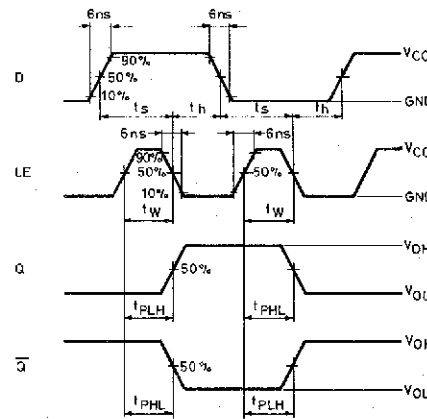
The CPD when n pcs of FLIP-FLOP operate, can be gained by following equations:

for HC563 CPD (TOTAL) = $33 + 16 \times n$ [pF]; for HC573 CPD (TOTAL) = $33 + 18 \times n$ [pF]

SWITCHING CHARACTERISTICS TEST WAVEFORM

 t_{PLH} , t_{PHL} , (D - Q, $\bar{Q}$)

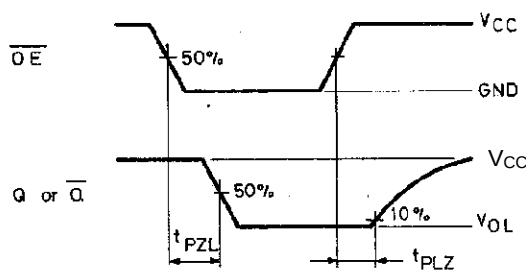
S-10427/A

 t_{PLH} , t_{PHL} , (LE - Q, $\bar{Q}$) t_s , t_h , t_w 

S-10428

 t_{PLZ} , t_{PZL}

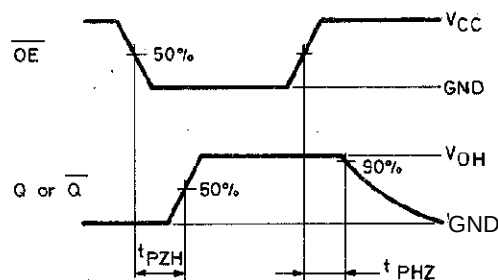
The 1K Ω load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.



S-10429

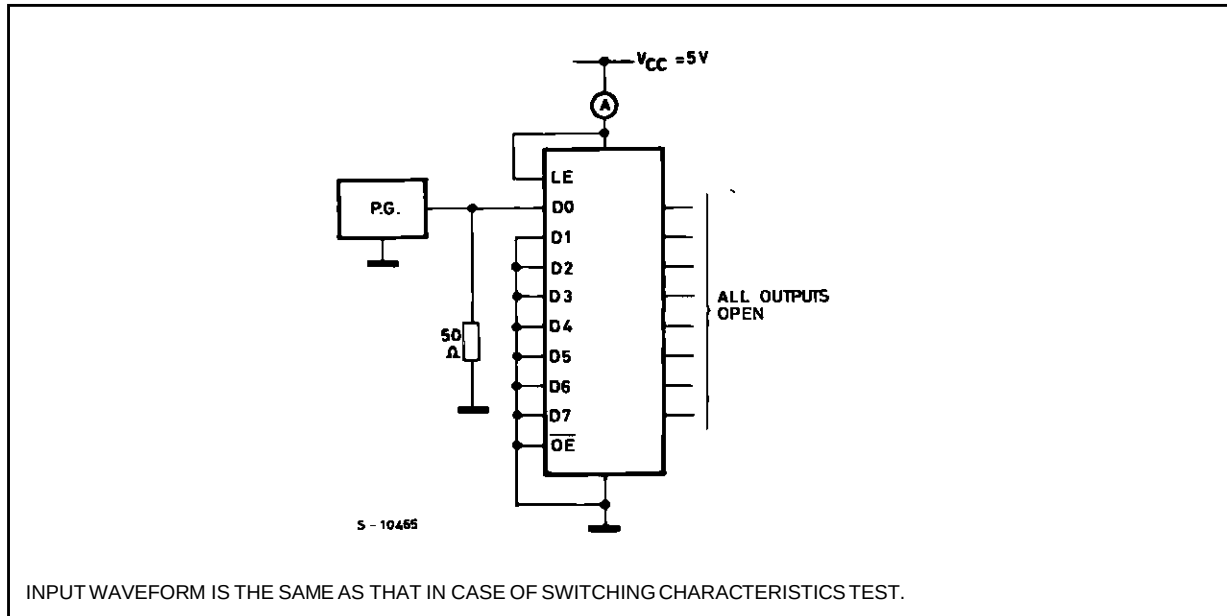
 t_{PHZ} , t_{PZH}

The 1K Ω load resistors and the 50pF load capacitors should be connected between each output and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.



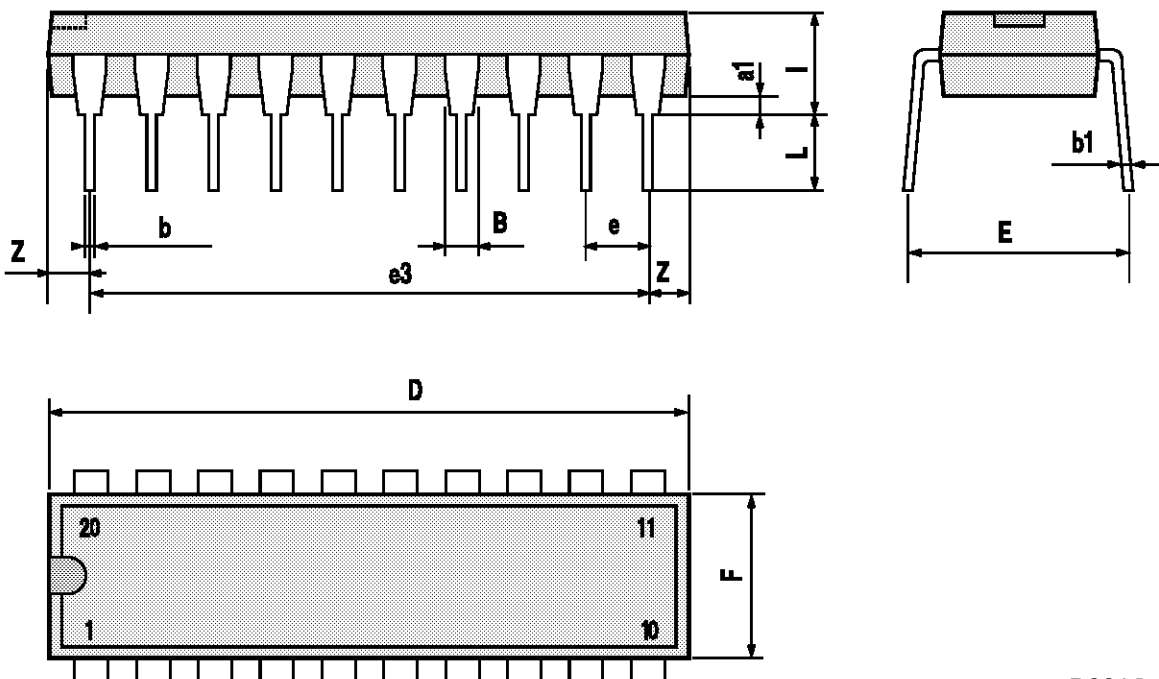
S-10430

TEST CIRCUIT I_{CC} (Opr.)



Plastic DIP20 (0.25) MECHANICAL DATA

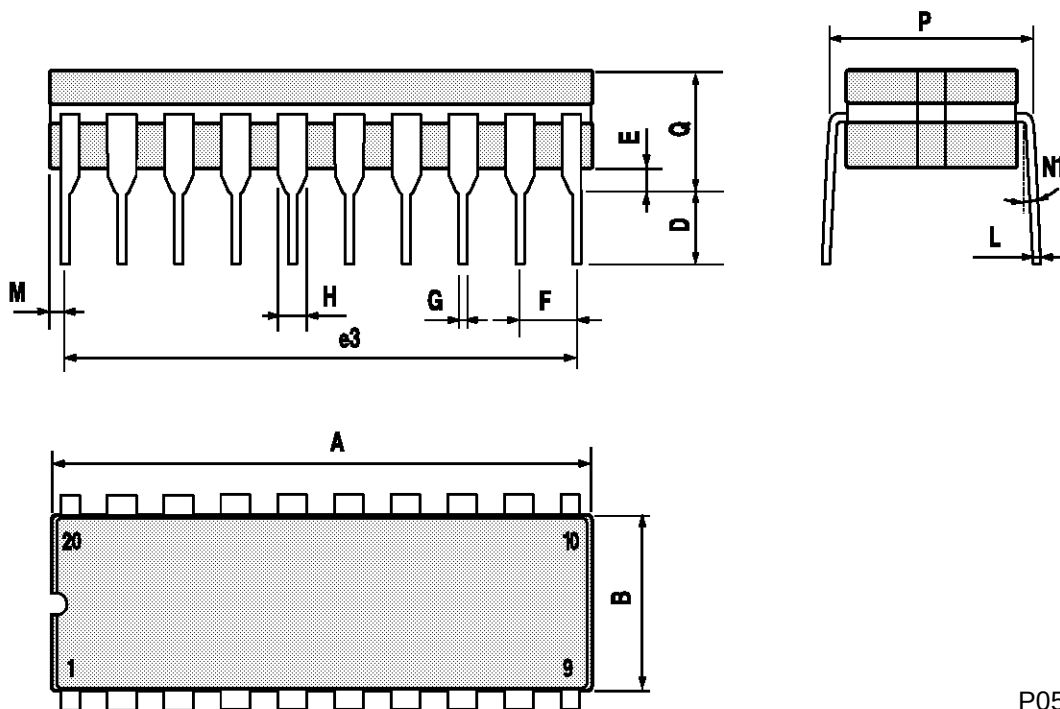
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

Ceramic DIP20 MECHANICAL DATA

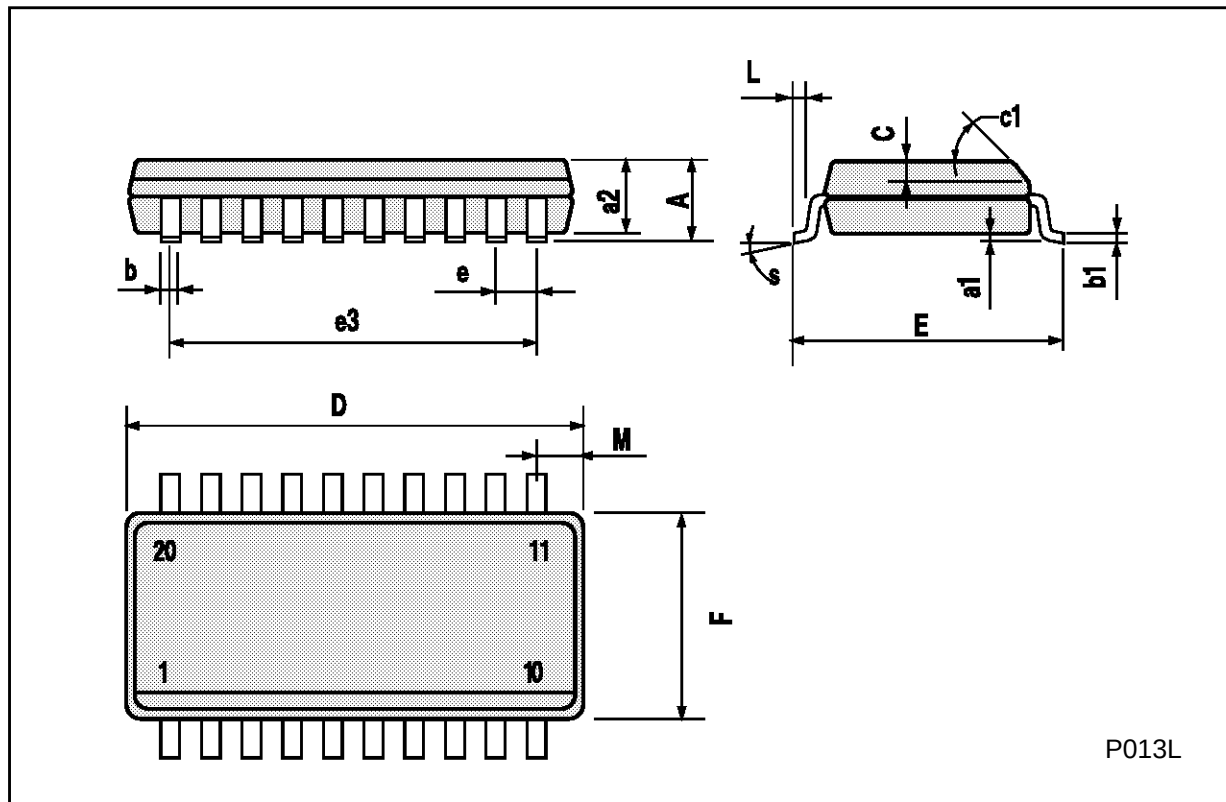
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225



P057H

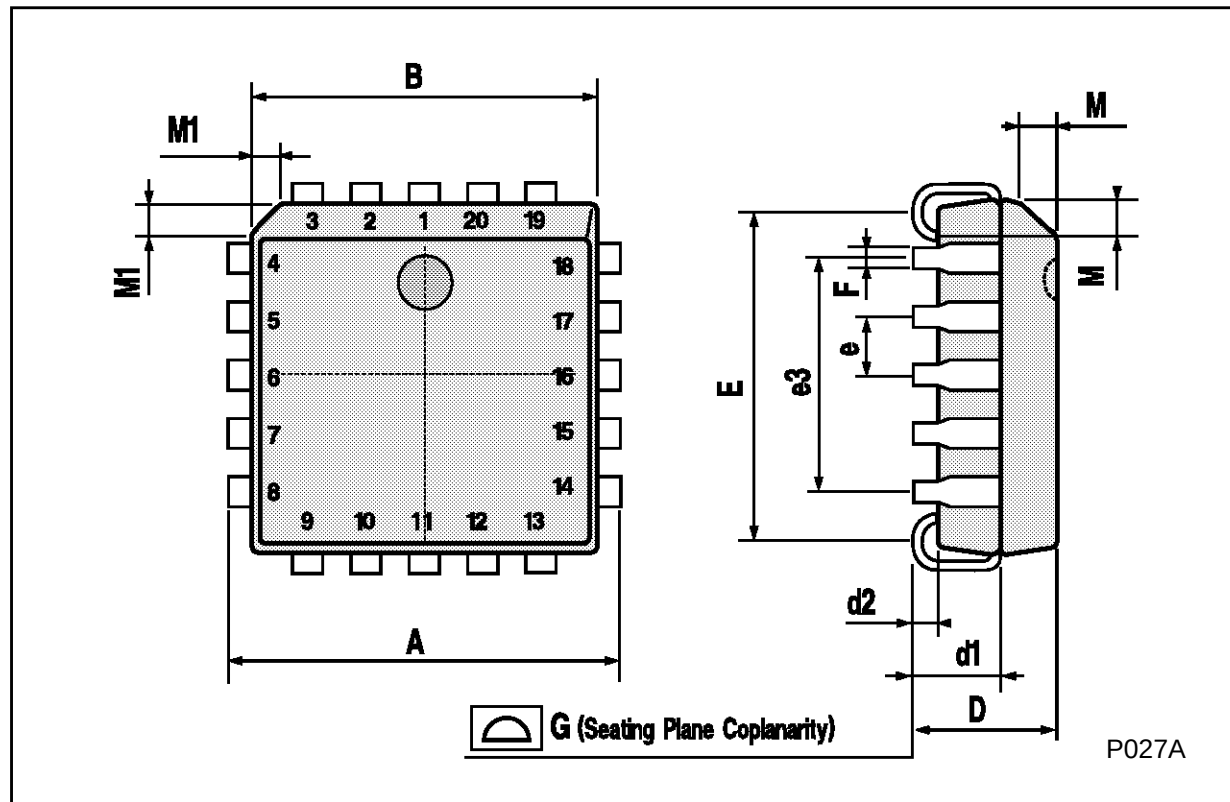
SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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- Техническая поддержка проекта;
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