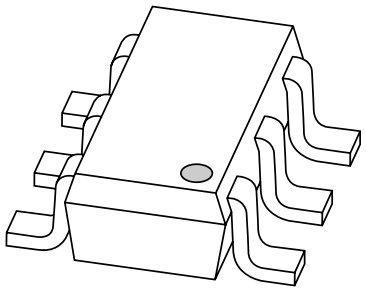
DATA SHEET



BZA408B
Quadruple bidirectional ESD transient voltage suppressor

Product data sheet
Supersedes data of 1998 Jun 05

1998 Oct 15

Quadruple bidirectional ESD transient voltage suppressor

BZA408B

FEATURES

- ESD rating >15 kV, according to IEC1000-4-2
- SOT457 surface mount package
- Non-clamping range: –5 V to +5 V
- Channel separation: >70 dB
- Low reverse current: <100 nA
- Low diode capacitance: <75 pF.

APPLICATIONS

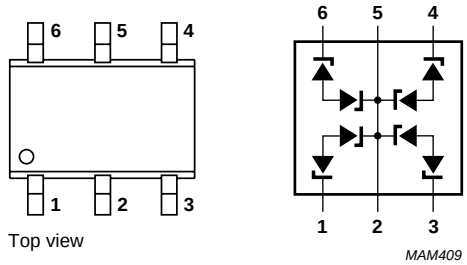
- Protection of equipment, connected to data and transmission lines, against voltage surges caused by electrostatic discharge e.g:
  - Computers and peripherals
  - Audio and video equipment
  - Communication systems
  - Medical equipment
  - Portable electronics.

DESCRIPTION

4-bit wide monolithic bidirectional ESD transient voltage suppressor in a six lead SOT457 (SC-74) package.

PINNING

PIN	DESCRIPTION
1	cathode 1
2, 5	ground
3	cathode 2
4	cathode 3
6	cathode 4



Marking code: Z8.

Fig.1 Simplified outline (SOT457) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode (pin 2 and / or 5 connected to ground)					
I_{ZSM}	non-repetitive peak reverse current	t_p = 1 ms; square pulse; see Fig.2	–	2	A
P_{ZSM}	non-repetitive peak power	t_p = 1 ms; square pulse	–	20	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	one or more diodes loaded	340	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode (pin 2 and / or 5 connected to ground)					
V_{RWM}	working reverse voltage		–	5	V
V_R	reverse voltage	I_{test} = 5 mA	5.5	–	V
V_{ZSM}	non-repetitive peak reverse voltage	t_p = 1 ms; I_{ZSM} = 2 A	–	10	V
I_R	reverse current	$V_R = V_{RWM}$	–	100	nA
C_d	diode capacitance	see Fig.3			
		V_R = 0; f = 1 MHz	–	75	pF
		V_R = 5 V; f = 1 MHz	–	55	pF
$\alpha_{ch\ (p\ to\ p)}$	pin to pin channel separation	note 1; see Fig.4	70	–	dB

Note

1. $\alpha_{ch\ (p\ to\ p)}$ is measured as follows: a −7 dBs sinewave of 400 Hz is connected to e.g. pin 6 and a −7 dBs sinewave of 1 kHz to pin 1. The 1 kHz signal of pin 1 is measured on pin 6 by means of a spectrum analyser with an input impedance of 1 MΩ. So $\alpha_{ch\ (p\ to\ p)}$ equals the 1 kHz level on pin 1 minus the 1 kHz level on pin 6. For the 400 Hz signal the same measurement is done in the opposite way.

GRAPHICAL DATA

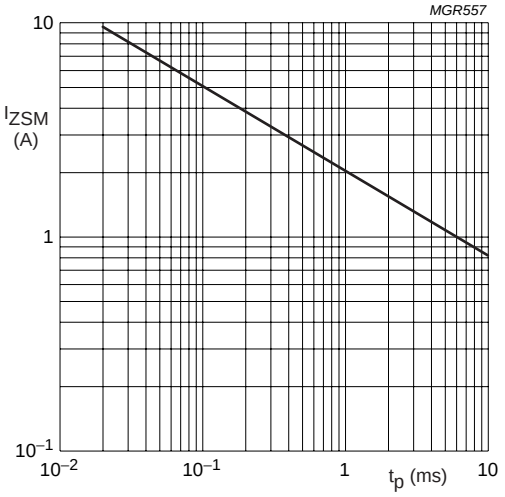
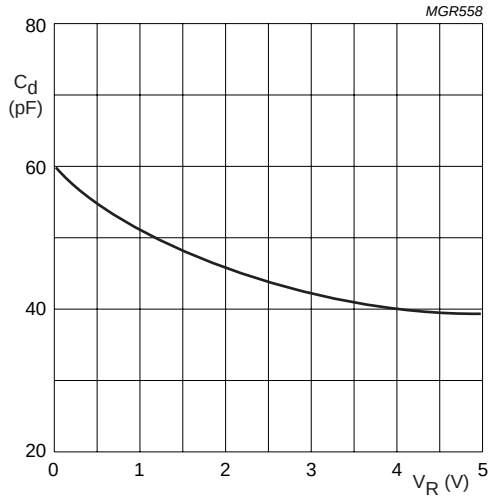


Fig.2 Maximum non-repetitive peak reverse current as a function of pulse time.



T_j = 25 °C; f = 1 MHz.

Fig.3 Diode capacitance as a function of reverse voltage; typical values.

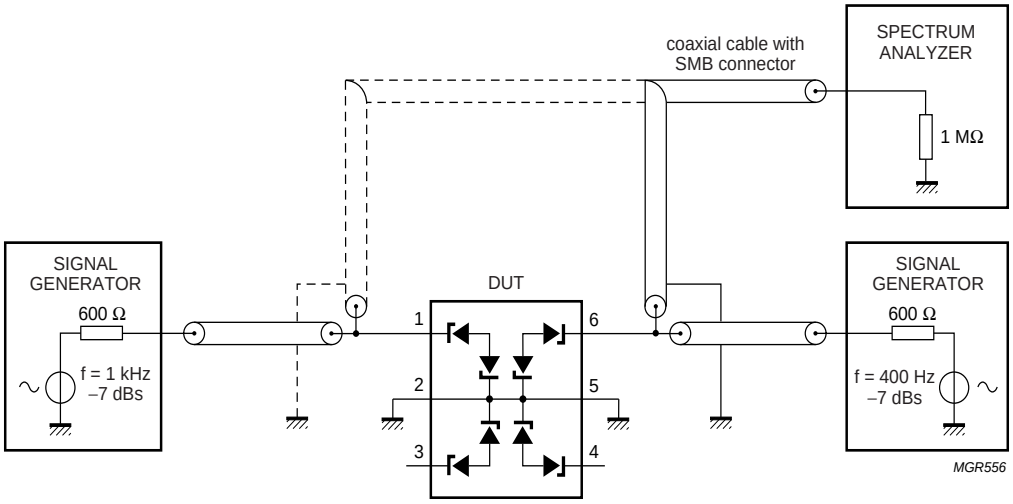
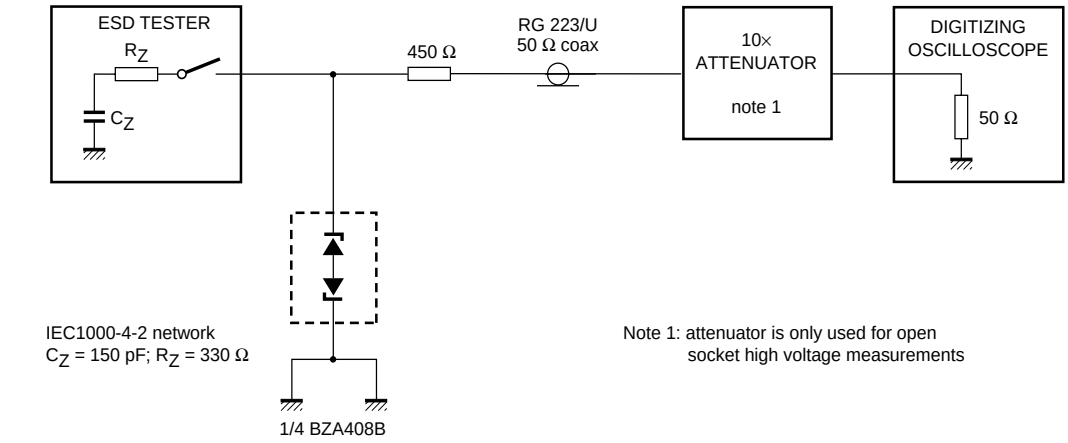
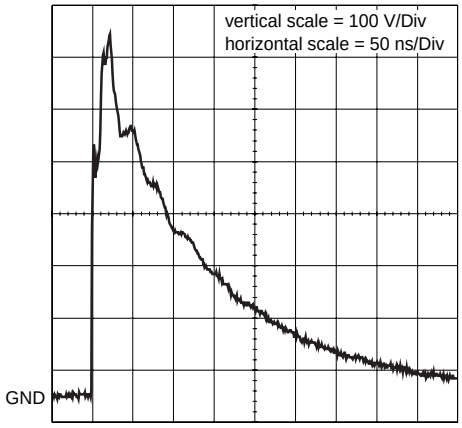


Fig.4 Channel separation measurement setup.

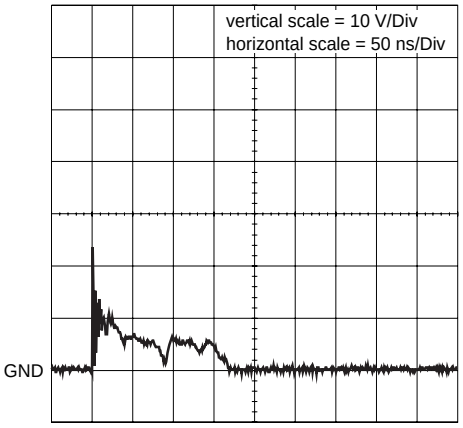


IEC1000-4-2 network
C_Z = 150 pF; R_Z = 330 Ω

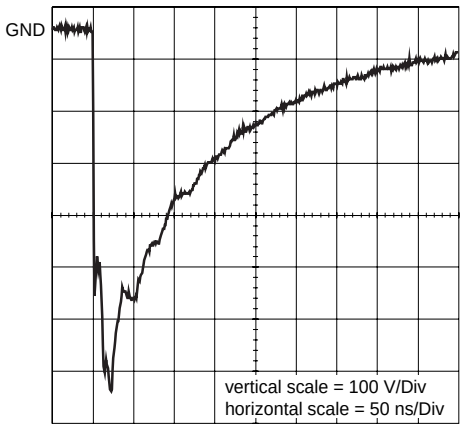
Note 1: attenuator is only used for open socket high voltage measurements



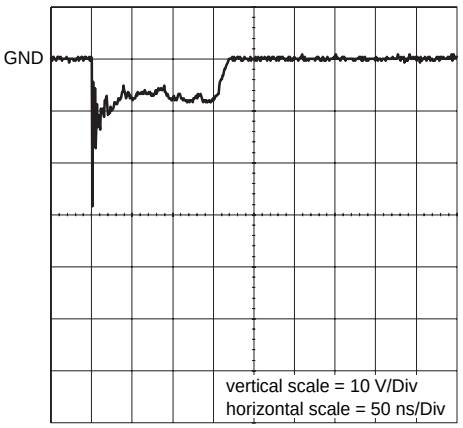
unclamped +1 kV ESD voltage waveform (IEC1000-4-2 network)



clamped +1 kV ESD voltage waveform (IEC1000-4-2 network)



unclamped –1 kV ESD voltage waveform (IEC1000-4-2 network)



clamped –1 kV ESD voltage waveform (IEC1000-4-2 network)

MGR560

Fig.5 ESD clamping test set-up and waveforms.

APPLICATION INFORMATION

Typical bidirectional application

A quadruple bidirectional transient suppressor in a SOT457 package makes it possible to protect four separate lines using only one package. One simplified example is shown in Fig.6.

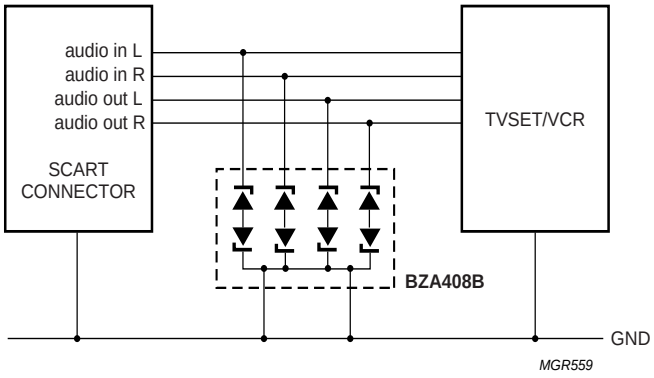


Fig.6 Scart connector protection.

Device placement and printed-circuit board layout

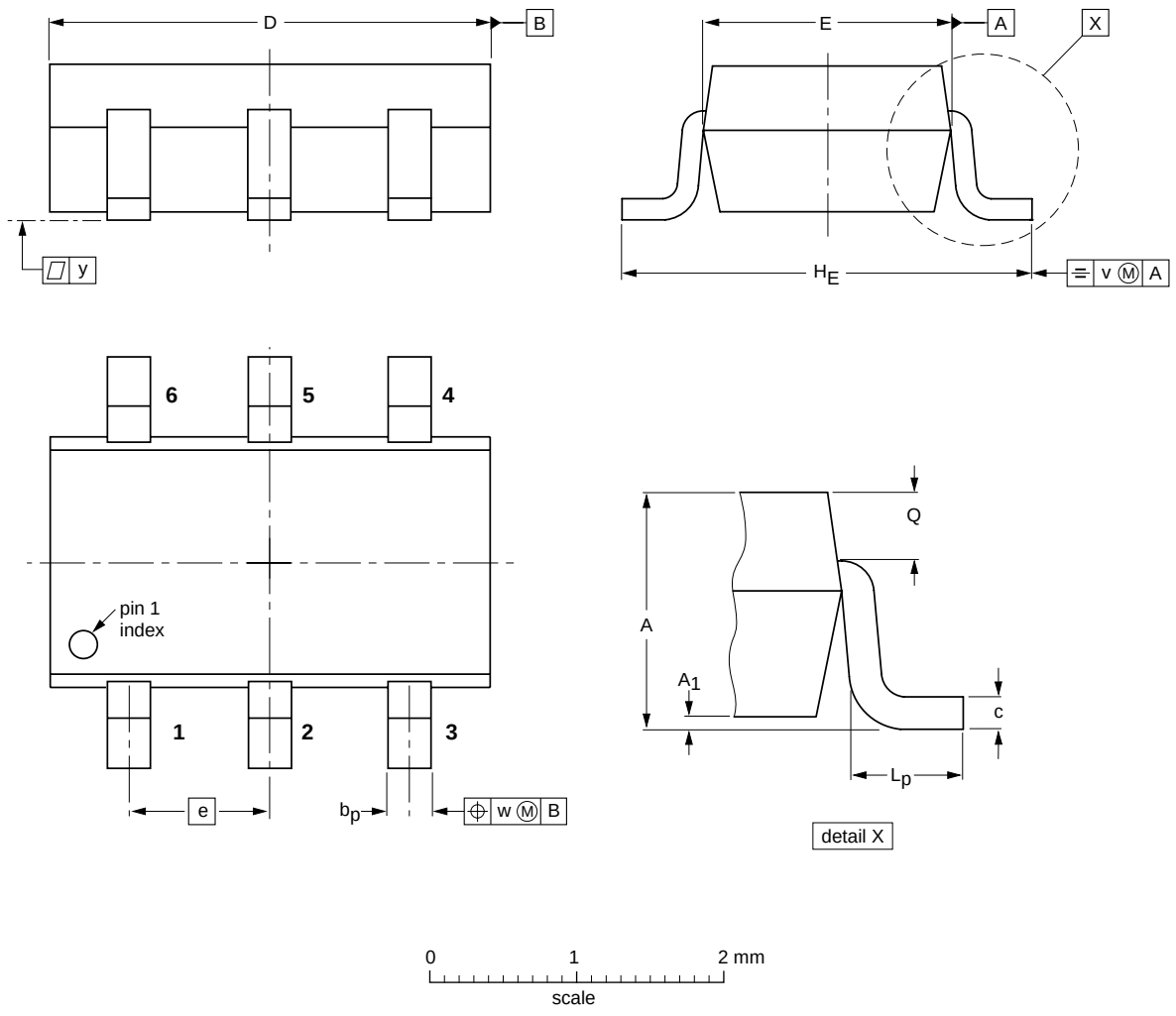
Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA408B is determined by the peak transient current and the rate of rise of that current (di/dt). Since parasitic inductances can further add to the clamping voltage (V = L di/dt) the series conductor lengths on the printed-circuit board should be kept to a minimum. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element close to the input terminals or connectors.
2. Keep parallel signal paths to a minimum.
3. Avoid running protection conductors in parallel with unprotected conductors.
4. Minimize all printed-circuit board loop areas including power and ground loops.
5. Minimize the length of the transient return path to ground.
6. Avoid using shared transient return paths to a common ground point.

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			~~97-02-28~~ 01-05-04

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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Customer notification

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Contact information

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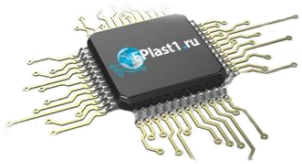

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