

6V to 20V, 1A 1ch PWM Buck Converter Integrated FET

BD9227F

General Description

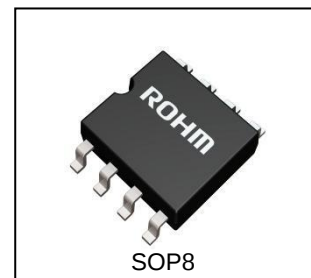
The BD9227F is a 20V, 1A non-synchronous PWM duty control buck converter with integrated internal high-side 20V Power MOSFET. Operating frequency is 1.0MHz fixed by inner circuit. Current mode control with internal slope compensation simplifies the external compensation calculation and reduces component count while allowing the use of ceramic output capacitors. Additional protection features are included such as Over Current Protection, Thermal Shutdown and Under Voltage Lockout. The BD9227F is available in SOP8.

Key Specifications

- Input Voltage Range: 6V to 20 V
- Ref. Precision: PWM=H: $\pm 2.0\%$ ($\pm 1.0\%$ @ $T_a = 25^\circ\text{C}$)
- Max Output Current: 1A (Max.)
- Switching Frequency: 1.0MHz (Typ.)
- Operating Temperature Range: -40°C to $+85^\circ\text{C}$

Packages
SOP8

W(Typ) x D(Typ) x H(Max)
5.00mm x 6.20mm x 1.71mm



Features

- Wide Operating Input Range 6V to 20V
- 20V/200mΩ Internal Power MOSFET
- 1.0MHz Fixed Operating Frequency
- Current Mode
- Over Current Hiccup Period Protection
- Under Voltage Locked Out(UVLO), Over Voltage Protection(OVP), Thermal Shut Down(TSD)
- Available in SOP8 Package.

Applications

- Home Appliance
- VM Motor

Typical Application Circuits

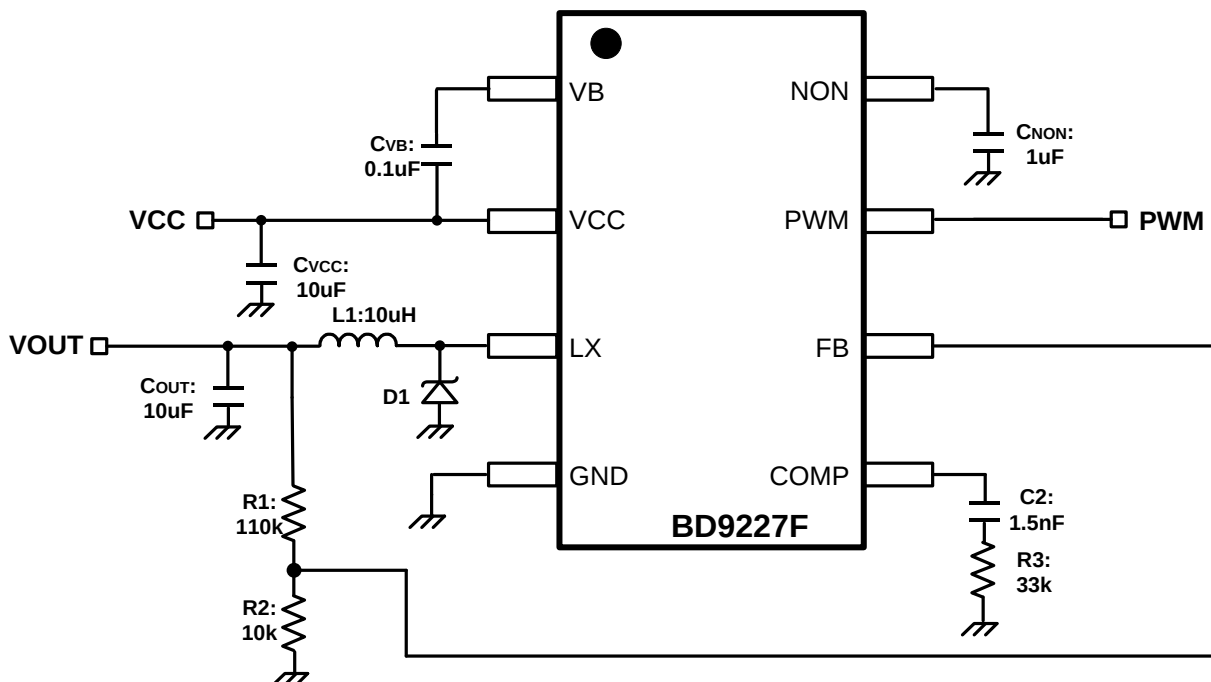


Figure 1. Typical Application Circuit

Pin Configuration

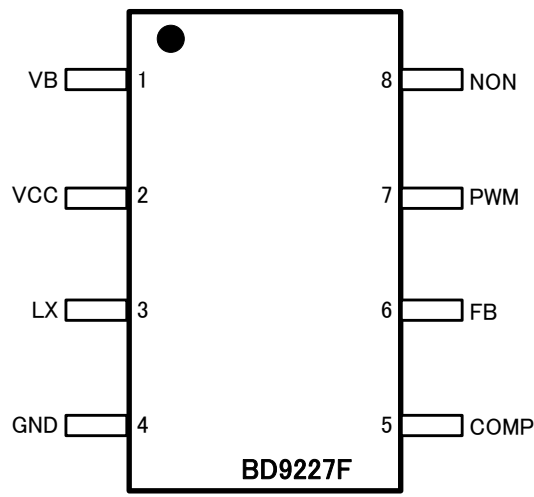


Figure 2. Pin Configuration (TOP VIEW)

Pin Description

Pin No.	Pin Name	Function
1	VB	Inner voltage regulator output power supply
2	VCC	Power supply
3	LX	Switch pin of PWM buck
4	GND	Ground
5	COMP	Compensation node
6	FB	Feedback signal
7	PWM	PWM input signal
8	NON	Inner DC ref voltage

Block Diagram

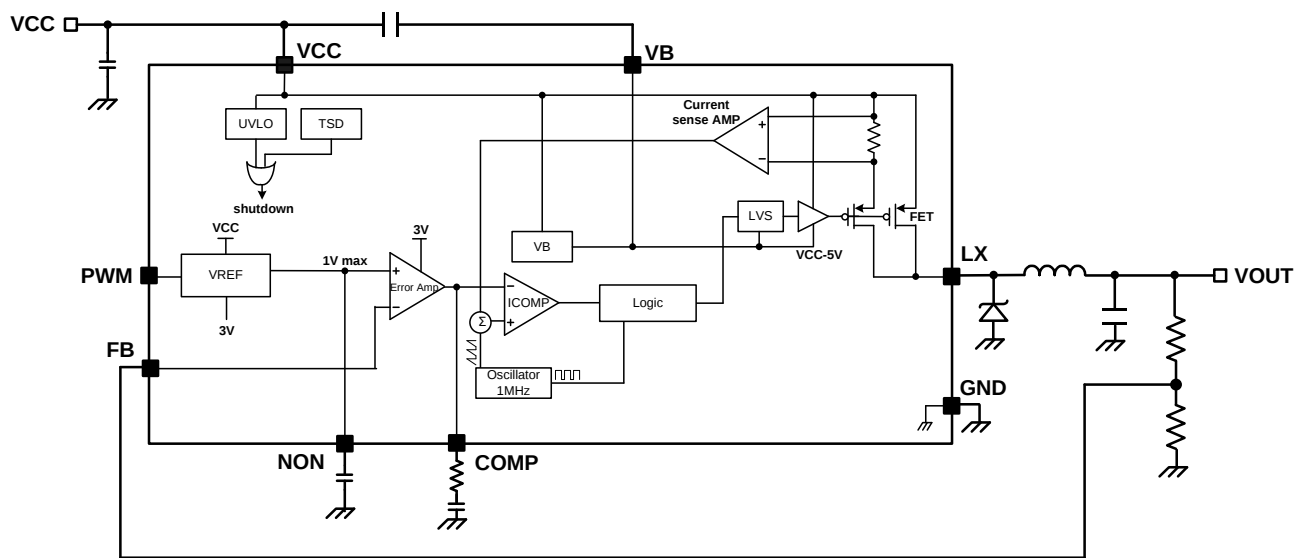


Figure 3. Block Diagram

Description of Blocks

1. VREF
This block generates reference voltage and current. It starts operation when VCC rise up. It provides reference voltage and current to Error AMP, Oscillator, and etc.
2. VB
This is a gate drive voltage generator and VCC-5.0V regulator for internal circuit voltage.
3. Oscillator
This is a precise wave oscillation circuit with operation frequency fixed to 1.0MHz.
4. Error AMP
This is an error amplifier which detects output signal, and outputs PWM control signal. Internal reference voltage is set by PWM input signal. Also, the BD9227F have current mode control with internal slope compensation simplifies the external compensation calculation and reduces component count while allowing the use of ceramic output capacitors.
5. ICOMP
This is a comparator that outputs PWM signal from current feed-back signal and error-amp output for current-mode.
6. Pch FET SW
This is a 20V/200mΩ Power Pch MOSFET SW that converts inductor current of DC/DC converter.
7. UVLO
This is a low voltage error prevention circuit.
This prevents internal circuit error during increase of power supply voltage and during decline of power supply voltage. It monitors VCC pin voltage and internal REG voltage, and when VCC voltage becomes 5.3V and below, it turns OFF all output FET and DC/DC converter's output, and Soft Start circuit resets.
Now this threshold has hysteresis of 200mV(Typ).
8. TSD
Circuit for preventing malfunction at high Temperature.
When it detects an abnormal temperature exceeding $T_J=150^{\circ}\text{C}$, it turns OFF DC/DC Converter Output. The threshold of TSD has Hysteresis. If temperature falls, the IC automatically returns.
9. OVP
Over Voltage Protection.
Output voltage is monitored with FB terminal, and output FET is turned off when it becomes $V_{\text{NON}}+200\text{mV}$.
10. OCP
This is a circuit to protect the high-side FET from over-current. Every cycle the switch current and the reference voltage of over-current protection are compared; when the peak inductor current continuously intersects the reference voltage, the high-side switch is turned off. Once 2 times continuous over current is detected, the device will stop and COMP/ NON pin voltage will be reset(to GND) and after 8.191ms the device restart. (refer to Page.7 Figure 5)
11. PWM
The PWM pin is the input pin to control active or inactive of the BD9227F and the PWM input pulse determines the OUTPUT voltage (refer to Page.15 (3) Output Voltage Setting).
Once the pulse is input on the PWM pin, the internal enable signal turns on then the internal regulator turns on. After the each regulator operates, the BD9227F starts switching. When the low period of the PWM pulse is longer than 2.047msec (typ), the BD9227F stops operation (refer to Page.7 Figure 4).

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
VCC to GND	V _{CC}	-0.3 to +22	V
VB to GND	V _B	-0.3 to +22	V
LX to GND	V _{LX}	-2.0 to +22	V
VCC to LX	ΔV _{LX}	-0.3 to +22	V
VCC to VB	ΔV _B	-0.3 to +7	V
COMP to GND	V _{COMP}	-0.3 to +7	V
NON to GND	V _{NON}	-0.3 to +7	V
FB to GND	V _{FB}	-0.3 to +7	V
PWM to GND	V _{PWM}	-0.3 to +7	V
High-Side FET Drain Current	I _{DH}	OCP	A
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Temperature	T _{jmax}	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
SOP8				
Junction to Ambient	θ_{JA}	197.4	109.8	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	21	19	°C/W

(Note 1) Based on JESD51-2A(Still-Air)

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note3) Using a PCB board based on JESD51-3

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

(Note 4) Using a PCB board based on JESD51-7

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{CC}	6	-	20	V
Output Voltage	$V_{OUT}^{(Note5)}$	$V_{CC} \times 0.252$	-	V_{CC}	V
Output Current	I_{OUT}	-	-	1	A
NON Input Voltage	V_{NON}	-	-	1	V
PWM Input Voltage	V_{PWM}	-	-	5.5	V
PWM Input Frequency	F_{PWM}	1	-	50	kHz
Input Capacitor	$C_{VCC}^{(Note6)}$	4.7	10	-	μF
Inner Regulator Capacitor	$C_{VB}^{(Note7)}$	0.047	0.1	0.22	μF
Inductor	$L^{(Note8)}$	4.7	10	-	μH
Output Capacitor	$C_{OUT}^{(Note9)}$	4.7	10	-	μF
Ref Voltage Capacitor	$C_{NON}^{(Note10)}$	-	1	-	μF
Operating Temperature	T_{opr}	-40	-	+85	$^{\circ}C$

Please select each capacitor considering the effect of DC bias and temperature coefficient to satisfy the specification.

(Note5) Refer to P.19(10)

(Note6) Refer to P.16 (6)

(Note7) Refer to P.16 (4)

(Note8) Refer to P.15 (1)

(Note9) Refer to P.15 (2)

(Note10) Refer to P.16 (7)

Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=16.0V, VOUT=12.0V, PWM=H)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current						
Operating Non-Switching Supply Current	I _{CC}	-	0.4	1.0	mA	PWM=H, FB=3V (Non-switching)
Standby Quiescent Current	I _{ST}	-	0.05	0.2	mA	PWM=L
Under Voltage Lockout						
Detect Threshold Voltage	V _{UV}	5.0	5.3	5.6	V	VCC falling
Hysteresis Width	V _{UVHY}	-	200	400	mV	
Oscillator						
Oscillating Frequency	F _{SW}	0.80	1.00	1.20	MHz	
Error Amplifier						
FB Pin Reference Voltage	V _{FBN}	0.990	1.000	1.010	V	PWM=H, Ta=25°C
	V _{FBA}	0.980	1.000	1.020	V	PWM=H, Ta=-40 to +85°C
FB Pin Bias Current	I _{FB}	-1.0	0	+1.0	μA	VFB = 0 V
NON Inner R	R _{NON}	100	250	400	kΩ	
ICOMP Sink Current	I _{VC_{SI}}	7.5	15	30	μA	COMP=1V, NON=1V, FB=2V
ICOMP Source Current	I _{VC_{SO}}	-30	-15	-7.5	μA	COMP=1V, NON=1V, FB=0V
Error Amplifier Transconductance	G _m	50	115	180	μA/V	ICOMP= ± 3μA, NON=1V, COMP=1V
Switch Current to COMP Transconductance	G _{CS}	-	2.2	5	A/V	VCC=16V
High-Side MOSFET						
On Resistance	R _{ONH}	-	200	-	mΩ	
VB Clamp Voltage	V _B	VCC-5.5	VCC-5	VCC-4.5	V	
Over Current Detect Current	I _{OCP}	1.6	2.6	4.2	A	
PWM						
PWM Logic High Level	V _{PWMH}	1.5	-	5.5	V	
PWM Logic Low Level	V _{PWML}	-	-	0.5	V	
PWM Internal Pull-Down Resistor	R _{PWM}	200	500	800	kΩ	

Timing Chart

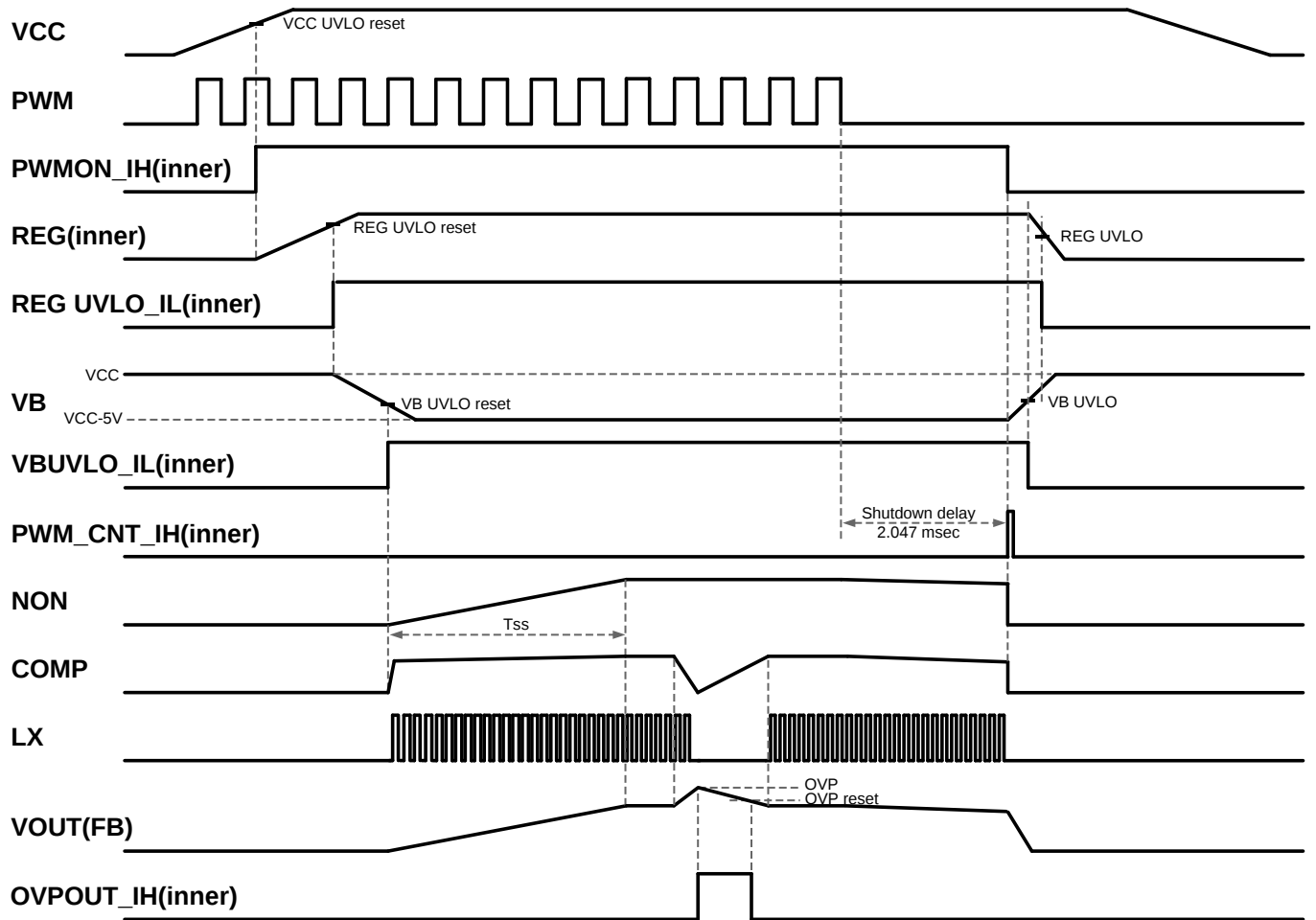


Figure 4. Startup/Shutdown Timing Chart

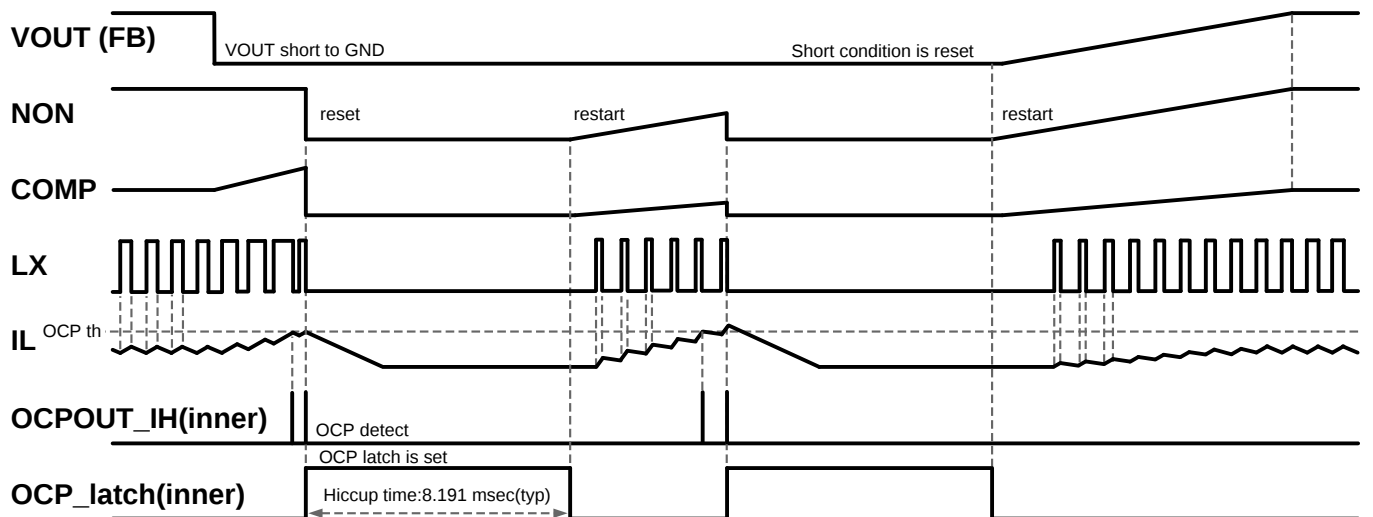


Figure 5. OCP Timing Chart

Typical Performance Characteristics (Unless otherwise specified, Ta=25°C, Vcc=16V, Vout=12V, PWM=3V)

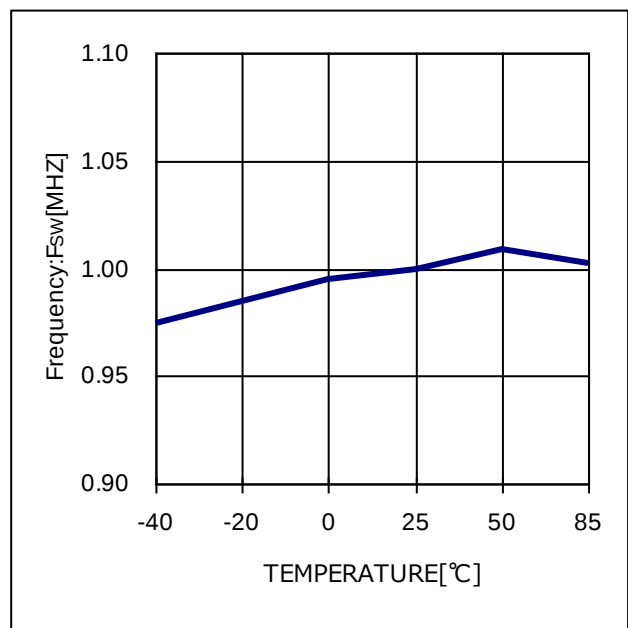


Figure 6. Frequency - Temperature

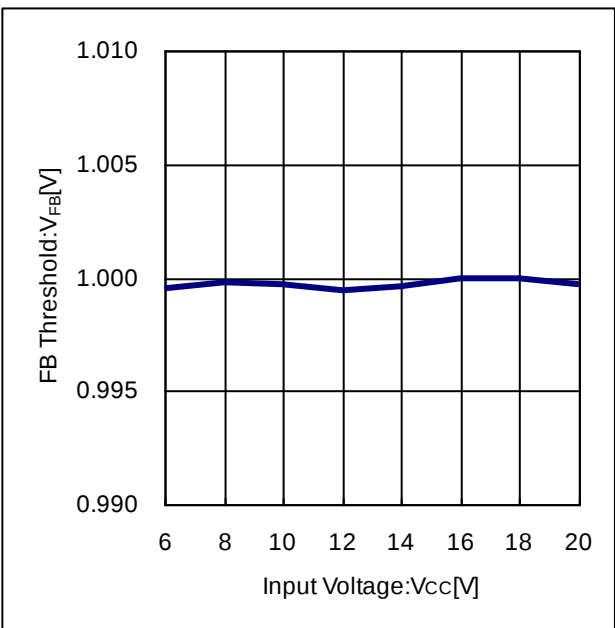


Figure 7. FB Threshold Voltage – Input Voltage

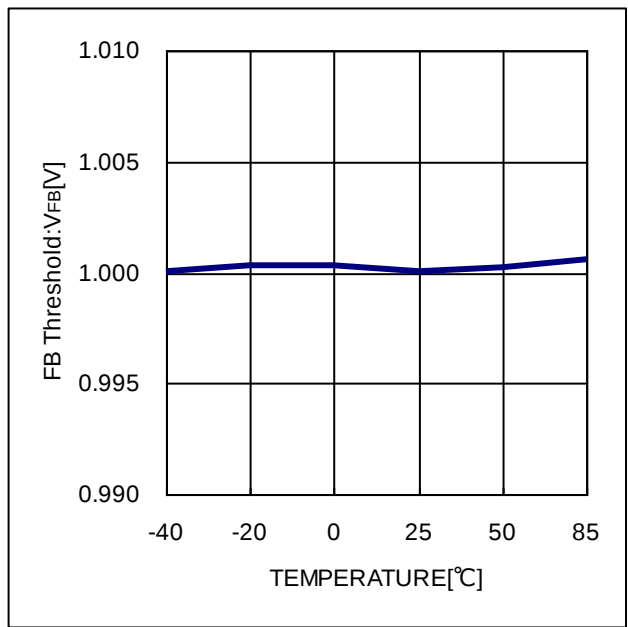


Figure 8. FB Threshold Voltage - Temperature

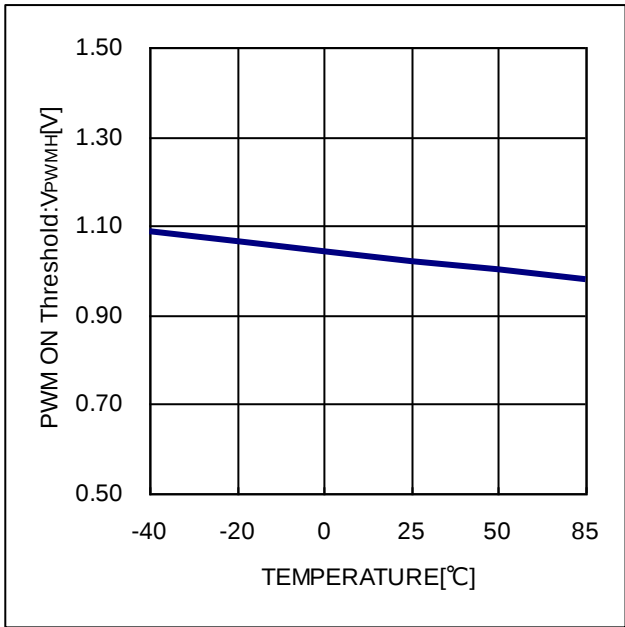


Figure 9. PWM Pin Inner REG ON Threshold - Temperature

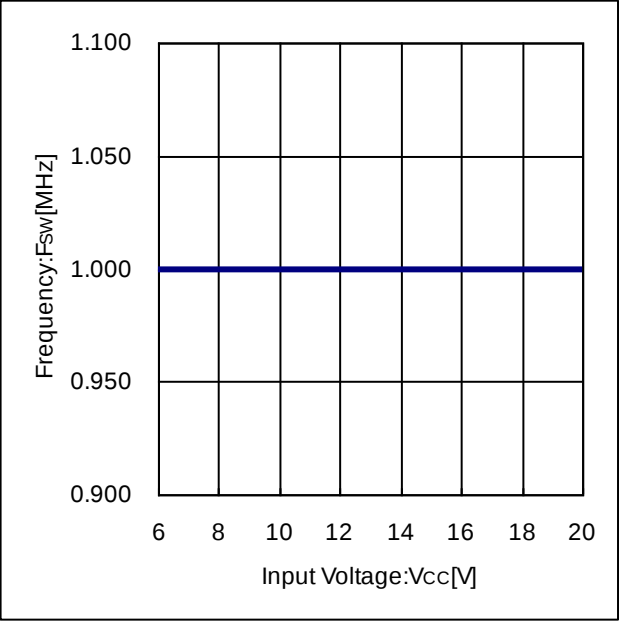


Figure 10. Frequency – Input Voltage

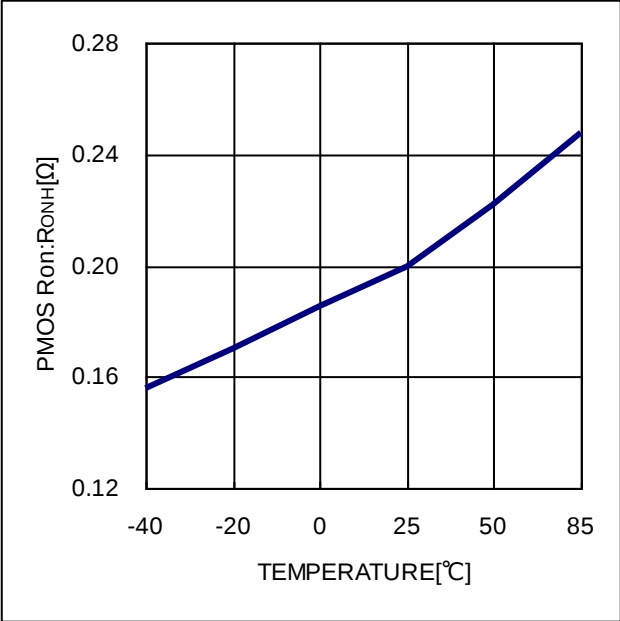


Figure 11. PMOS ON Resistance - Temperature

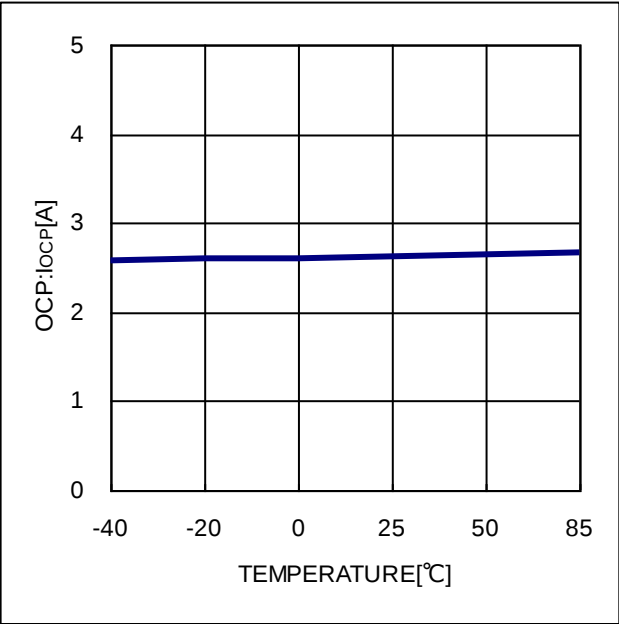


Figure 12. OCP Detect Current - Temperature

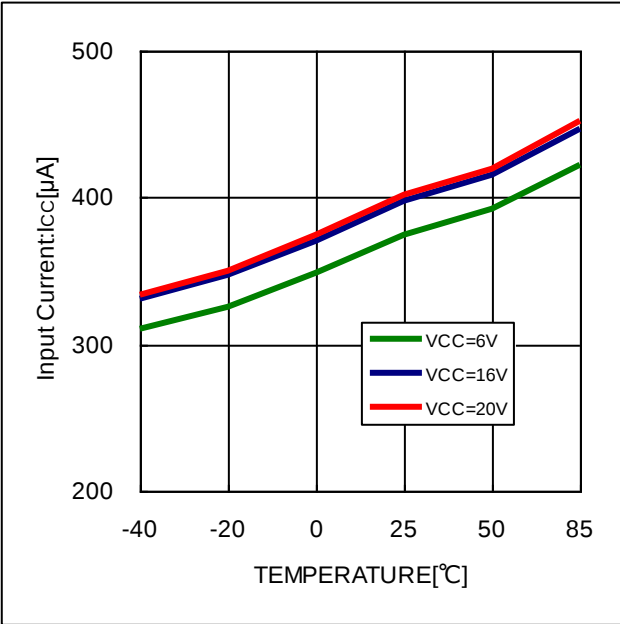


Figure 13. Operating Current – Temperature

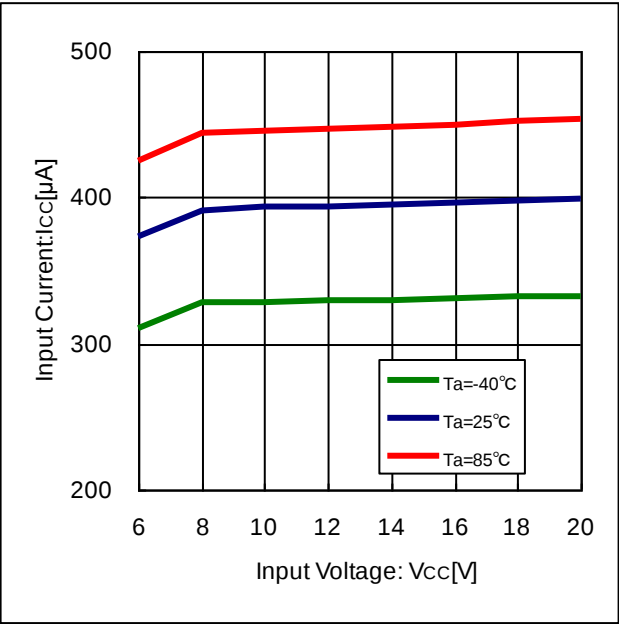


Figure 14. Operating Current – Input Voltage

Reference Characteristics of Typical Application Circuits

• VOUT=12V

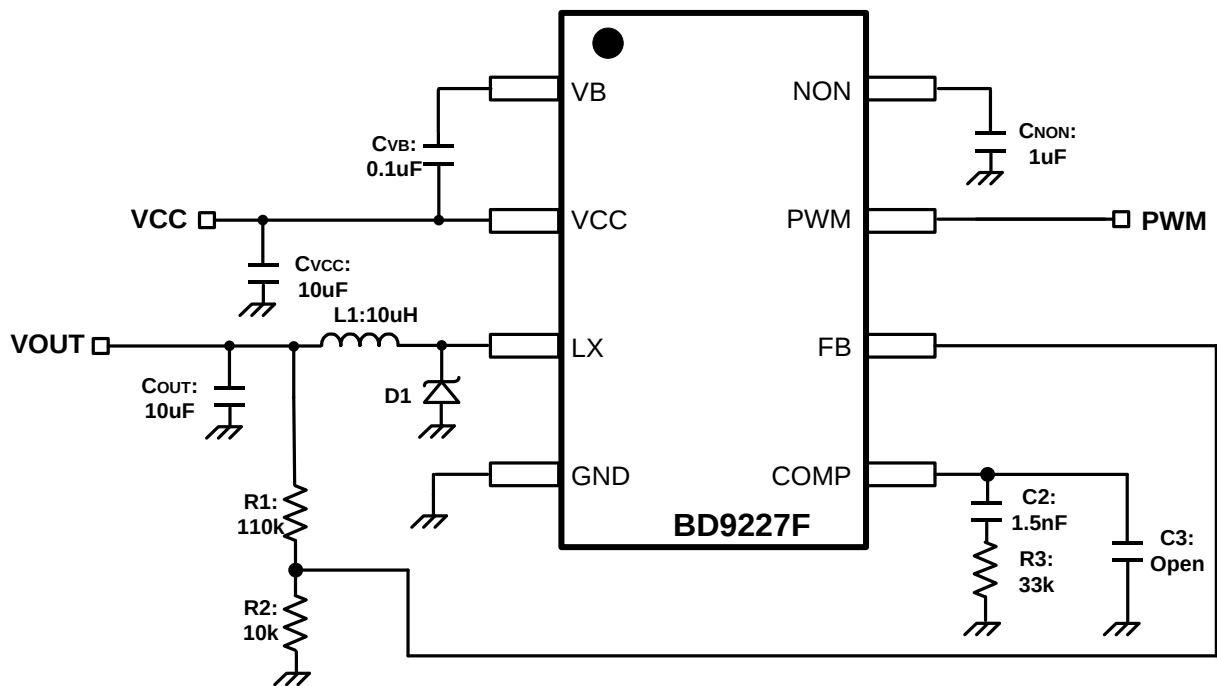


Figure 15. Typical Application Circuit (VOUT=12V)

Parts	L1 :	Coilcraft	LPS5030-103ML	10µH
	Cvcc/Cout :	Murata	GRM31CR71E106MA12#	10µF/25V
	CvB :	Murata	GRM155R71E104ME14#	0.1µF/25V
	D1 :	Rohm	RB060MM-30	

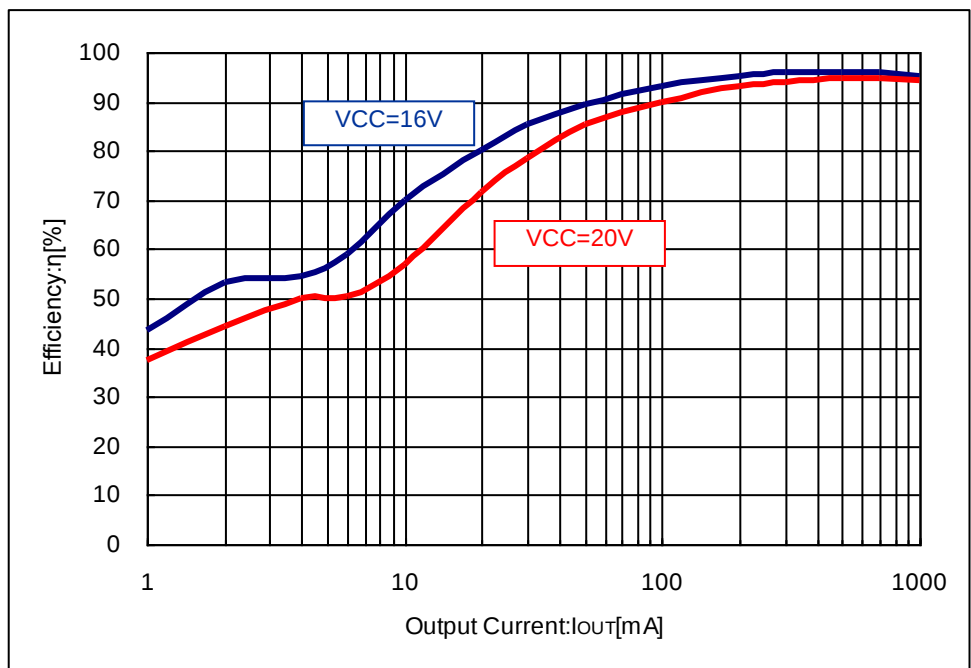


Figure 16. Efficiency-Output Current (VOUT=12V)

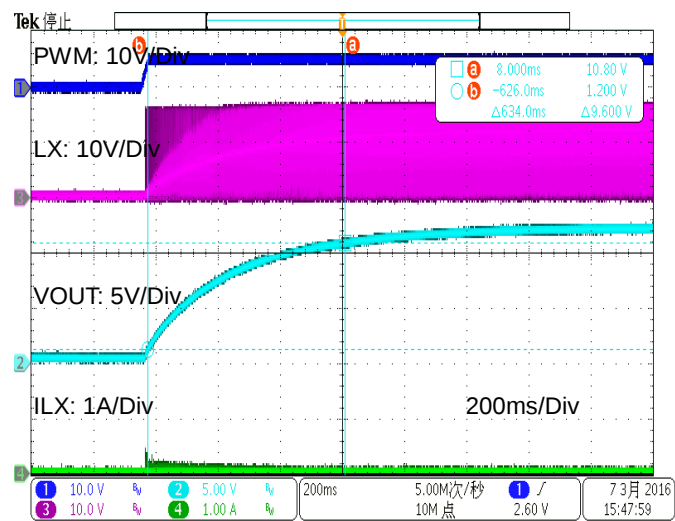


Figure 17. Start-up Characteristics
($V_{CC}=16\text{V}$, $I_{OUT}=0\text{mA}$, $V_{OUT}=12\text{V}$)

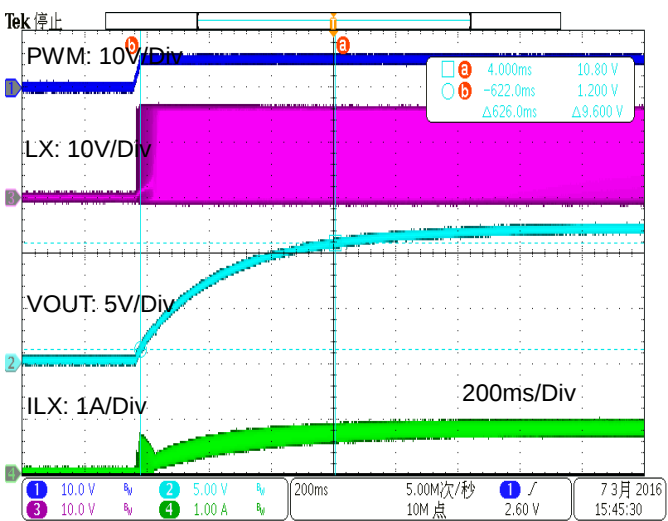


Figure 18. Start-up Characteristics
($V_{CC}=16\text{V}$, $I_{OUT}=1\text{A}$, $V_{OUT}=12\text{V}$)

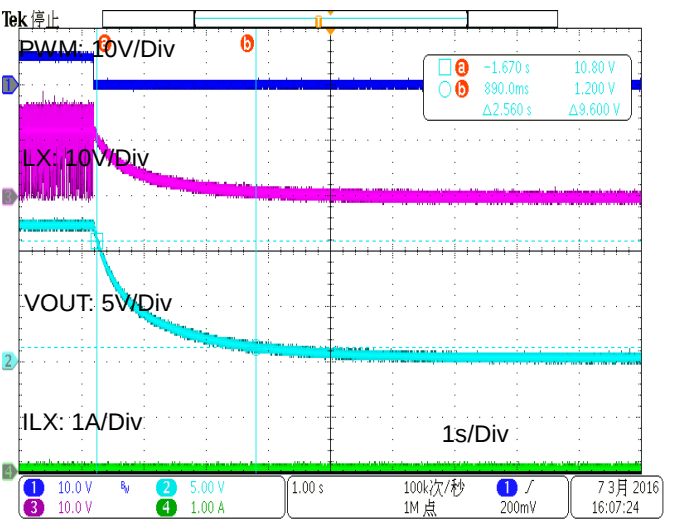


Figure 19. Shut-down Characteristics
($V_{CC}=16\text{V}$, $I_{OUT}=0\text{mA}$, $V_{OUT}=12\text{V}$)

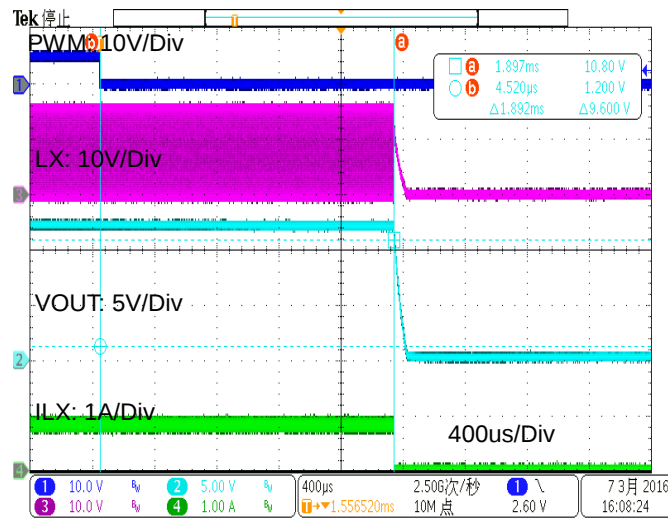


Figure 20. Shut-down Characteristics
($V_{CC}=16\text{V}$, $I_{OUT}=1\text{A}$, $V_{OUT}=12\text{V}$)

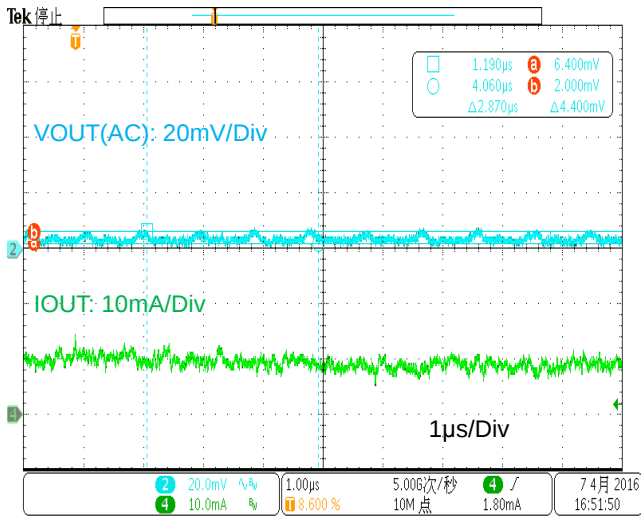


Figure 21. VOUT Ripple
($V_{CC}=16V$, $I_{OUT}=10mA$; $V_{OUT}=12V$)

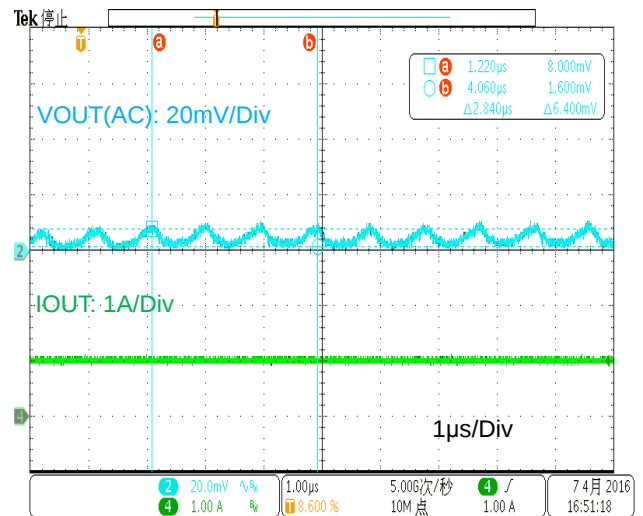


Figure 22. VOUT Ripple
($V_{CC}=16V$, $I_{OUT}=1A$, $V_{OUT}=12V$)

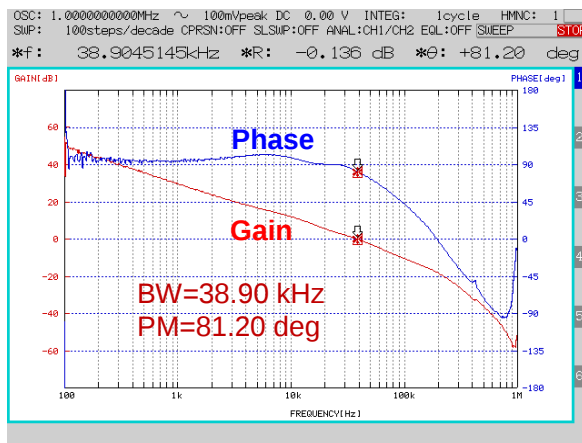


Figure 23. Frequency Response
($V_{CC}=16V$, $I_{OUT}=100mA$, $V_{OUT}=12V$)

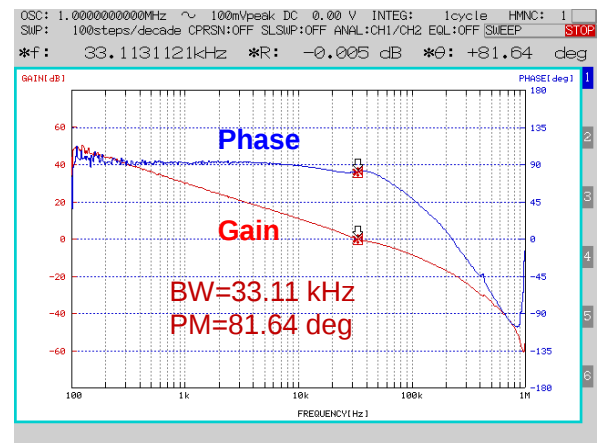


Figure 24. Frequency Response
($V_{CC}=16V$, $I_{OUT}=1A$, $V_{OUT}=12V$)

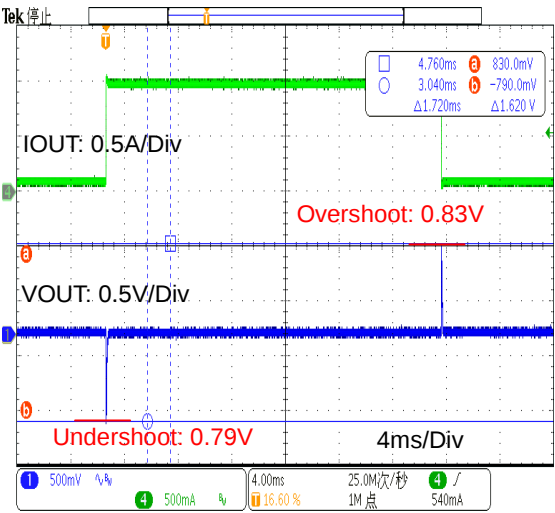


Figure 25. Load Response
(VCC=16V, VOUT=12V, IOUT=100mA⇔1A)

Selection of Components Externally Connected

(1) Inductors

Something of the shield type that fulfills the current rating (Current value I_{peak} below), with low DCR is recommended. Value of Inductance influences Inductor Ripple Current and becomes the cause of Output Ripple. In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

$$I_{peak} = I_{OUT} + \frac{\Delta IL}{2} \quad (1)$$

$$\Delta IL = \frac{VCC - VOUT}{L1} \times \frac{VOUT}{VCC} \times \frac{1}{f} \quad (2)$$

where:

ΔIL is the Output Ripple Current,

VCC is the Input Voltage.

$VOUT$ is the Output Voltage.

f is the Switching Frequency.

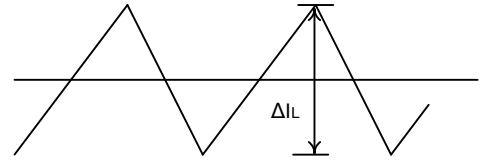


Figure 26. Inductor Current

For design value of Inductor Ripple Current, please carry out design tentatively with about 20% ~ 50% of Maximum Input Current. In the BD9227F, it is recommended the inductance value more than 4.7μH.

Recommended Inductor **CoilCraft LPS5030 Series**

⚠When current that exceeds Coil rating flows to the coil, the Coil causes a Magnetic Saturation, and there are cases wherein a decline in efficiency, oscillation of output happens. Please have sufficient margin and select so that Peak Current does not exceed Rating Current of Coil.

(2) Output Capacitor

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended. Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage. The output ripple voltage can be estimated by the following formula.

$$V_{pp} = \Delta IL \times \frac{1}{2\pi \times f \times COUT} + \Delta IL \times R_{ESR} \quad (3)$$

The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the crossover frequency at less than 1/20 of the switching frequency. With high switching frequencies such as the 1.0MHz frequency of this design, internal circuit limitations of the BD9227F limit the practical maximum crossover frequency to about 50kHz. In general, the crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

$$COUT_{min} = \frac{1}{2\pi \times RI \times fc_{max}} \quad (4)$$

Where:

RI is the output load resistance.

fc_{max} is the maximum crossover frequency.

Please design in a way that it is held within Capacity Ripple Voltage.

In the BD9227F, it is recommended a ceramic capacitor more than 4.7μF.

(3) Output Voltage Setting

ERROR AMP internal Standard Voltage is 1V, V_{NON} Voltage is determined by

$$V_{NON} = 1V \times PWM \text{ Duty} \quad (5)$$

Where:

PWM Duty is the duty of the waveform inputted into PWM terminal.

Output Voltage is determined by

$$VOUT = \frac{R1 + R2}{R2} * PWM \text{ Duty} \quad (6)$$

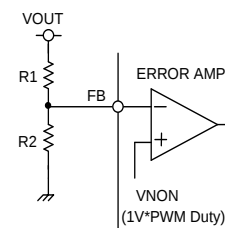


Figure 27. Output Voltage

(4) VB Capacitor

Please connect from 0.047μF~0.22μF (Ceramic Capacitor) between VCC Pin and VB Pin.
(**caution:** Don't connect Capacitor between VB pin to GND pin that cause destroy the chip)

(5) Catch Diode

The BD9227F is designed to operate using an external catch diode between LX and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the LX pin, which is VCCMAX + 0.5 V. Peak current must be greater than IOUTMAX + 1/2 ΔIL plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. It's recommended to use schottky barrier diode with the BD9227F.

(6) Input Capacitor

The BD9227F requires an input capacitor for decoupling and depending on the application. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but low-ESR electrolytic capacitors may also suffice. Please place this capacitor as possible as close to the VCC pin. In the BD9227F, it is recommended a ceramic capacitor more than 4.7μF. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta VCC = \frac{IOUT}{f \times CVCC} \times \frac{VOUT}{VCC} \times \left[1 - \frac{VOUT}{VCC} \right] \quad (7)$$

Since the input capacitor (CVCC) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CVCC} = IOUT \times \sqrt{\frac{VOUT}{VCC} \times \left[1 - \frac{VOUT}{VCC} \right]} \quad (8)$$

The worst case condition occurs at VCC = 2VOUT, where

$$I_{CVCC_max} = \frac{IOUT}{2} \quad (9)$$

(7) Recommended CNON (vs PWM Frequency) setting

The PWM signal control ON/OFF of BD9227F(PWM>1.5V ON, PWM<0.5V OFF) , and PWM duty determine the NON value, In order to get proper NON ripple value, according PWM frequency to select proper CNON capacitor.
Below is the relationship of PWM frequency, CNON and NON ripple:

$$NON_{ripple} = \frac{D \times (1 - D)}{R \times C_{NON} \times PWM_Frequency} \quad (10)$$

When D=0.5, NON ripple=NON ripple(max)

$$NON_{ripple(max)} = \frac{0.25}{R \times C_{NON} \times PWM_Frequency} \quad (11)$$

where:

D is PWM Duty.

R is Inner 250kΩ resistor.

NON ripple=1mV condition.

NON value=1V*PWM Duty.

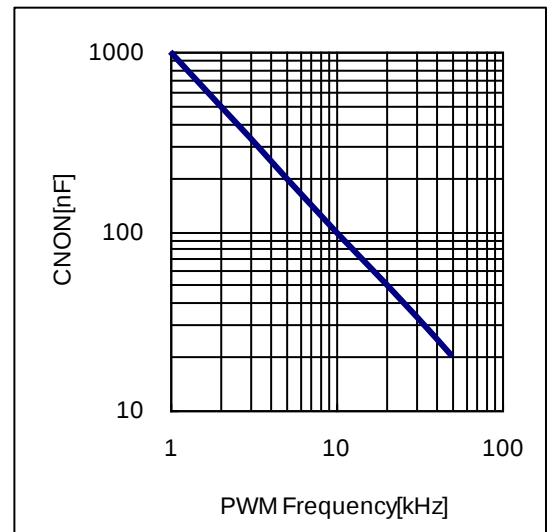


Figure 28. Recommended PWM Frequency vs CNON

(8) Recommended Tss selection vs C_{NON}

BD9227F Softstart time T_{ss} is determined by NON rising speed, T_{ss} have relation with C_{NON}.

Below is the relationship of T_{ss} and C_{NON}

$$T_{ss} = 4.61 \times R \times C_{NON} \quad (12)$$

where:

R is the inner 250kΩ resistor.

NON reach 99% of Target NON value

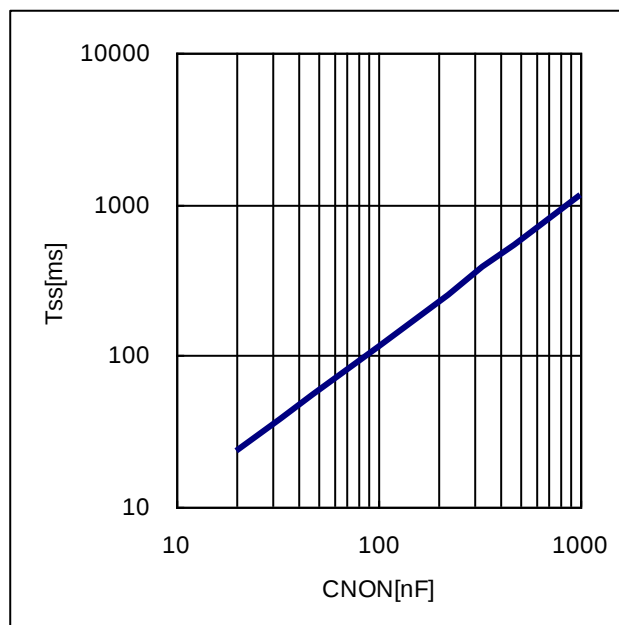


Figure 29. Recommended C_{NON} vs T_{ss}

(9) About Adjustment of DC/DC Comparator Frequency Characteristics

Role of Phase compensation element C2, C3, R3 (See P.11 Figure15. Example of Reference Application Circuit)

Stability and Responsiveness of Loop are controlled through COMP Pin which is the output of Error Amp.

The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the COMP Pin.

DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$A_{dc} = R_l \times G_{cs} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}} \quad (13)$$

Here, V_{FB} is Feedback Voltage (1.0V*PWM Duty).A_{EA} is Voltage Gain of Error amplifier (typ : 66.8 dB), G_{cs} is the Trans-conductance of Current Detect (typ : 2.2A/V), and R_l is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.

The first occurs with/ through the output resistance of Phase compensation Capacitor (C2) and Error amplifier.

The other one occurs with/through the Output Capacitor and Load Resistor.

These poles appear in the frequency written below.

$$f_{p1} = \frac{G_{EA}}{2 \times \pi \times C2 \times A_{EA}} \quad (14)$$

$$f_{p2} = \frac{1}{2 \times \pi \times COUT \times R_l} \quad (15)$$

Here, G_{EA} is the trans-conductance of Error amplifier (typ : 115uA/V).

Here, in this Control Loop, one zero becomes important.

With the zero which occurs because of Phase compensation Capacitor C2 and Phase compensation Resistor R3, the Frequency below appears.

$$f_{z1} = \frac{1}{2 \times \pi \times C2 \times R3} \quad (16)$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).

This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$f_{z_{ESR}} = \frac{1}{2 \times \pi \times COUT \times RESR} \quad (17) \quad (\text{ESR zero})$$

In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C3) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.

This pole exists in the frequency shown below.

$$fp3 = \frac{1}{2 \times \pi \times C3 \times R3} \quad (18) \quad (\text{pole that corrects ESR zero})$$

The target of Phase compensation design is to create a communication function in order to acquire necessary bandwidth and Phase margin.

Cross-over Frequency (bandwidth) at which Loop gain of Return Loop becomes "0" is important.

When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.

On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.

Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency. Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency. Calculation of RC is done using the formula below.

$$R3 = \frac{2 \times \pi \times COUT \times fc}{G_{EA} \times G_{CS}} \times \frac{VOUT}{VFB} \quad (19)$$

Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Switching Frequency (Fsw).

2. Phase compensation Capacitor (C2) is selected in order to achieve the desired phase margin. In an application that has a representative Inductance value (more than 4.7uH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C2 can be calculated using the following formula.

$$C2 > \frac{4}{2 \times \pi \times R3 \times fc} \quad (20)$$

3. Examination whether the second Phase compensation Capacitor C3 is necessary or not is done. If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

$$\frac{1}{2 \times \pi \times COUT \times RESR} < \frac{F_{sw}}{2} \quad (21)$$

In this case, add the second phase compensation Capacitor C3, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

C3 is looked for using the following formula:

$$C3 = \frac{COUT \times RESR}{R3} \quad (22)$$

(10) About PWM Duty adjustable range of BD9227F

BD9227F VOUT voltage is determined by LX duty, but BD9227F Ton-min limited Duty range. The Ton-min(max)=210ns, Tperiod(min)=833ns, then the Duty worst=210/833=25.2%, then the 25.2%<VOUT/VCC<100%.

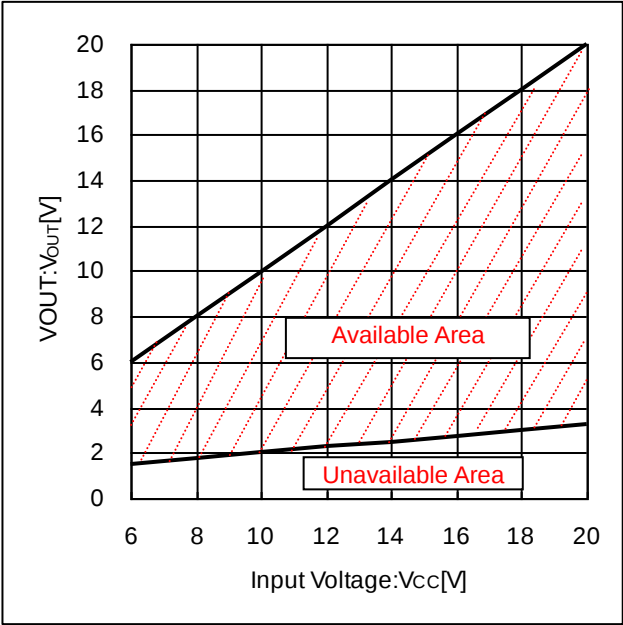


Figure 30. VOUT vs VCC available range

Cautions on PCB board layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. See Figure31 for a PCB layout example.

In the BD9227F, since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. And GND area should be connected directly to power GND for avoiding the external connect which causes the different GND voltage. The additional external components can be placed approximately as shown.

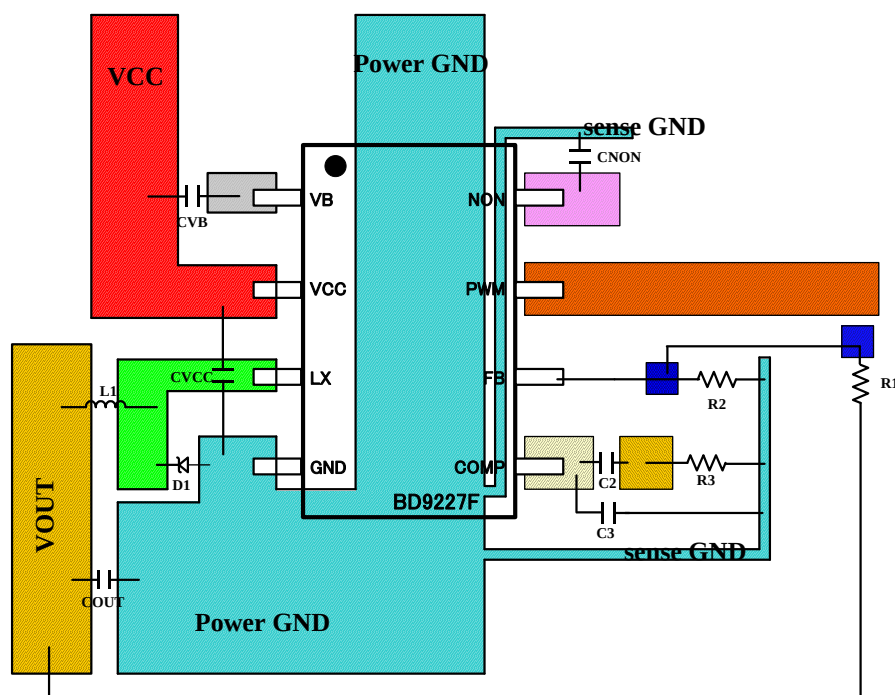


Figure 31. Reference PCB

I/O Equivalent Circuit

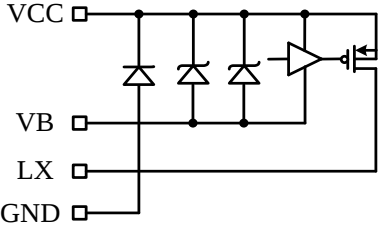
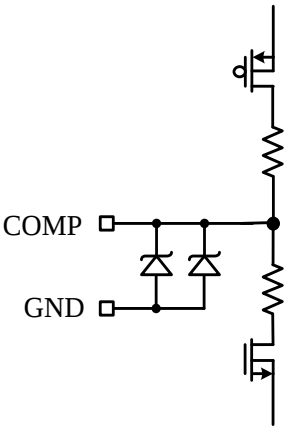
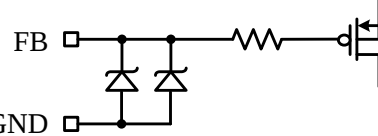
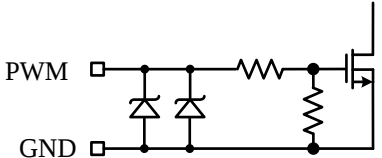
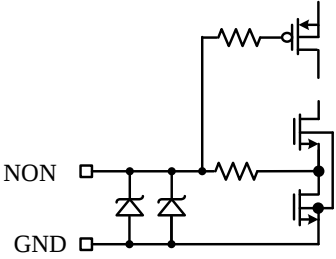
Pin. No	Pin Name	Pin Equivalent Circuit	Pin. No	Pin Name	Pin Equivalent Circuit
1 2 3 4	VB VCC LX GND		5	COMP	
6	FB		7	PWM	
8	NON				

Figure 32. I/O Equivalent Circuit

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

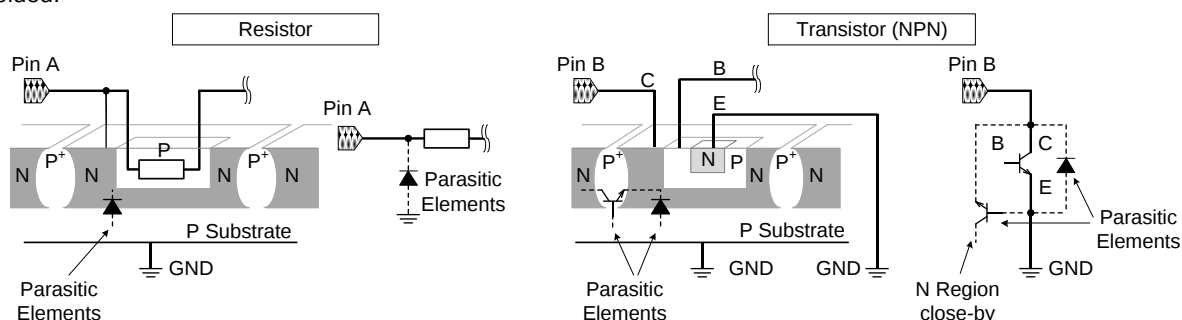
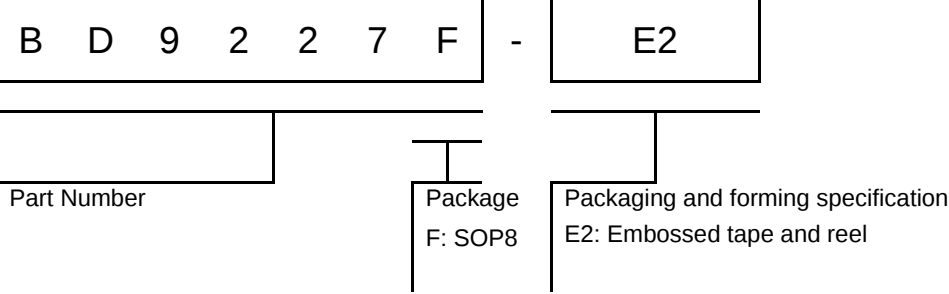


Figure 33. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information



Marking Diagram

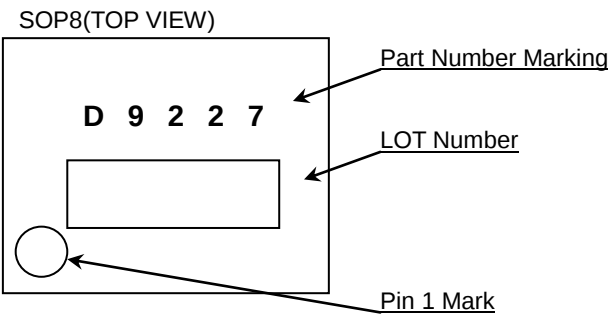
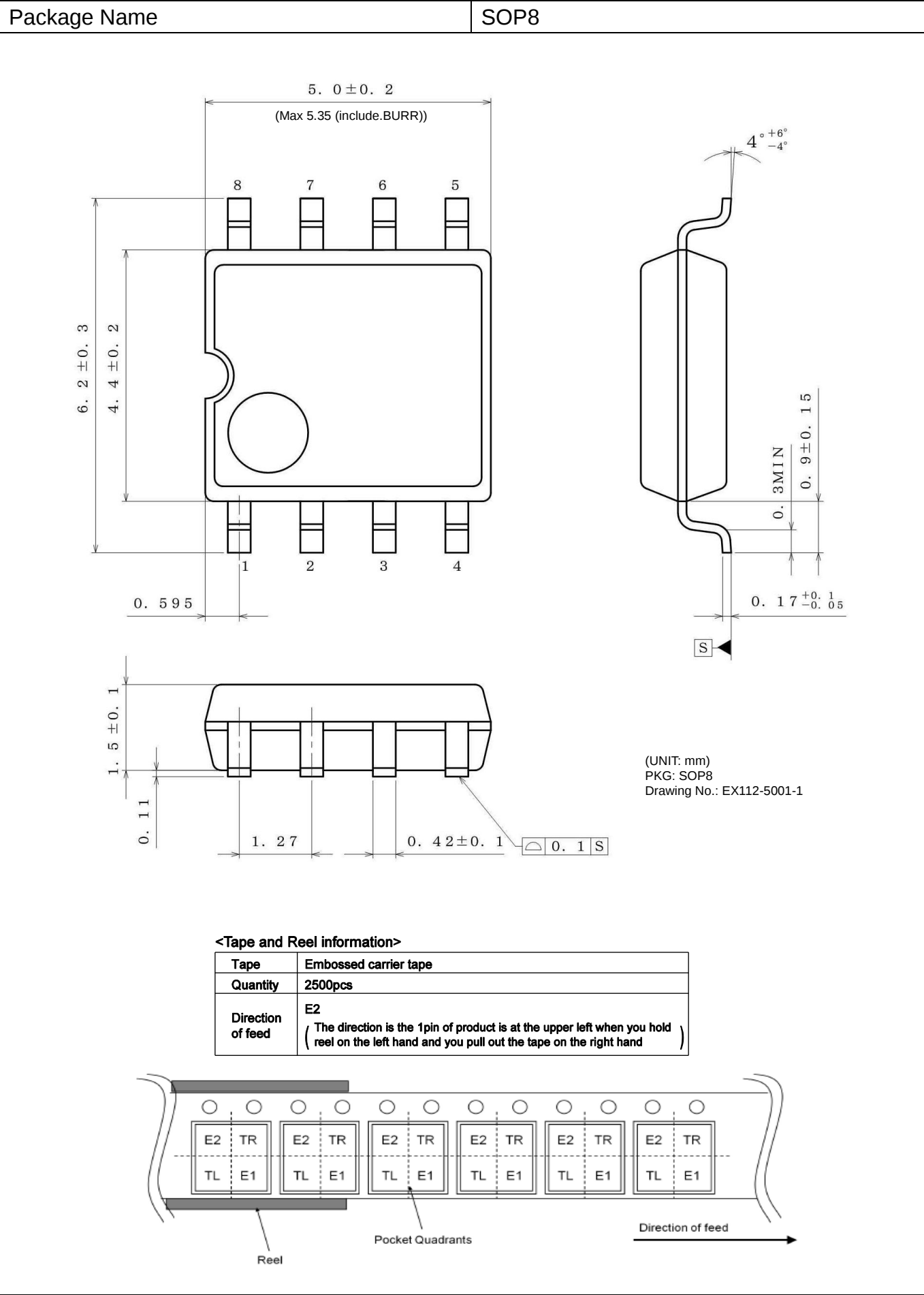


Figure 34. Marking Diagram

Physical Dimension and Packing Information



Revision History

Data	Revision	Changes
8.Jun.2016	001	New Release
31.Aug.2017	002	The modifications are following: p22 : Operational Notes p25 : Physical Dimension and Packing Information

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