CMOS, Low Voltage, 3-Wire Serially-Controlled, Matrix Switches

Data Sheet **ADG738/ADG739**

FEATURES

- 3-wire serial interface
- 2.7 V to 5.5 V single supply
- 2.5 Ω on resistance
- 0.75 Ω on-resistance flatness
- 100 pA leakage currents
- Single 8-to-1 multiplexer ADG738
- Dual 4-to-1 multiplexer ADG739
- Power-on reset
- TTL/CMOS-compatible
- Qualified for automotive applications

APPLICATIONS

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching

FUNCTIONAL BLOCK DIAGRAMS

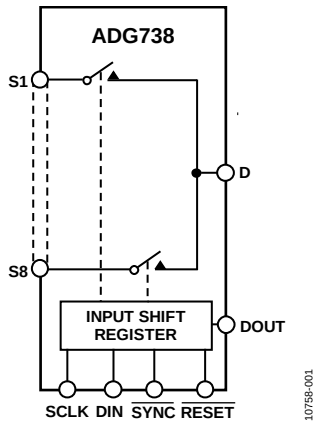


Figure 1.

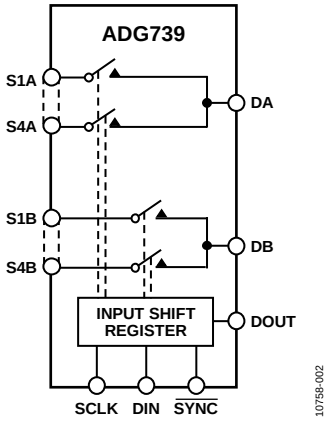


Figure 2.

GENERAL DESCRIPTION

The ADG738 and ADG739 are CMOS analog matrix switches with a serially-controlled 3-wire interface. The ADG738 is an 8-channel matrix switch, while the ADG739 is a dual 4-channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range.

The ADG738 and ADG739 utilize a 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE®, and some DSP interface standards. The output of the input shift register, DOUT, enables a number of these parts to be daisy-chained. On power-up, the internal input shift register contains all zeros and all switches are in the off state.

Each switch conducts equally well in both directions when on, making these parts suitable for both multiplexing and demultiplexing applications. As each switch is turned on or off by a separate bit, these parts can also be configured as a type of switch array, where any, all, or none of the eight switches may be closed at any time. The input signal range extends to the supply rails.

All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The ADG738 and ADG739 are available in 16-lead TSSOP packages.

PRODUCT HIGHLIGHTS

1. 3-Wire Serial Interface.
2. Single Supply Operation. The ADG738/ADG739 are fully specified and guaranteed with 3 V and 5 V supply rails.
3. Low On Resistance, 2.5 Ω typical.
4. Any configuration of switches may be on or off at any one time.
5. Guaranteed Break-Before-Make Switching Action.
6. Small 16-lead TSSOP Package.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

11/12—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Features Section ... 1
Added W Version Specifications to Table 1 ... 3
Added W Version Specifications to Table 2 ... 4
Changes to Table 4 ... 6
Changes to Figure 7, Figure 8, and Figure 11 ... 9
Changes to Figure 12 ... 10
Deleted Figure 22 ... 12
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

4/00—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	B Version −40°C to +85°C	W Version −40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5			Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA; see Figure 19
	4.5	5	6	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		0.4		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		0.8	1	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75			Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	1.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage I_S (Off)	±0.01			nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V; see Figure 20
	±0.1	±0.3	±0.6	nA max	
Drain Off Leakage I_D (Off)	±0.01			nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V
	±0.1	±1	±1.3	nA max	
Channel On Leakage I_D, I_S (On)	±0.01			nA typ	V_D = V_S = 1 V/4.5 V, see Figure 21
	±0.1	±1	±1.3	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	±0.1	μA max	
C_{IN}, Digital Input Capacitance	3			pF typ	
DIGITAL OUTPUT					
Output Low Voltage		0.4		max	I_{SINK} = 6 mA
C_{OUT}, Digital Output Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	20			ns typ	R_L = 300 Ω, C_L = 35 pF, see Figure 22; V_{S1} = 3 V
		32	35	ns max	
t_{OFF}	10			ns typ	R_L = 300 Ω, C_L = 35 pF, see Figure 22; V_{S1} = 3 V
		17	20	ns max	
Break-Before-Make Time Delay, t_D	9			ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	1	ns min	V_{S1} = V_{S8} = 3 V, see Figure 22
Charge Injection	±3			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 23
Off Isolation	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25
Channel-to-Channel Crosstalk	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 24
−3 dB Bandwidth					
ADG738	65			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 25
ADG739	100			MHz typ	
C_S (Off)	13			pF typ	
C_D (Off)					
ADG738	85			pF typ	
ADG739	42			pF typ	
C_D, C_S (On)					
ADG738	96			pF typ	
ADG739	48			pF typ	
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	10			μA typ	Digital Inputs = 0 V or 5.5 V
		20	20	μA max	

[1] Guaranteed by design, not subject to production test.

V_{DD} = 3 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	B Version −40°C to +85°C	W Version −40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	6			Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA; see Figure 19
	11	12	16	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		0.4		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	1.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	3.5			Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source Off Leakage I_S (Off)	±0.01			nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V; see Figure 20
	±0.1	±0.3	±0.6	nA max	
Drain Off Leakage I_D (Off)	±0.01			nA typ	V_D = 3 V/1 V, V_D = 1 V/3 V
	±0.1	±1	±1.3	nA max	
Channel On Leakage I_D, I_S (On)	±0.01			nA typ	V_D = V_S = 3 V/1 V, see Figure 21
	±0.1	±1	±1.3	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.4	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	±0.1	μA max	
C_{IN}, Digital Input Capacitance	3			pF typ	
DIGITAL OUTPUT					
Output Low Voltage		0.4		max	I_{SINK} = 6 mA
C_{OUT}, Digital Output Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	40			ns typ	R_L = 300 Ω, C_L = 35 pF, see Figure 22; V_{S1} = 2 V
		70	75	ns max	
t_{OFF}	14			ns typ	R_L = 300 Ω, C_L = 35 pF, see Figure 22; V_{S1} = 2 V
		25	40	ns max	
Break-Before-Make Time Delay, t_D	12			ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	1	ns min	V_S = 2 V, see Figure 22
Charge Injection	±3			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 23
Off Isolation	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25
Channel-to-Channel Crosstalk	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 24
−3 dB Bandwidth					
ADG738	65			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 25
ADG739	100			MHz typ	
C_S (Off)	13			pF typ	
C_D (Off)					
ADG738	85			pF typ	
ADG739	42			pF typ	
C_D, C_S (On)					
ADG738	96			pF typ	
ADG739	48			pF typ	
POWER REQUIREMENTS					V_{DD} = 3.3 V
I_{DD}	10			μA typ	Digital Inputs = 0 V or 3.3 V
		20	20	μA max	

[1] Guaranteed by design, not subject to production test.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V. All specifications −40°C to +105°C, unless otherwise noted.

Table 3.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}		Unit	Test Conditions/Comments
	Min	Max		
f_{SCLK}		30	MHz	SCLK cycle frequency
t_1	33		ns	SCLK cycle time
t_2	13		ns	SCLK high time
t_3	13		ns	SCLK low time
t_4	0		ns	$\overline{SYNC}$ to SCLK active edge setup time
t_5	5		ns	Data setup time
t_6	4.5		ns	Data hold time
t_7	0		ns	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	33		ns	Minimum $\overline{SYNC}$ high time
t_9[3]	20		ns min	SCLK rising edge to DOUT valid

[1] See Figure 3.
[2] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] C_L = 20 pF, R_L = 1 kΩ.

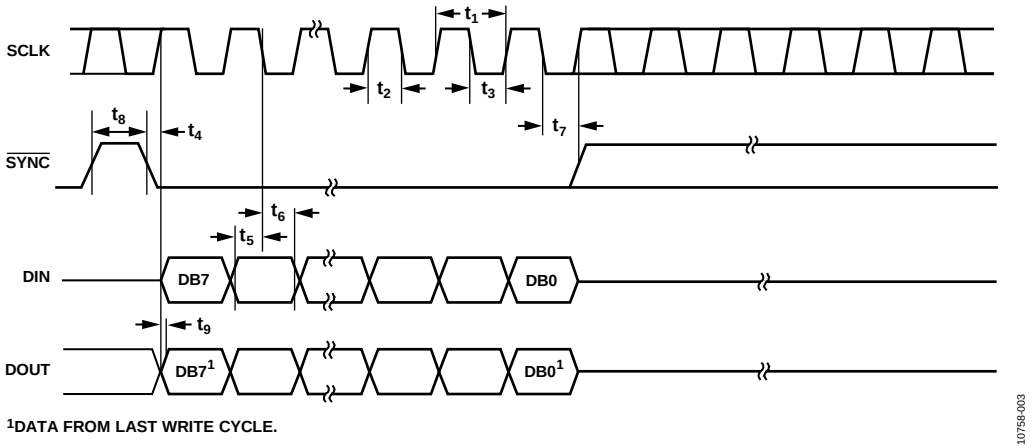


Figure 3. 3-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, Each S	30 mA
Continuous Current D	
ADG739	80 mA
ADG738	120 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Industrial (W Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	150.4°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Lead Temperature, Soldering	As per JEDEC J-STD-020

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

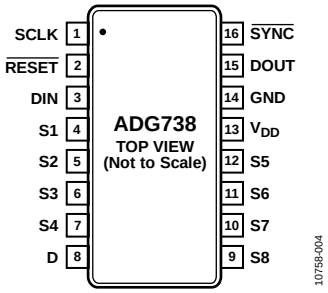


Figure 4. ADG738 Pin Configuration

Table 5. ADG738 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
2	$\overline{\text{RESET}}$	Active Low Control Input. This pin clears the input register and turns all switches to the off condition.
3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4, 5, 6, 7	S1, S2, S3, S4	Source. May be an input or output.
8	D	Drain. May be an input or output.
9, 10, 11, 12	S8, S7, S6, S5	Source. May be an input or output.
13	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
14	GND	Ground Reference.
15	DOUT	Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output, which should be pulled to the supply with an external resistor.
16	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switch conditions.

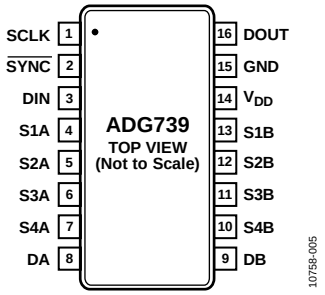


Figure 5. ADG739 Pin Configuration

Table 6. ADG739 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switch conditions.
3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4, 5, 6, 7	S1A, S2A, S3A, S4A	Source. May be an input or output.
8, 9	DA, DB	Drain. May be an input or output.
10, 11, 12, 13	S4B, S3B, S2B, S1B	Source. May be an input or output.
14	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
15	GND	Ground Reference.
16	DOUT	Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output, which should be pulled to the supply with an external resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

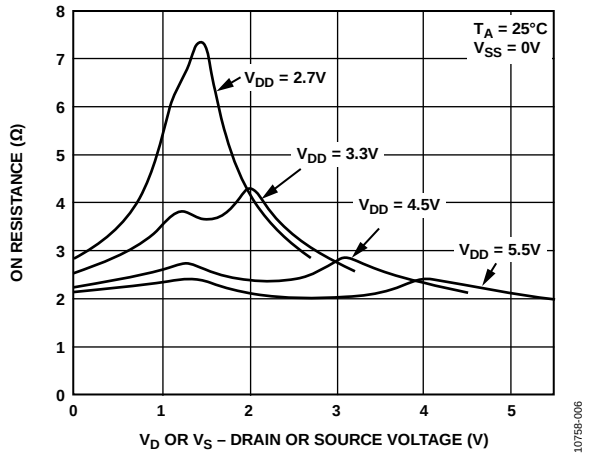


Figure 6. On Resistance as a Function of V_D (V_S)

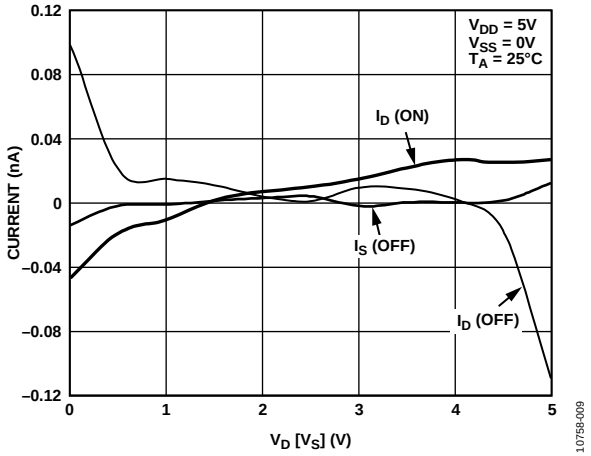


Figure 9. Leakage Currents as a Function of V_D (V_S), V_{DD} = 5 V

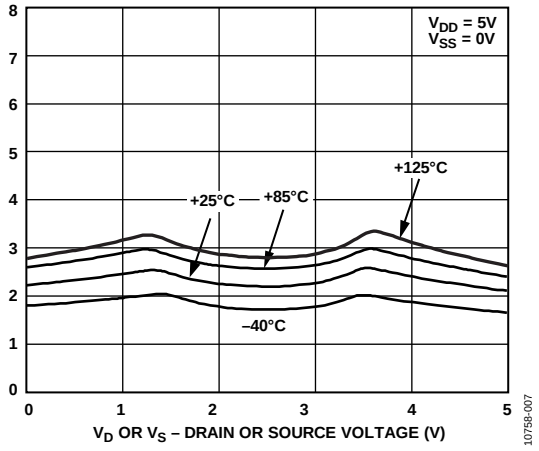


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, V_{DD} = 5 V

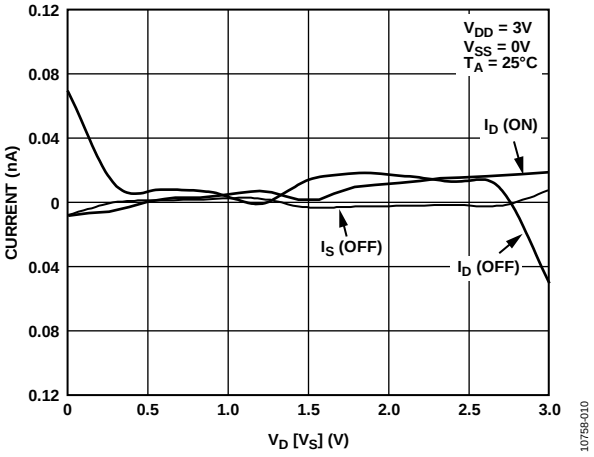


Figure 10. Leakage Currents as a Function of V_D (V_S), V_{DD} = 3 V

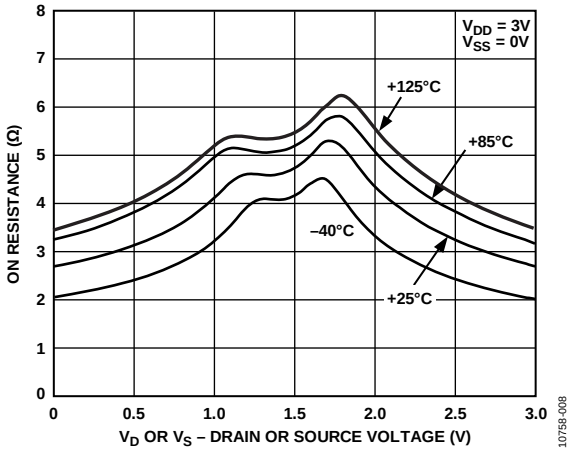


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, V_{DD} = 3 V

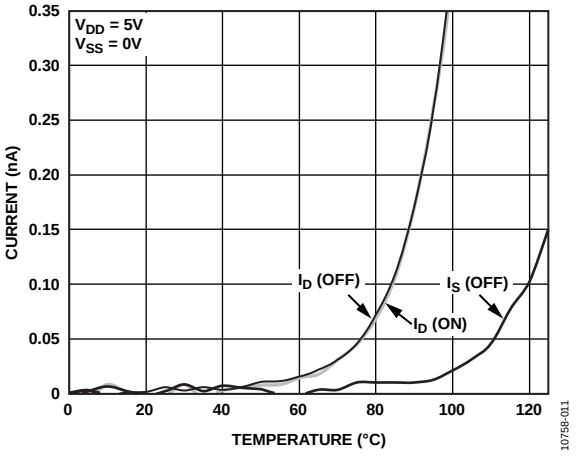


Figure 11. Leakage Currents as a Function of Temperature, V_{DD} = 5 V

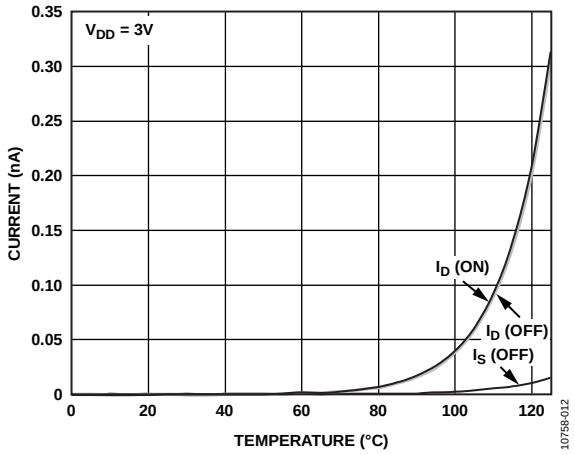


Figure 12. Leakage Currents as a Function of Temperature, V_{DD} = 3 V

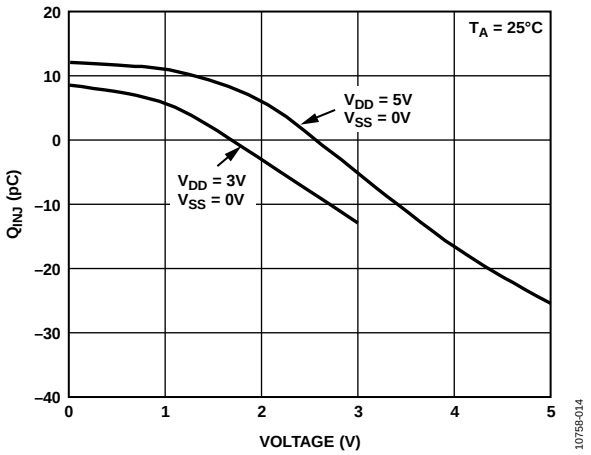


Figure 14. Charge Injection vs. Source Voltage

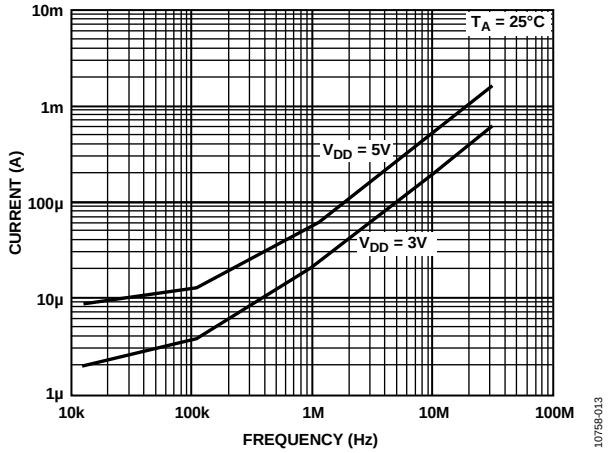


Figure 13. Input Currents vs. Switching Frequency

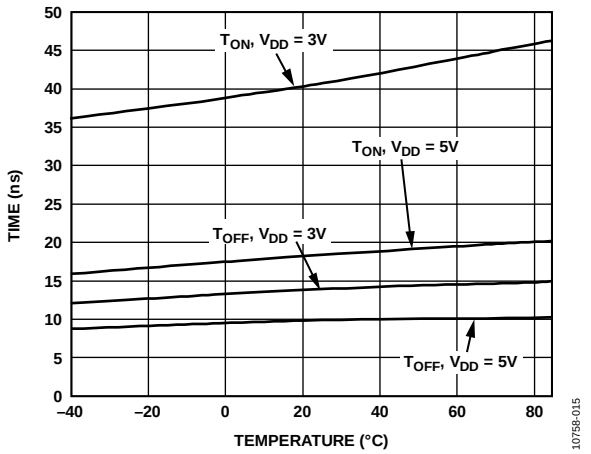


Figure 15. T_{ON}/T_{OFF} Times vs. Temperature

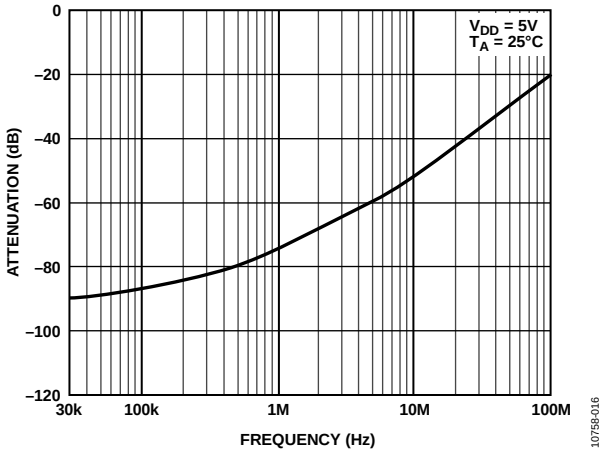


Figure 16. Off Isolation vs. Frequency

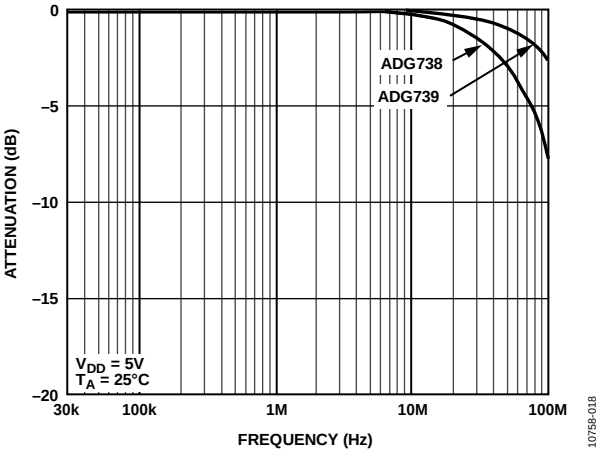


Figure 18. On Response vs. Frequency

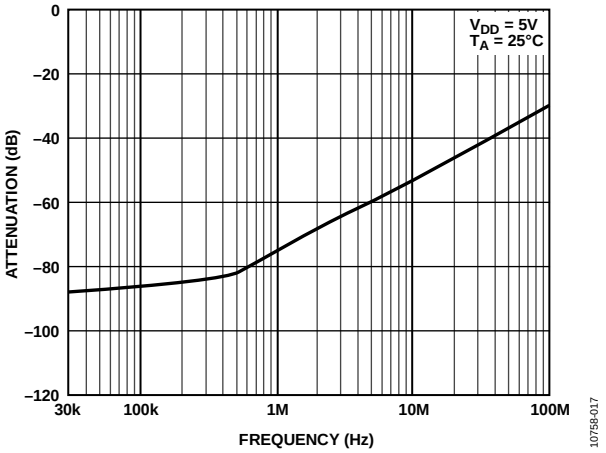


Figure 17. Crosstalk vs. Frequency

TEST CIRCUITS

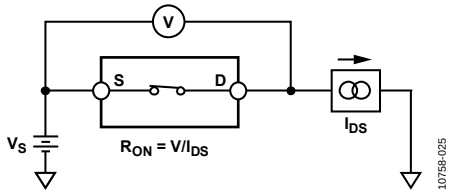


Figure 19. On Resistance

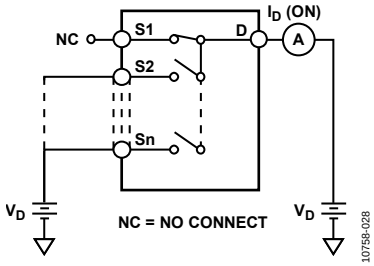


Figure 21. I_S, I_D (On)

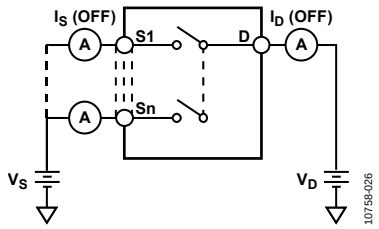


Figure 20. I_D (Off), I_S (Off)

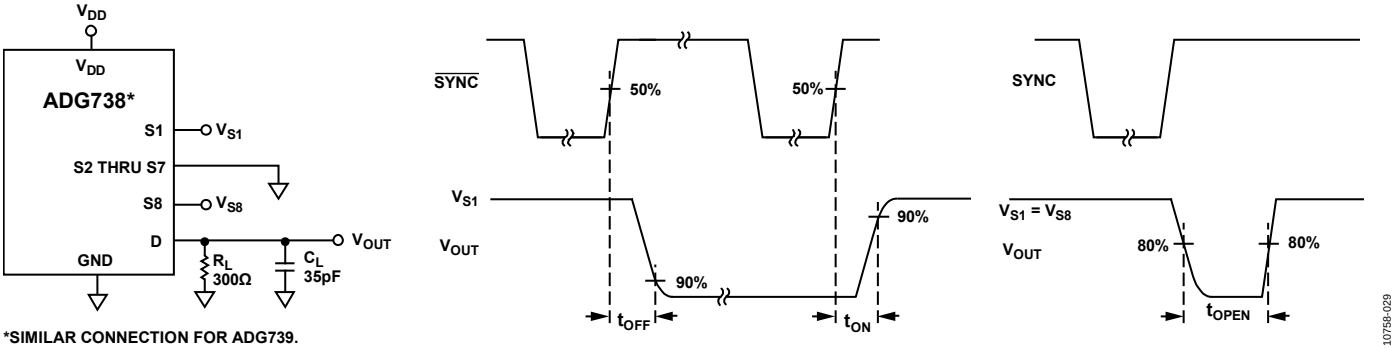


Figure 22. Switching Times and Break-Before-Make Times

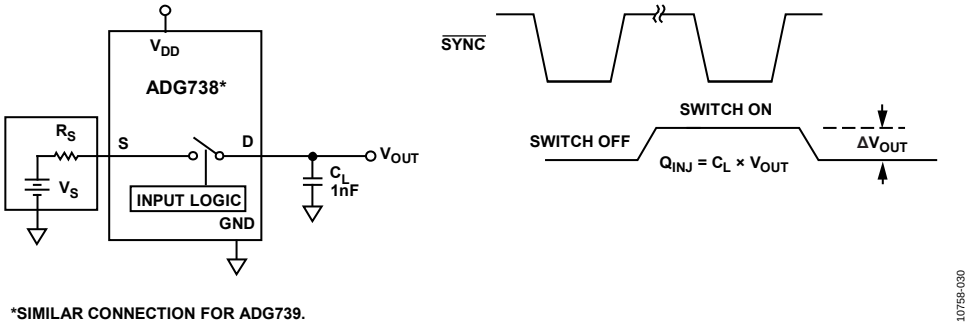
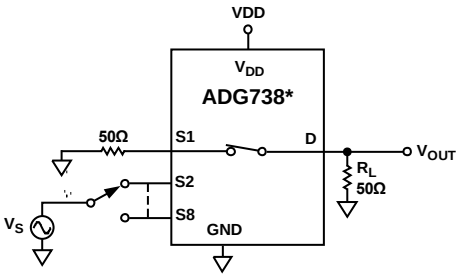


Figure 23. Charge Injection

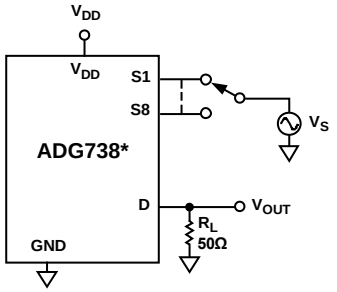


*SIMILAR CONNECTION FOR ADG739.

CHANNEL-TO-CHANNEL CROSSTALK = 20LOG_{10} (V_{OUT}/V_S)

10758-031

Figure 24. Channel-to-Channel Crosstalk



*SIMILAR CONNECTION FOR ADG739.

S1 IS SWITCHED OFF FOR OFF ISOLATION MEASUREMENTS AND ON FOR BANDWIDTH MEASUREMENTS

OFF ISOLATION = 20LOG_{10} (V_{OUT}/V_S)

INSERTION LOSS = $20\text{LOG}_{10}\left(\frac{V_{OUT}\text{ WITH SWITCH}}{V_{OUT}\text{ WITHOUT SWITCH}}\right)$

10758-032

Figure 25. Off Isolation and Bandwidth

TERMINOLOGY

V_{DD}
Most positive power supply potential.

I_{DD}
Positive supply current.

GND
Ground (0 V) reference.

S
Source terminal. May be an input or output.

D
Drain terminal. May be an input or output.

V_D (V_S)
Analog voltage on Terminal D, Terminal S.

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
On resistance match between any two channels, that is, R_{ON}max – R_{ON}min.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
Source leakage current with the switch off.

I_D (Off)
Drain leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (Off)
Off switch source capacitance. Measured with reference to ground.

C_D (Off)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and 90% points of the $\overline{\text{SYNC}}$ rising edge and the switch on condition.

t_{OFF}
Delay time between the 50% and 90% points of the $\overline{\text{SYNC}}$ rising edge and the switch off condition.

t_D
Off time measured between the 80% points of both switches when switching from one switch to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THEORY OF OPERATION

The ADG738 and ADG739 are serially controlled, 8-channel and dual 4-channel matrix switches, respectively. While providing the normal multiplexing and demultiplexing functions, these parts also provide the user with more flexibility as to where their signal may be routed. Each bit of the 8-bit serial word corresponds to one switch of the part. A Logic 1 in the particular bit position turns on the switch, while a Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches on. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Take care, however, in the multiplexing situation where a number of inputs may be shorted together (separated only by the small on resistance of the switch).

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle, as the user may not wish to change the state of some switches. To minimize glitches on the output of these switches, the part cleverly compares the state of switches from the previous write cycle. If the switch is already in the on condition, and is required to stay on, there will be minimal glitches on the output of the switch.

POWER-ON RESET

During device power-up, all switches will be in the off condition and the internal input shift register is filled with zeros and remains so until a valid write takes place.

SERIAL INTERFACE

The ADG738 and ADG739 have a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN), which is compatible with SPI, QSPI, MICROWIRE interface standards and most DSPs. Figure 3 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit input shift register via DIN under the control of the $\overline{\text{SYNC}}$ and SCLK signals. Data may be written to the input shift register in more or less than eight bits. In each case, the input shift register retains the last eight bits that were written.

When $\overline{\text{SYNC}}$ goes low, the input shift register is enabled. Data from DIN is clocked into the input shift register on each falling edge of SCLK. Each bit of the 8-bit word corresponds to one of the eight switches. Figure 26 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy-chaining, delayed, of course, by eight bits. When all eight bits have been written into the shift register, the $\overline{\text{SYNC}}$ line is brought high again. The switches are updated with the new configuration and the input shift register is disabled. With $\overline{\text{SYNC}}$ held high, any further data or noise on the DIN line has no effect on the shift register.

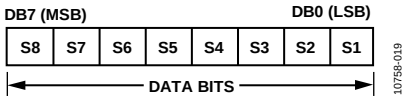


Figure 26. Input Shift Register Contents

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the ADG738/ADG739 is via a serial bus that uses a standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The ADG738/ADG739 requires an 8-bit data word with data valid on the falling edge of SCLK.

Data from the previous write cycle is available on the DOUT pin. The following sections illustrate simple 3-wire interfaces with popular microcontrollers and DSPs.

ADSP-21xx TO ADG738/ADG739

An interface between the ADG738/ADG739 and the ADSP-21xx is shown in Figure 27. In the interface example shown, SPORT0 is used to transfer data to the matrix switch. The SPORT control register should be configured as follows: internal clock operation, alternate framing mode; active low framing signal.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the matrix switch. The update of each switch condition takes place automatically when TFS is taken high.

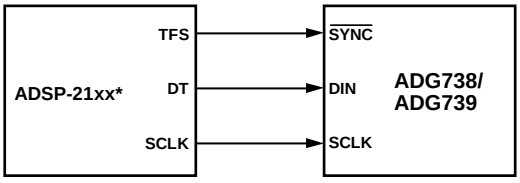


Figure 27. ADSP-21xx to ADG738/ADG739 Interface

8051 INTERFACE TO ADG738/ADG739

A serial interface between the ADG738/ADG739 and the 8051 is shown in Figure 28. TXD of the 8051 drives SCLK of the ADG738/ADG739, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{\text{SYNC}}$.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user has to ensure that the data in the SBUF register is arranged correctly as the switch expects MSB first.

When data is to be transmitted to the matrix switch, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result no glue logic is required between the ADG738/ADG739 and microcontroller interface.

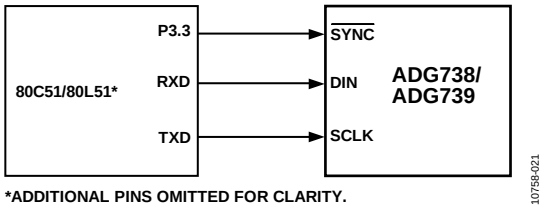


Figure 28. 8051 Interface to ADG738/ADG739

MC68HC11 INTERFACE TO ADG738/ADG739

Figure 29 shows an example of a serial interface between the ADG738/ADG739 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the matrix switch, while the MOSI output drives the serial data line, DIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case PC7.

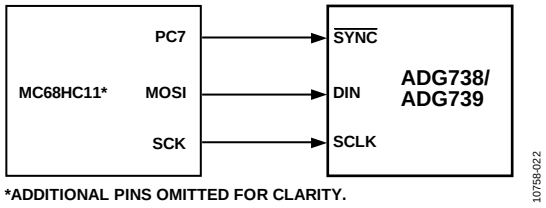


Figure 29. MC68HC11 Interface to ADG738/ADG739

The 68HC11 is configured for master mode; MSTR = 1, CPOL = 0, and CPHA = 1. When data is transferred to the part, PC7 is taken low, data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK.

If the user wishes to verify the data previously written to the input shift register, the DOUT line could be connected to MISO of the MC68HC11, and with $\overline{\text{SYNC}}$ low, the input shift register would clock data out on the rising edges of SCLK.

APPLICATIONS INFORMATION

EXPAND THE NUMBER OF SELECTABLE SERIAL DEVICES USING AN ADG739

The dual 4-channel ADG739 multiplexer can be used to multiplex a single chip select line to provide chip selects for up to four devices on the SPI bus. Figure 30 illustrates the ADG739 in such a typical configuration. All devices receive the same serial clock and serial data, but only one device receives the $\overline{\text{SYNC}}$ signal at any one time. The ADG739 is a serially controlled device also. One bit programmable pin of the microcontroller is used to enable the ADG739 via $\overline{\text{SYNC2}}$, while another bit programmable pin is used as the chip select for the other serial devices, $\overline{\text{SYNC1}}$. Driving $\overline{\text{SYNC2}}$ low enables changes to be made to the addressed serial devices. By bringing $\overline{\text{SYNC1}}$ low, the selected serial device hanging from the SPI bus is enabled and data will be clocked into its input shift register on the falling edges of SCLK. The convenient design of the matrix switch allows for different combinations of the four serial devices to be addressed at any one time. If more devices need to be addressed via one chip select line, the ADG738 is an 8-channel device and would allow further expansion of the chip select scheme. There may be some digital feedthrough from the digital input lines because SCLK and DIN are permanently connected to each device. Using a burst clock minimizes the effects of digital feedthrough on the analog channels.

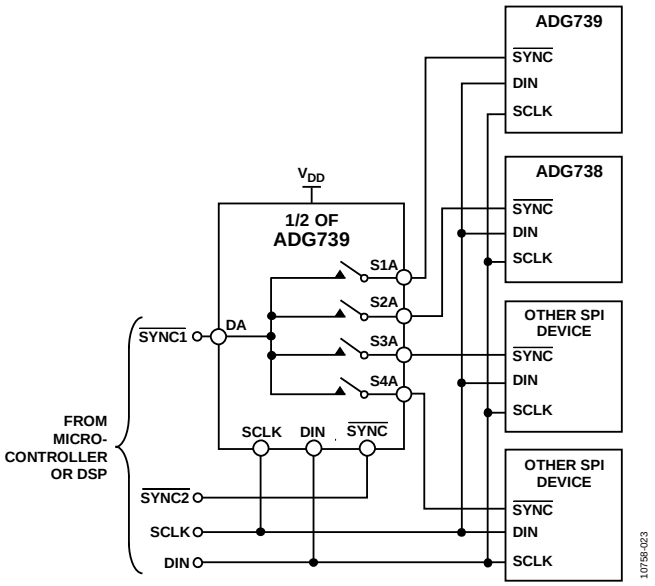


Figure 30. Addressing Multiple Serial Devices Using an ADG739

DAISY-CHAINING MULTIPLE ADG738S

A number of ADG738 matrix switches may be daisy-chained simply by using the DOUT pin. DOUT is an open-drain output that should be pulled to the supply with an external resistor. Figure 31 shows a typical implementation. The $\overline{\text{SYNC}}$ pin of all three parts in the example are tied together. When $\overline{\text{SYNC}}$ is brought low, the input shift registers of all parts are enabled, data is written to the parts via DIN, and clocked through the shift registers. When the transfer is complete, $\overline{\text{SYNC}}$ is brought high and all switches are updated simultaneously. Further shift registers may be added in series.

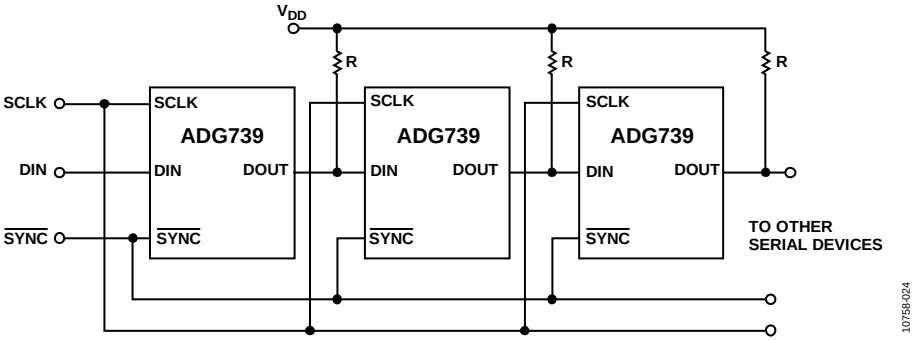


Figure 31. Multiple ADG739 Devices in a Daisy-Chained Configuration

OUTLINE DIMENSIONS

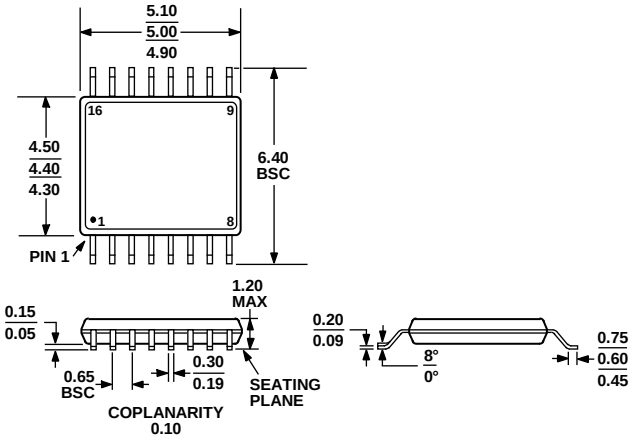


Figure 32. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADG738BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG738BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG738BRUZ-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG738BRUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG738WBRUZ-REEL	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG739BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG739BRU-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG739BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG739BRUZ-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG739BRUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADG738W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

NOTES

D10758-0-11/12(A)

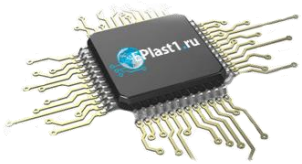
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.